Reconfigurable RF Power Amplifiers on Silicon for Wireless Handsets

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Preface

The design of power amplifiers (*PA*) for wireless applications has been a topic of great concern among the scientific community in electronics since the early 1990s. Power amplifiers dominantly determine the power efficiency and battery lifetime of modern mobile terminals. *PA* linearity is a key feature that limits the maximum allowed data rate of a radio link. The deployment of always more complex radio networks with a continuously growing throughput sharpens the specifications of power amplifiers. The market of wireless handsets (cellular phones, ...) pushes manufacturers towards multi-standard capabilities (3G, Bluetooth, *WIFI*) and a growing level of integration. The *Bill-of-Material* and the consumed die area that are affordable are constantly reduced for cost purpose. The trade-offs that are inherent to *PA* design are therefore extremely stringent and no technical/technological solution can unanimously be regarded as a definitive contribution. To this date, the market of handset-dedicated power amplifiers is widely dominated by *III/V* technologies. However, throughout the following pages, we will try to highlight the benefits of *PA* integration on silicon. The architectures that will be proposed hereunder take advantage of silicon capabilities and strength, among others their relatively low cost and their ability to combine high power devices with low-power analog/digital control circuitry.

Chapter 1 will first present the respective features of 2nd and 3rd generation cellular applications (*GSM*, *DCS*, *EDGE, WCDMA*...) and data transmission standards (*WIFI*, *WIMAX*, *LTE*). An overview of the most commonly employed *RF* power amplifier topologies will also be provided, with their advantages and drawbacks. Finally, the 0.25 μm *BICMOS* ST Microelectronics technology will be described and compared with *III/V* processes in the prospect of *PA* development. The fundamental features of power devices will be detailed and the most appropriate technological choice prior to the *PA* design itself will be discussed.

In Chapters 2 and 3, several novel *PA* topologies will be proposed and discussed in terms of efficiency, linearity and complexity by means of mixed system/transistor-level analyses. Chapter 2 will investigate three novel switched-mode power amplifier topologies. The first non-constant-gain principle is based on the power stage bypass/extinction and applied to a silicon *HBT* demonstrator. A silicon *HBT* demonstrator that was developed in the frame of *RNRT ASTURIES* project will be presented The other two topologies were proposed in the frame of the European Medea+ *UPPERMOST* project and deal with the dynamic control of a fragmented reconfigurable multi-cell power stage. First, open-loop power stage control will be considered. In this topology, power detection is carried out by a specifically dedicated digital ΔΣ *Built-In Current Sensor* whose behavior will be detailed. Second, a closed-loop power stage control system will be addressed and compared with the open-loop power stage control.

Lastly, Chapter 3 will describe a *PA* Module that was developed in the frame of the European *FP6 MOBILIS* project. Furthermore, some mathematical developments and vector illustration will explain the theory of a continuously and dynamically power adaptive system that aims to combine linearity and efficiency even at low power levels. Moreover, frequency-dependent memory effects will be introduced in order to provide some further insight in the complex non-linear phenomenon's that may alter the behavior of power amplifiers operating at wide channel bandwidths. An illustration of memory effects will be provided in the experimental section of this chapter. A *PA* module demonstrator based on integrated silicon and passive network dice will be presented, both in a stand-alone mode and in association with the other blocks of the *MOBILIS* transceiver. The final discussion will validate the proposed efficiency/linearity improvement principle under some conditions of channel bandwidth.

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Contents

Abbreviations

A

ACLR	Adjacent Channel Leakage Ratio
ADC	Analogue to Digital Converter
AGC	Automated Gain control
AM/AM	(Input) Amplitude to (output) Amplitude conversion
AM/PM	(Input) Amplitude to (output) Phase conversion

B

BAW	Bulk Acoustic Wave (resonator)
BER	Bit Error Rate
BICS	Built-In Current Sensor
BOM	Bill Of Material
BPSK	Binary Phase Shift Keying
BV	Breakdown Voltage
BV_{CE}	Collector/Emitter breakdown voltage
BV_{CB}	Collector/Base breakdown voltage
BV_{DS}	Drain/Source breakdown voltage

C

CCDF	Complementary Cumulative Distribution Function
CDMA	Code Division Multiple Access
CHE	Channel Hot-Electron injection
CMFB	Common-Mode Feed-Back
COB	Chip on Board
CW	Continuous-Wave

D

DAC	Digital to Analogue Converter
DACH	Drain Avalanche Hot Carrier injection

DCS	Digital Communication System
DPCCH	Dedicated Physical Control Channel
DPDCH	Dedicated Physical Data Channel
DSP	Digital Signal Processing
DUT	Device Under Test

E

EDGE	Enhanced Data rates for *GSM* Evolution
EER	Envelope Elimination and Restoration
ET	Envelope Tracking
EVM	Error Vector Magnitude

F

FBI	Feed-Back Information
FCC	Federal Communications Commission (USA)
FDD	Frequency Division Duplex

G

GBW	Gain×Bandwidth product
GMSK	Gaussian Minimum-Shift Keying
GPRS	General Packet Radio Service
GSM	Global System for Mobile communications

H

HEMT	High Electron Mobility Transistor
HBT	Hetero-junction Bipolar Transistor
HICUM	HIgh Current transistor Model
HPSK	Hybrid Phase Shift Keying
HS-DPDCH	High-Speed Dedicated Physical Data Channel
HSUPA	High-Speed Uplink Packet Access

I

IF	Intermediate Frequency
IMD_3	3rd order Inter-Modulation Distortion
IPD	Integrated Passive Device
ISI	Inter-Symbol Interference

L

LDD	Lateral Lightly Doping
LDMOS	Laterally Doped MOSFET
LINC	LInear amplification with Non-linear Components
LNA	Low Noise Amplifier
LO	Local Oscillator
LOCOS	LOCal Oxidation of Silicon

N

NF	Noise Figure
nodeB	Base Station
NTF	Noise Transfer Function

O

OCP_1	1 dB Output Compression Point
OED	Oxidation Enhanced Diffusion
OFDM	Orthogonal Frequency Division Multiplexing
OIP_3	3rd order Output-referred Intercept Point
OSR	Over-Sampling Ratio

P

PA	Power Amplifier
PAE	Power Added Efficiency
PAPR	Peak-to-Average Ratio
PCB	Printed Circuit Board
PLL	Phase-Lock Loop
PSK	Phase-Shift Keying
PWM	Pulse Width Modulation

Q

QAM	Quadrature Amplitude Modulation
QOS	Quality of Service
QPSK	Quadrature Phase Shift Keying

R

RNRT	Réseau National de Recherche en Télécommunication (French National Research Network in Telecommunication)
RRC	Root Raised Cosine

RSSI	Received Signal Strength Indicator
RX	Reception path

S

SIP	System in Package
SNR	Signal-to-Noise Ratio
SNDR	Signal-to-Noise/distortion Ratio
SOI	Substrate on Isolator
STF	Signal Transfer Function
STI	Shallow Trench Isolation

T

TDD	Time Division Duplex
TDMA	Time Division Multiple Access
TFCI	Transport Format Channel Information
TPC	Transport Power Control
TQFP	Thin Quad Flat Pack
TX	Transmission path

U

UE	User Equipment

V

VCO	Voltage-Controlled Oscillator
VGA	Variable-Gain Amplifier
VSWR	Voltage Standing-Wave Ratio

W

WCDMA	Wide-band Code Division Multiple Access
WIMAX	Worldwide Interoperability for Microwave Access
WLAN	Wireless Local Area Network