Low-Power VLSI Circuits and Systems

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Preface

Several years ago, I introduced a graduate course entitled “Low Power VLSI Circuits and Systems” (CS60054) to our students at IIT Kharagpur. Although the course became very popular among students, the lack of a suitable textbook was sorely felt. To overcome this problem, I began to hand out lecture notes, which was highly appreciated by the students. Over the years, those lecture notes have gradually evolved into this book. The book is intended as a first-level course on VLSI circuits for graduate and senior undergraduate students. While a basic course on digital circuits is a prerequisite, no background in the area of VLSI circuits is necessary to use this book. Each chapter is provided with an abstract and keywords in the beginning and a chapter summary, review questions and references at the end to meet pedagogical requirements of a textbook. This will help the students in understanding the topics covered and also help the instructors while teaching the subject. The book comprises the following 12 chapters covering different aspects of the digital VLSI circuit design with particular emphasis on low-power aspects. A chapter-wise summary of coverage is given below.

Chapter 1: Introduction

This chapter begins with the historical background that led to the development of present-day VLSI circuits. In the next section, Sect. 1.2, the importance of low-power in high-performance and battery-operated embedded systems is highlighted. Various sources of power dissipation are identified in Sect. 1.3. Low-power design methodologies are introduced in Sect. 1.4.

Chapter 2: MOS Fabrication Technology

The basic metal–oxide–semiconductor (MOS) fabrication processes such as diffusion, photolithography, etc. are introduced in Sect. 2.1. Then, n-type metal–oxide–semiconductor (nMOS) fabrication steps are highlighted in Sect. 2.2 followed by an overview of complementary metal–oxide–semiconductor (CMOS) fabrication steps in Sect. 2.3. The latch-up problem, which is an inherent problem of CMOS circuits, is introduced and two approaches to overcome the latch-up problem are explained in Sect. 2.4. Short channel effects arising out of smaller dimension of MOS devices are highlighted. The chapter ends with Sect. 2.5 with a brief introduction of emerging MOS technologies such as high-K and Fin field-effect transistor (FinFET) to overcome short channel and other effects.

Chapter 3: MOS Transistors

The structure of various types of MOS transistors that can be obtained after fabrication is presented in Sect. 3.1. In Sect. 3.2, characteristics of MOS transistors are explained with the help of fluid model, which helps to understand the operation of a MOS transistor without going into the details of device physics. Three different modes of operation such as accumulation, depletion, and inversion are discussed in Sect. 3.3. Electrical characteristics of MOS transistors are explained in detail in Sect. 3.4. Use of MOS transistors as a switch is explored in Sect. 3.5.

Chapter 4: MOS Inverters

Basic characteristics of an inverter followed by its noise margin are explained in Sect. 4.1. The advantages and disadvantages of different inverter configurations are explored along with their transfer characteristics and noise margin in Sect. 4.2. Section 4.3 considers the inverter ratio in different situations. Switching characteristics of MOS inverters are discussed in Sect. 4.4. Different configurations of MOS inverters on MOS inverters are presented in Sect. 4.4. Various delay parameters have been estimated in Sect. 4.5. Section 4.6 presents different circuit configurations such as super buffers, bipolar CMOS (BiCMOS) inverters, and buffer sizing to drive a large capacitive load.

Chapter 5: MOS Combinational Circuits

The operation of pass transistor logic circuits is introduced in Sect. 5.1. Advantages and limitations of pass transistor logic circuits have been highlighted. Different members of the pass transistor logic family have been introduced. Logic circuits based on gate logic are considered in Sect. 5.2 by considering the realization of NAND and NOR gates. Differences between gate logic and pass transistor logic circuits are highlighted. The operation of MOS dynamic circuits is discussed in Sect. 5.3. The charge sharing and charge leakage problems of MOS dynamic circuits are explained. The clock skew problem of MOS dynamic circuits is introduced. To overcome the clock skew problem, the operation of the domino-CMOS and NORA-CMOS circuits is presented. In Sect. 5.4, realization of several example functions such as full-adder, parity generator, and priority encoder and using different logic styles are considered and compared.

Chapter 6: Sources of Power Dissipation

Various sources of power dissipation in MOS circuits are presented in this chapter. It begins with the explanation of the difference between power and energy. How short circuit power dissipation takes place in CMOS circuits is explained and the expression for short circuit power dissipation is derived in Sect. 6.1. Switching power dissipation in CMOS circuits has been considered in Sect. 6.2 and an expression for switching power dissipation is derived. Switching activity for different types of gates is calculated and that for dynamic CMOS circuits is highlighted. Expression for power dissipation due to charge sharing is derived. Section 6.3 presents glitching power dissipation along with techniques to reduce it. Sources of leakage power dissipation such as subthreshold leakage and gate leakage have been introduced and techniques to reduce them are presented in Sect. 6.4. Various mechanisms which affect the subthreshold leakage current are also highlighted.

Chapter 7: Supply Voltage Scaling for Low Power

In this chapter various voltage scaling techniques starting with static voltage scaling are discussed. The challenges involved in supply voltage scaling for low power are highlighted. The distinction between constant field and constant voltage scaling are explained in detail. First, the physical level-based approach, device feature size scaling, to overcome the loss in performance is discussed in Sect. 7.1. The short-channel effect arising out of feature size scaling is introduced. In Sect. 7.2 architecture level approaches such as parallelism and pipelining for static voltage scaling are discussed. The relevance of multi-core for low power is explained. Static

voltage scaling exploiting high-level transformation is discussed in Sect. 7.3. Multi-level voltage scaling (MVS) approach is explained and various challenges in MVS are highlighted. Dynamic voltage and frequency scheduling (DVFS) approach is discussed in Sect. 7.4. The adaptive voltage scaling (AVS) approach is explained in Sect. 7.5.

Chapter 8: Switched Capacitance Minimization

A system-level approach based on hardware–software co-design is presented in Sect. 8.1. Various bus-encoding techniques are presented in Sect. 8.2. The difference between redundant and non-redundant bus-encoding technique to reduce switching activity is explained in detail. Non-redundant bus encoding technique such as Gray coding technique for address bus is explained. Redundant bus encoding techniques such as one-hot encoding, bus-inversion encoding and T0 encoding techniques are explained with examples. Various aspects of clock gating technique to reduce dynamic power dissipation are provided in Sect. 8.3. Clock gating at different levels of granularity is highlighted. Section 8.4 presents the basic principle behind gated clock finite state machines (FSMs) to reduce switching activity in FSMs. In Sect. 8.5, FSM state encoding approach is presented to minimize switching activity. Another approach for reducing the switching activity of an FSM is FSM partitioning in which a single FSM is partitioned into more than one FSM to reduce switching activity, which is presented in Sect. 8.6. The technique of operand isolation presented in Sect. 8.7 can be used to reduce the switching activity of a combinational circuit. Pre-computation is a technique in which selective computation of output values is done in advance with the objective of using it to reduce switching activity in the subsequent cycles. This technique is presented in Sect. 8.8. The basic approach of minimizing glitching power is considered in Sect. 8.9. Finally, various logic styles including dynamic CMOS and pass transistor logic styles are considered in Sect. 8.10 for low-power logic synthesis.

Chapter 9: Leakage Power Minimization

As multiple threshold voltages are used to minimize leakage power, various approaches for the fabrication of multiple threshold voltage transistors are first presented in Sect. 9.1. Variable threshold voltage CMOS (VTCMOS) approach for leakage power minimization is discussed in Sect. 9.2. Transistor stacking approach based on the stack effect to minimize standby leakage power is highlighted in Sect. 9.3. How run-time leakage power can be minimized by using multiple-threshold voltage (MTCMOS) approach is discussed in Sect. 9.4. Section 9.5 addresses the power-gating technique to minimize leakage power and various issues related to power-gating approaches are highlighted. How power management approach can

be used to reduce leakage power dissipation and how it can be combined with dynamic voltage scaling approach are explained. Isolation strategy is highlighted in Sect. 9.6. State retention strategy is introduced in Sect. 9.7. Power gating controllers are discussed in Sect. 9.8. Power management techniques are considered in Sect. 9.9. Dual-V_t assignment technique is introduced in detail in Sect. 9.10. Delay-constrained dual-V_t technique is presented in Sect. 9.11 and energy constrained dual-V_t technique is considered in Sect. 9.12. Dynamic V_t scaling technique is introduced in Sect. 9.13.

Chapter 10: Adiabatic Logic Circuits

Section 10.1 introduces adiabatic charging which forms the basis of adiabatic circuits. The difference between adiabatic charging and conventional charging of a capacitor is explained. As amplification is a fundamental operation performed by electronic circuits to increase the current or voltage drive, adiabatic amplification is presented in Sect. 10.2. The steps of realization of adiabatic logic gates are explained and illustrated with the help of an example. Adiabatic logic gates are introduced in Sect. 10.3. Realization of pulsed power supply, which is the most fundamental building block of an adiabatic logic circuit is introduced in Sect. 10.4. The realizations of both synchronous and asynchronous pulsed power supplies are explained. How stepwise charging and discharging can be used to minimize power dissipation is explainedin Sect. 10.5. Various partially adiabatic circuits such as efficient charge recovery logic (ECRL), positive feedback adiabatic logic (PFAL), and 2N-2N2Pare introduced and compared in Sect. 10.6.

Chapter 11: Battery-Aware Systems

This chapter discusses few design techniques and proposes an architectural power management method to optimize the battery lifetime and to obtain maximum number of cycles per recharge. Section 11.1 introduces the so called battery gap, which depicts that ever-increasing power requirement versus the actual rate of growth of energy density of the battery technology. An overview of different battery technologies is provided in Sect. 11.2. Section 11.3 introduces different characteristics of a rechargeable battery. The underlying process of battery discharge is explained in Sect. 11.4. Different approaches of battery modeling are briefly introduced in Sect. 11.5. Realizations of battery-driven systems are presented in Sect. 11.6. As an example of a battery-aware system, Sect. 11.7 presents battery-aware sensor networks.

Chapter 12: Software for Low Power

This chapter introduces different software optimization techniques for low power. Power aware software does not require any additional hardware, but performs suitable optimization of software to minimize energy consumption for their execution. The optimization techniques can be broadly classified into two categories: machine independent and machine dependent. Machine-independent optimization techniques are independent of the processor architecture and can be used for any processor. Various software optimization techniques to reduce power consumption without any change in the underlying hardware are considered in this chapter. Both types of software are discussed here. Various sources of power dissipation in the computer hardware are highlighted in Sect. 12.1. Machine-independent software optimizations approaches are discussed in Sect. 12.2. Various loop optimization techniques have been combined with DVFS to achieve larger reduction in energy dissipation; this has been discussed in detail in Sect. 12.3. Power aware software prefetching approach exploit the architectural features of the target processor and the hardware platform, which has been discussed in detail in Sect. 12.4.

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About the Author

Ajit Pal is currently a Professor in the Department of Computer Science and Engineering at Indian Institute of Technology Kharagpur (IITKGP). He received his MTech and PhD degrees for the Institute of Radio Physics and Electronics from Calcutta University in 1971 and 1976, respectively. Before joining IITKGP in the year 1982, he served at Indian Statistical Institute (ISI), Calcutta; Indian Telephone Industries (ITI), Naini; and Defense Electronics Research Laboratory (DLRL), Hyderabad in various capacities. He was designated professor in 1988 and served as Head of Computer Center from 1993 to 1995 and Head of the Computer Science and Engineering Department from 1995 to 1998. His research interests include embedded systems, low-power VLSI circuits, sensor networks and optical communication. He has served as the principal investigator of several sponsored research projects including 'Low Power circuits' sponsored by Intel, USA and 'formal methods for power intent verification', sponsored by Synopsis (India) Pvt. Ltd. He has over 150 publications in reputed journals and conference proceedings and three books entitled *Microprocessors: Principles and Applications, Microcontrollers: Principles and Applications,* and Data Communication and Computer Networks. He is a Fellow of IETE, India and Senior Member of IEEE, USA.

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