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Taimur Rabuske • Jorge Fernandes

Charge-Sharing SAR ADCs for Low-Voltage Low-Power Applications

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Taimur Rabuske
INESC-ID
Instituto Superior Técnico
Universidade de Lisboa
Lisboa, Portugal

Jorge Fernandes
INESC-ID
Instituto Superior Técnico
Universidade de Lisboa
Lisboa, Portugal

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To our families

Preface

The integrated successive-approximation-register (SAR) analog-to-digital converter (ADC) is known to present a remarkable energy efficiency. Additionally, the SAR ADC is a very scaling-friendly architecture, due to its highly digital and switching-intensive nature and its ability to effortlessly accommodate rail-to-rail signals without resorting to precision amplifiers. These characteristics have been boosting the popularity of SAR ADCs as process scaling reduces the transistor's intrinsic gain and supply voltages. The most basic form of an SAR ADC requires a voltage comparator, a digital controller, a track-and-hold (TH) circuitry, and a digital-to-analog converter (DAC).

In most of the reported designs, the DAC of an SAR ADC is capacitive and relies on the charge-redistribution (CR) principle. Alternatively, an SAR ADC that relies on the charge-sharing (CS) principle has been proposed more recently. The main advantages of the CS-ADC are that it is immune to inaccuracies in the reference buffer during the conversion and requires less demanding buffers for the input signal and the reference voltage. Additionally, the CS-ADC allows the use of nonlinear capacitors. On the other hand, the CS-ADC is less tolerant to noise and to the comparator offset, which limits the competitiveness of the architecture. Finally, the literature lacks a comprehensive analysis of the limiting factors of CS-ADCs.

The aim of this book is to fill the gap in knowledge that exists for CS-ADCs by providing an in-depth analysis of the architecture and quantifying its limiting factors. Finally, the insights gained through this analysis are applied to devise techniques that mitigate the critical drawbacks of the architecture and allow the design of energy-efficient SAR ADCs for low-voltage applications. These techniques are validated through the design of two SAR ADCs that operate at supply voltages down to 0.35 and 0.4 V. Experimental results show that the two reported ADCs present the best energy efficiency among ADCs designed in technologies down to 0.13 μm. Additionally, one of the presented prototypes is the first demonstration of SAR ADC that uses a DAC with very-nonlinear capacitors, benefitting from the improved capacitance density and matching characteristics of metal-oxide-semiconductor (MOS) capacitors.

Much of the material presented in this monograph originates from the work carried out by the first author for his Ph.D., at Universidade de Lisboa, Portugal. This work includes original research results that have been presented at international conferences (ESSCIRC, ISCAS, and ICECS, among others), published in Springer *Analog Integrated Circuits and Signal Processing, IEEE Transactions on Very Large Scale Integration (VLSI) Systems and IEEE Journal of Solid-State Circuits.*

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Lisboa, Portugal — Taimur Rabuske
Lisboa, Portugal — Jorge Fernandes
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