

Analog Integrated Circuit Design Automation

Ricardo Martins • Nuno Lourenço • Nuno Horta

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Placement, Routing and Parasitic
Extraction Techniques

 Springer

Ricardo Martins
Instituto Superior Técnico,
Universidade de Lisboa
Instituto de Telecomunicações
Lisboa, Portugal

Nuno Lourenço
Instituto Superior Técnico,
Universidade de Lisboa
Instituto de Telecomunicações
Lisboa, Portugal

Nuno Horta
Instituto Superior Técnico,
Universidade de Lisboa
Instituto de Telecomunicações
Lisboa, Portugal

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Ricardo Martins

To my little girls, Nádia, Joana, and Daniela

Nuno Lourenço

To Alina and Íris

Nuno Horta

To Carla, João, and Tiago

Preface

In the last years, the proliferation of consumer electronic devices triggered a huge increase in microelectronic activities, enabling the growth of the integrated circuit (IC) market from \$10 billion in 1980 to over than \$340 billion in 2015. Due to the developments made in terms of very-large-scale integration technologies, nowadays, designers have the means to build multimillion transistor ICs that implement complete systems in a single chip. The need of new functionalities, smaller devices, more power efficiency, less production and integration costs, and less design cost makes the design of electronic systems a truly challenging task, which must be completed within strict time-to-market constraints. Despite analog blocks representing only a small fraction of the die area, the effort in their design is considerably higher when compared to the effort spent on their digital counterpart, which is reflected in the total development time. Specifically, the development and test cost of analog or mixed-signal components usually surpasses the 50% of total design cost, even though the area occupied can be as low as 3% of the system-on-a-chip.

In digital IC design, several electronic design automation (EDA) tools and design methodologies are available to help designers in keeping up with new capabilities offered by state-of-the-art integration technologies, while analog design automation tools are not keeping up with those challenges. This difference in the level of automation happens because analog is, in general, less systematic, more heuristic and knowledge intensive than its digital counterpart, and becomes critical when digital and analog circuits are integrated together. Furthermore, while new fabrication technologies bring huge advantages to systems' performance, the reduction of devices' sizes and consequent increase in device density does not come only with benefits. This is especially true for the analog layout, where the layout induced disturbances, e.g., substrate noise, cross talk, supply noise, thermal noise, etc., effects became even more significant, having the potential to drastically affect the performance of the circuit. Moreover, the impact of layout-dependent effects, e.g., well proximity effect, poly spacing effect, length of diffusion, oxide to oxide spacing effect, etc., in deeper nanometer technologies can easily drive circuits to malfunction. Analog design automation has been intensively studied in academia for more than two decades, and although much has been accomplished, the fact is that there is still no

mature tool in the industrial environment and the analog layout is mostly done manually using time-consuming layout editors. Applications that provide some kind of user-assisted functionalities found their way into commercial EDA tools; however, the automatic functionalities are limited and lots of problems remain unsolved. For these reasons, the onset of more efficient and user-oriented tools to boost analog designers' productivity and ease this time-consuming task is mandatory.

The work presented in this book belongs to the scientific area of EDA and addresses the automatic generation of analog IC layout. A set of innovative placement, routing, and parasitic extraction methodologies for analog IC design automation were implemented in the tool AIDA-L. AIDA-L, which is integrated in the bottom-up physical synthesis path of an in-house analog IC design automation environment, AIDA, assists the analog designer in the iterative and error-prone process of layout generation. The designer specifies the circuit topology and the required technology and also provides intuitive high-level floorplan guidelines coded in a technology- and specification-independent template file. The high-level floorplan is mapped to a non-slicing topological representation, and the tool instantiates the devices and packs the floorplan for any set of devices' sizes provided. In the absence of the designer's guidelines, an innovative hierarchical multi-objective optimization, over an absolute representation, is used to provide a full Pareto set of placement solutions. For routing, the effects of current densities are considered to construct an electromigration-aware wiring topology for each power and signal network directly from the netlist, and then, several symmetry rules between wires are automatically identified and applied in the global and groundbreaking evolutionary detailed routing phases. Unlike previous approaches, the use of multiport structures for each terminal strongly enhances circuits' routability and the quality of the wiring symmetry. Furthermore, AIDA-L is also suited to the inclusion of layout-related data during automatic circuit sizing, by performing a fast, but accurate, 2.5-D parasitic extraction in loop over a semi-complete layout, whereas competing approaches require the complete detailed layout. The robustness of the automatic layout generation is demonstrated on several analog circuit structures, from simple amplifiers, generated in less than 1 min, to more complex circuits, generated in a few hours, using a 130 nm design process. The output layouts are stored in GDSII format and the results are validated, first, using an industrial-grade verification tool for design rule check and layout versus schematic and, then, with electric simulations over the extracted layouts.

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This book is organized in nine chapters.

Chapter 1 presents a brief introduction to the area of analog IC design, with special emphasis to automatic layout generation. First, a well-accepted design flow for

analog ICs is presented, and then, AIDA-L's features and advances to the state of the art are outlined.

Chapter 2 presents a study of the available tools for analog layout design automation. The chapter starts by addressing the placement and routing problems in EDA, followed by the presentation of the main references of automatic layout generation tools and the most recent advances in analog layout-aware circuit sizing approaches. The available commercial solutions are also outlined throughout the chapter.

Chapter 3 gives an overview of the proposed automatic flow for analog IC design. Details about AIDA-L tool embedded in the AIDA's framework, as a stand-alone low-level layout generator and as part of layout-aware circuit sizing methodology, are presented. Additional detail about the tool's implementation, inputs, outputs, and interfaces is also provided.

Chapter 4 presents the methods used by the template-based Placer to process and place the modules in the floorplan, while following the high-level floorplan guidelines provided by the designer in the template file. Also, the B*-tree layout representation and all extraction and packing procedures are detailed.

Chapter 5 introduces the optimization-based Placer, where a well-known multi-objective evolutionary algorithm is enhanced and applied over the circuit's hierarchy. Instead of the template guidelines, current-flow and current-density considerations are taken, during an optimization over absolute coordinates, to improve the floorplan solutions.

Chapter 6 covers the description of the fully automatic Router architecture and generation procedure, depicting each task implemented in the AIDA-L's Router, i.e., the planning phases (electromigration-aware wiring topology construction and wiring symmetry detection), the global routing procedures (multiport selection and Steiner point assignment), and the evolutionary detailed routing phase.

Chapter 7 explains the methods used in the empirically based parasitic extractor to accurately compute the parasitic structures from a semi-complete layout. The processing of the intercap model tables is detailed, and also, the extraction of all resistive and capacitive structures.

Chapter 8 illustrates the application of the proposed design flow to practical examples on well-known analog circuit structures for a 130 nm design process. Also, placement and routing benchmark sets are used to evaluate each of the developed modules.

Chapter 9 shows the closing remarks, and the future directions for the continuous development of AIDA-L are outlined.

Lisboa, Portugal

Ricardo Martins
Nuno Lourenço
Nuno Horta

Contents

1	Introduction	1
1.1	The AMS IC Design Flow	1
1.2	Motivation for Analog Design Automation	4
1.3	Analog Layout Automation.....	6
1.4	Advances to the State-of-the-Art	8
1.5	Conclusion	9
	References.....	10
2	State-of-the-Art on Analog Layout Automation	11
2.1	Placement.....	12
2.1.1	Analog Topological Constraints.....	12
2.1.2	Floorplan Representations	13
2.1.3	Challenges in Modern Analog Placement.....	17
2.1.4	Optimization Algorithm of Choice: Simulated Annealing.....	20
2.1.5	Commercial Solutions.....	20
2.2	Routing.....	21
2.2.1	From Netlist to Pathfinding.....	21
2.2.2	Electromigration and IR-Drop	22
2.2.3	Electromigration-Aware Approaches	23
2.2.4	Wiring Symmetry.....	24
2.2.5	Commercial Solutions.....	24
2.3	Complete Layout Generation Tools	25
2.3.1	Procedural Generation	25
2.3.2	Template-Based.....	25
2.3.3	Optimization-Based	26
2.3.4	Commercial Solutions.....	27
2.4	Closing the Gap Between Electrical and Physical Design.....	29
2.4.1	Circuit Sizing Task.....	30
2.4.2	Layout Generators Embedded in Layout-Aware Approaches	30
2.4.3	Parasitic Extractors Used in Layout-Aware Approaches	31

- 2.5 Overview of the State-of-the-Art on Analog Layout Automation 32
 - 2.5.1 Support User-Assisted Placement Generation 32
 - 2.5.2 Support Fully-Automatic Placement Generation..... 34
 - 2.5.3 Alleviate Designer from the Routing Task 35
 - 2.5.4 Embedding in a Layout-Aware Circuit Sizing Methodology 35
- 2.6 Conclusions..... 36
- References..... 36
- 3 AIDA-L: Architecture and Integration..... 43**
 - 3.1 Standalone Design Flow 43
 - 3.1.1 User-Assisted Floorplan Generation..... 44
 - 3.1.2 Fully-Automatic Floorplan Generation..... 46
 - 3.2 Standalone Design Flow 47
 - 3.2.1 Inputs..... 48
 - 3.2.2 Outputs..... 51
 - 3.2.3 Technology Design Kit and AIDA-AMG 51
 - 3.2.4 Graphical User Interface 52
 - 3.2.5 Automatic Layout Generation Using AIDA-L..... 53
 - 3.3 Integration on AIDA’s Framework..... 54
 - 3.3.1 Layout-Aware Design Flow 55
 - 3.3.2 Floorplan-Aware Loop..... 56
 - 3.3.3 Parasitic-Aware Loop..... 57
 - 3.4 Conclusion 58
 - References..... 59
- 4 Template-Based Placer 61**
 - 4.1 Template-Based Placer Architecture..... 61
 - 4.2 XML Description for Template-Based Placement..... 63
 - 4.2.1 Automatic Generation from the Netlist..... 63
 - 4.2.2 Designer Guidelines..... 64
 - 4.3 B*-Tree Extraction..... 68
 - 4.4 Instantiation: AIDA’s Analog Module Generator 69
 - 4.4.1 Supported Structures..... 71
 - 4.4.2 Biasing 73
 - 4.4.3 Handling of Complex Layout Structures 74
 - 4.4.4 Multiport Terminals 74
 - 4.5 B*-Tree Packing 76
 - 4.6 Case Study: Simple Differential Amplifier 76
 - 4.6.1 Floorplan Generation: Design 1..... 77
 - 4.6.2 Retargeting Operation: Design 2..... 78
 - 4.6.3 Retargeting Operation: Design 3..... 79
 - 4.7 Conclusion 80
 - References..... 81

- 5 Optimization-Based Placer** 83
 - 5.1 Optimization-Based Placer Architecture..... 84
 - 5.2 Constrained Archive-Based Multi-Objective Simulated Annealing Algorithm 85
 - 5.2.1 Double Annealing Schedule..... 88
 - 5.2.2 Archive Compaction 89
 - 5.3 XML Description for Optimization-Based Placement..... 89
 - 5.4 Hierarchical Placement Optimization in Absolute Coordinates 90
 - 5.4.1 Analog Constraints and Proximity Groups 91
 - 5.4.2 Absolute Coordinates’ Problem Definition 94
 - 5.4.3 Multi-Objective Hierarchical Framework..... 95
 - 5.5 Current-Flow and Current-Density Considerations 96
 - 5.5.1 Current-Flow Constraints..... 96
 - 5.5.2 Current-Density Considerations..... 100
 - 5.5.3 Application in the Hierarchical Framework 100
 - 5.6 Conclusion 101
 - References..... 104
- 6 Fully-Automatic Router** 105
 - 6.1 Router Architecture 105
 - 6.1.1 Evolution of AIDA-L’s Routing Paradigm 106
 - 6.1.2 Current Architecture/Design Flow 106
 - 6.2 Electromigration-Aware Wiring Planner 109
 - 6.2.1 Electromigration and IR-Drop-Reliable Interconnects’ Widths..... 110
 - 6.2.2 Problem Formulation 111
 - 6.2.3 Optimal Wire Planning 113
 - 6.2.4 Strongly Connected Network..... 116
 - 6.3 Symmetry Planner..... 117
 - 6.3.1 Symmetry Extraction 117
 - 6.3.2 Wire Symmetry Analysis 118
 - 6.4 Global Router: Step I—Multilayer Multiport Selection 120
 - 6.4.1 Multiport Multiterminal Signal Nets 120
 - 6.4.2 Multilayer Multiport Obstacle-Aware Grid 121
 - 6.4.3 Multiport Selection 123
 - 6.4.4 Wiring Symmetry in the Pathfinding Algorithm..... 125
 - 6.5 Global Router: Step II—Steiner Point Assignment 126
 - 6.5.1 Basic Assignment..... 126
 - 6.5.2 Assignment over Obstacles..... 127
 - 6.5.3 Symmetry Considerations..... 127
 - 6.6 Detailed Router 130
 - 6.6.1 Evolutionary Algorithm 131
 - 6.6.2 Chromosome Structure 132
 - 6.6.3 Optimization Phases..... 133
 - 6.7 Conclusion 134
 - References..... 135

7 Empirical-Based Parasitic Extractor	137
7.1 Empirical-Based Parasitic Extractor Architecture	137
7.2 <i>Intercap</i> Models Processing	138
7.3 RC Extraction	140
7.3.1 Parasitic Resistance	143
7.3.2 Parasitic Capacitances	144
7.3.3 Geometrical Considerations	147
7.4 Case Study: Single Ended Two-Stage Amplifier	147
7.5 Conclusion	154
References	155
8 Experimental Results	157
8.1 Organization of the Results	157
8.2 Case Study I: Single Stage Amplifier with Gain Enhancement Using Voltage Combiner	159
8.2.1 Inputs: Template File Definition and Floorplan-Aware Circuit Sizing	159
8.2.2 Layout Generation: Template-Based Placer	161
8.2.3 Layout Generation: Optimization-Based Placer with Current-Flow and Current-Density Considerations	164
8.3 Case Study II: Single Ended Two-Stage Amplifier	167
8.3.1 Inputs: Template File Definition and Floorplan-Aware Circuit Sizing	167
8.3.2 Layout Generation: Template-Based Placer	170
8.3.3 Parasitic Extraction and Layout-Aware Circuit Sizing	173
8.4 Case Study III: Two-Stage Folded Cascode Amplifier	175
8.4.1 Parasitic Extraction and Layout-Aware Circuit Sizing	175
8.4.2 Layout Generation: Optimization-Based Placer	179
8.4.3 Layout Generation: Optimization-Based Placer with Current-Flow and Current-Density Considerations	181
8.5 Case Study IV: Operational Transconductance Amplifier	183
8.6 Benchmarks	187
8.6.1 Optimization-Based Placer Benchmark: Single-Objective vs. Multi-Objective	187
8.6.2 MCNC Benchmarks: Optimization-Based Placer vs. Topological	190
8.6.3 Routing Benchmark: Single-Port vs. Multiport	192
8.7 Conclusion	192
References	198
9 Conclusions and Future Work	199
9.1 Conclusions	199
9.2 Future Work	201
9.2.1 Improved Efficiency	201
9.2.2 Radio-Frequency	201
9.2.3 Deep-Nanometer Technologies	202
Index	203

Abbreviations

AIDA	Analog IC Design Automation
AMG	Analog Module Generator
AMOS	Archive-based Multi-objective Simulated Annealing
AMS	Analog and/or Mixed Signal
ASF	Automatically Symmetric Feasible
BSG	Bounded-Sliceline Grid
CAD	Computer-Aided Design
CAMOSA	Constrained Archive-based Multi-Objective Simulated Annealing
CMOS	Complementary Metal-Oxide-Semiconductor
DRC	Design Rule Check
EDA	Electronic Design Automation
EM	Electromigration
ERC	Electrical-Rule Check
GA	Genetic Algorithm
GDS	Graphic Database System
GUI	Graphical User Interface
HB*-tree	Hierarchical B*-Tree
HPWL	Half-Perimeter Wirelength
HS-tree	Hierarchical Slicing Tree
IC	Integrated Circuit
LDS	Layout Description Script
LP	Linear Programming
LVS	Layout Versus Schematic
MIM	Metal-Insulator-Metal
MOEA	Multi-Objective Evolutionary Algorithm
MOM	Metal-Oxide-Metal
MOO	Multi-Objective Optimization
MP	Multiport
MSP	Minimum Spanning Tree
MT	Multiterminal
MTF	Median Time to Failure

NP	Non-deterministic Polynomial-time
NSGA	Non-dominated Sorting Genetic Algorithm
O-Tree	Ordered Tree
POF	Pareto Optimal Front
PVT	Process, Voltage, and Temperature
RSMT	Rectilinear Steiner Minimal Tree
SA	Simulated Annealing
SMT	Steiner Minimal Tree
SO	Single-objective
SoC	System-on-a-Chip
SP	Symmetry Pair
TCG	Transitive Closure Graph
UMC	United Microelectronics Corporation
VLSI	Very-Large-Scale Integration
XML	Extensible Markup Language
WT	Wiring Topology
WS	Wiring Symmetry