Analog Integrated Circuit Design Automation

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Placement, Routing and Parasitic Extraction Techniques

Springer

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ISBN 978-3-319-34059-3 ISBN 978-3-319-34060-9 (eBook)
DOI 10.1007/978-3-319-34060-9

Library of Congress Control Number: 2016941743

Printed on acid-free paper

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The registered company is Springer International Publishing AG Switzerland

Ricardo Martins
To my little girls, Nádia, Joana, and Daniela
Nuno Lourenço
To Alina and Íris
Nuno Horta
To Carla, João, and Tiago

Preface

In the last years, the proliferation of consumer electronic devices triggered a huge increase in microelectronic activities, enabling the growth of the integrated circuit (IC) market from $10 billion in 1980 to over than $340 billion in 2015. Due to the developments made in terms of very-large-scale integration technologies, nowadays, designers have the means to build multimillion transistor ICs that implement complete systems in a single chip. The need of new functionalities, smaller devices, more power efficiency, less production and integration costs, and less design cost makes the design of electronic systems a truly challenging task, which must be completed within strict time-to-market constraints. Despite analog blocks representing only a small fraction of the die area, the effort in their design is considerably higher when compared to the effort spent on their digital counterpart, which is reflected in the total development time. Specifically, the development and test cost of analog or mixed-signal components usually surpasses the 50 % of total design cost, even though the area occupied can be as low as 3 % of the system-on-a-chip.

In digital IC design, several electronic design automation (EDA) tools and design methodologies are available to help designers in keeping up with new capabilities offered by state-of-the-art integration technologies, while analog design automation tools are not keeping up with those challenges. This difference in the level of automation happens because analog is, in general, less systematic, more heuristic and knowledge intensive than its digital counterpart, and becomes critical when digital and analog circuits are integrated together. Furthermore, while new fabrication technologies bring huge advantages to systems' performance, the reduction of devices' sizes and consequent increase in device density does not come only with benefits. This is especially true for the analog layout, where the layout induced disturbances, e.g., substrate noise, cross talk, supply noise, thermal noise, etc., effects became even more significant, having the potential to drastically affect the performance of the circuit. Moreover, the impact of layout-dependent effects, e.g., well proximity effect, poly spacing effect, length of diffusion, oxide to oxide spacing effect, etc., in deeper nanometer technologies can easily drive circuits to malfunction. Analog design automation has been intensively studied in academia for more than two decades, and although much has been accomplished, the fact is that there is still no

mature tool in the industrial environment and the analog layout is mostly done manually using time-consuming layout editors. Applications that provide some kind of user-assisted functionalities found their way into commercial EDA tools; however, the automatic functionalities are limited and lots of problems remain unsolved. For these reasons, the onset of more efficient and user-oriented tools to boost analog designers' productivity and ease this time-consuming task is mandatory.

The work presented in this book belongs to the scientific area of EDA and addresses the automatic generation of analog IC layout. A set of innovative placement, routing, and parasitic extraction methodologies for analog IC design automation were implemented in the tool AIDA-L. AIDA-L, which is integrated in the bottom-up physical synthesis path of an in-house analog IC design automation environment, AIDA, assists the analog designer in the iterative and error-prone process of layout generation. The designer specifies the circuit topology and the required technology and also provides intuitive high-level floorplan guidelines coded in a technology- and specification-independent template file. The high-level floorplan is mapped to a non-slicing topological representation, and the tool instantiates the devices and packs the floorplan for any set of devices' sizes provided. In the absence of the designer's guidelines, an innovative hierarchical multi-objective optimization, over an absolute representation, is used to provide a full Pareto set of placement solutions. For routing, the effects of current densities are considered to construct an electromigration-aware wiring topology for each power and signal network directly from the netlist, and then, several symmetry rules between wires are automatically identified and applied in the global and groundbreaking evolutionary detailed routing phases. Unlike previous approaches, the use of multiport structures for each terminal strongly enhances circuits' routability and the quality of the wiring symmetry. Furthermore, AIDA-L is also suited to the inclusion of layout-related data during automatic circuit sizing, by performing a fast, but accurate, 2.5-D parasitic extraction in loop over a semi-complete layout, whereas competing approaches require the complete detailed layout. The robustness of the automatic layout generation is demonstrated on several analog circuit structures, from simple amplifiers, generated in less than 1 min, to more complex circuits, generated in a few hours, using a 130 nm design process. The output layouts are stored in GDSII format and the results are validated, first, using an industrial-grade verification tool for design rule check and layout versus schematic and, then, with electric simulations over the extracted layouts.

Finally, the authors would like to express their gratitude for the financial support that made this work possible. The work developed in this book was supported in part by the Fundação para a Ciência e Tecnologia (grant FCT-SFRH/BD/86608/2012, grant FCT-SFRH/BPD/104648/2014, research project DISRUPTIVE EXCL/EEI-ELC/0261/2012, and research project UID/EEA/50008/2013) and by the Instituto de Telecomunicações (research project OPERA-PEst-OE/EEI/LA0008/2013).

This book is organized in nine chapters.

Chapter 1 presents a brief introduction to the area of analog IC design, with special emphasis to automatic layout generation. First, a well-accepted design flow for

analog ICs is presented, and then, AIDA-L's features and advances to the state of the art are outlined.

Chapter 2 presents a study of the available tools for analog layout design automation. The chapter starts by addressing the placement and routing problems in EDA, followed by the presentation of the main references of automatic layout generation tools and the most recent advances in analog layout-aware circuit sizing approaches. The available commercial solutions are also outlined throughout the chapter.

Chapter 3 gives an overview of the proposed automatic flow for analog IC design. Details about AIDA-L tool embedded in the AIDA's framework, as a stand-alone low-level layout generator and as part of layout-aware circuit sizing methodology, are presented. Additional detail about the tool's implementation, inputs, outputs, and interfaces is also provided.

Chapter 4 presents the methods used by the template-based Placer to process and place the modules in the floorplan, while following the high-level floorplan guidelines provided by the designer in the template file. Also, the B*-tree layout representation and all extraction and packing procedures are detailed.

Chapter 5 introduces the optimization-based Placer, where a well-known multi-objective evolutionary algorithm is enhanced and applied over the circuit's hierarchy. Instead of the template guidelines, current-flow and current-density considerations are taken, during an optimization over absolute coordinates, to improve the floorplan solutions.

Chapter 6 covers the description of the fully automatic Router architecture and generation procedure, depicting each task implemented in the AIDA-L's Router, i.e., the planning phases (electromigration-aware wiring topology construction and wiring symmetry detection), the global routing procedures (multiport selection and Steiner point assignment), and the evolutionary detailed routing phase.

Chapter 7 explains the methods used in the empirically based parasitic extractor to accurately compute the parasitic structures from a semi-complete layout. The processing of the intercap model tables is detailed, and also, the extraction of all resistive and capacitive structures.

Chapter 8 illustrates the application of the proposed design flow to practical examples on well-known analog circuit structures for a 130 nm design process. Also, placement and routing benchmark sets are used to evaluate each of the developed modules.

Chapter 9 shows the closing remarks, and the future directions for the continuous development of AIDA-L are outlined.

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Contents

Abbreviations

AIDA	Analog IC Design Automation
AMG	Analog Module Generator
AMOSA	Archive-based Multi-objective Simulated Annealing
AMS	Analog and/or Mixed Signal
ASF	Automatically Symmetric Feasible
BSG	Bounded-Sliceline Grid
CAD	Computer-Aided Design
CAMOSA	Constrained Archive-based Multi-Objective Simulated Annealing
CMOS	Complementary Metal-Oxide-Semiconductor
DRC	Design Rule Check
EDA	Electronic Design Automation
EM	Electromigration
ERC	Electrical-Rule Check
GA	Genetic Algorithm
GDS	Graphic Database System
GUI	Graphical User Interface
HB*-tree	Hierarchical B*-Tree
HPWL	Half-Perimeter Wirelength
HS-tree	Hierarchical Slicing Tree
IC	Integrated Circuit
LDS	Layout Description Script
LP	Linear Programming
LVS	Layout Versus Schematic
MIM	Metal-Insulator-Metal
MOEA	Multi-Objective Evolutionary Algorithm
MOM	Metal-Oxide-Metal
MOO	Multi-Objective Optimization
MP	Multiport
MSP	Minimum Spanning Tree
MT	Multiterminal
MTF	Median Time to Failure

NP	Non-deterministic Polynomial-time
NSGA	Non-dominated Sorting Genetic Algorithm
O-Tree	Ordered Tree
POF	Pareto Optimal Front
PVT	Process, Voltage, and Temperature
RSMT	Rectilinear Steiner Minimal Tree
SA	Simulated Annealing
SMT	Steiner Minimal Tree
SO	Single-objective
SoC	System-on-a-Chip
SP	Symmetry Pair
TCG	Transitive Closure Graph
UMC	United Microelectronics Corporation
VLSI	Very-Large-Scale Integration
XML	Extensible Markup Language
WT	Wiring Topology
WS	Wiring Symmetry