Brain-Machine Interface

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To my son Viggo Alan and
my daughter Emma

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About the Author

Amir Zjajo received the M.Sc. and DIC degrees from the Imperial College London, London, UK, in 2000 and the Ph.D. degree from Eindhoven University of Technology, Eindhoven, The Netherlands in 2010, all in electrical engineering. In 2000, he joined Philips Research Laboratories as a member of the research staff in the Mixed-Signal Circuits and Systems Group. From 2006 to 2009, he was with Corporate Research of NXP Semiconductors as a Senior Research Scientist. In 2009, he joined Delft University of Technology as a Faculty member in the Circuit and Systems Group.

Dr. Zjajo has published more than 70 papers in referenced journals and conference proceedings, and holds more than ten US patents or patent pending. He is the author of the books, *Low-Voltage High-Resolution A/D Converters: Design, Test and Calibration* (Springer 2011, Chinese translation 2015), and *Stochastic Process Variations in Deep-Submicron CMOS: Circuits and Algorithms* (Springer 2014). He serves as a member of Technical Program Committee of IEEE Design, Automation and Test in Europe Conference, IEEE International Symposium on Circuits and Systems, IEEE International Symposium on VLSI, IEEE International Symposium on Nanoelectronic and Information Systems, and IEEE International Conference on Embedded Computer Systems.

His research interests include power-efficient mixed-signal circuit and system design for health and mobile applications and neuromorphic electronic circuits for autonomous cognitive systems. Dr. Zjajo won the best paper award at BIODEVICES 2015 and DATE 2012.

Abbreviations

A/D	Analog to Digital
ADC	Analog-to-Digital Converter
ANN	Artificial Neural Network
AP	Action Potentials
BDF	Backward Differentiation Formula
BMI	Brain Machine Interface
BSIM	Berkeley Short-Channel IGFET Model
CAD	Computer-Aided Design
CDF	Cumulative Distribution Function
CMOS	Complementary MOS
CMRR	Common-Mode Rejection Ratio
D/A	Digital to Analog
DAC	Digital-to-Analog Converter
DAE	Differential Algebraic Equations
DFT	Discrete Fourier Transform
DIBL	Drain-Induced Barrier Lowering
DNL	Differential Nonlinearity
DR	Dynamic Range
DSP	Digital Signal Processor
DTFT	Discrete Time Fourier Transform
EM	Expectation Maximization
ENOB	Effective Number of Bits
ERBF	Exponential Radial Basis Function
ERBW	Effective Resolution Bandwidth
FFT	Fast Fourier Transform
GBW	Gain–Bandwidth Product
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
INL	Integral Nonlinearity

ITDFT	Inverse Time Discrete Fourier Transform
KCL	Kirchhoff' Current Law
KKT	Karush–Kuhn–Tucker
LFP	Local Field Potentials
LNA	Low Noise Amplifier
LSB	Least Significant Bit
MNA	Modified Nodal Analysis
MOS	Metal Oxide Semiconductor
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
MSB	Most Significant Bit
NA	Nodal Analysis
NMOS	Negative doped MOS
ODE	Ordinary Differential Equation
OTA	Operational Transconductance Amplifier
PDE	Partial Differential Equation
PDF	Probability Density Function
PGA	Programmable Gain Amplifier
PMOS	Positive doped MOS
PPA	Power per Area
PSD	Power Spectral Density
PSRR	Power Supply Rejection Ratio
QP	Quadratic Problem
QPO	Quadratic Program Optimization
RBF	Radial Basis Function
RTL	Register Transfer Level
S/H	Sample and Hold
SAR	Successive Approximation Register
SC	Switched Capacitor
SDE	Stochastic Differential Equation
SFDR	Spurious-Free Dynamic Range
SINAD	Signal-to-Noise and Distortion
SNDR	Signal-to-Noise plus Distortion Ratio
SNR	Signal-to-Noise Ratio
SPICE	Simulation Program with Integrated Circuit Emphasis
SRAM	Static Random-Access Memory
STI	Shallow Trench Isolation
SVD	Singular Value Decomposition
SVM	Support Vector Machine
T/D	Time to Digital
T/H	Track and Hold
TDC	Time-to-Digital Converter
THD	Total Harmonic Distortion
V/I	Voltage to Current
VCCS	Voltage-Controlled Current Sources

VGA	Variable Gain Amplifier
VTC	Voltage-to-Time Converter
WCD	Worst Case Design
WSS	Wide Sense Stationary

Symbols

a	Elements of the incidence matrix A, bounds
A	Amplitude, area, constant singular incidence matrix
A_f	Voltage gain of feedback amplifier
A_{fmb}	Mid-band gain of amplifier
b	Number of circuit branches, vector of biases, bounds
B_i	Number of output codes
B	Bit, effective stage resolution
B_n	Noise bandwidth
BW	Bandwidth
c_i	Class to which the data x_i from the input vector belongs
c_{xy}	Process correction factors depending upon the process maturity
C^*	Neyman–Pearson Critical region
C	Capacitance, covariance matrix
C_C	Compensation capacitance, cumulative coverage
C_{eff}	Effective capacitance
C_G	Gate capacitance, input capacitance of the operational amplifier
C_{GS}	Gate-Source capacitance
C_{in}	Input capacitance
C_L	Load capacitance
C_{out}	Parasitic output capacitance
C_{ox}	Gate-oxide capacitance
C_{par}	Parasitic capacitance
C_{tot}	Total load capacitance
C_Q	Function of the deterministic initial solution
$C_{\Xi\Xi}$	Autocorrelation matrix
$C_{\varsigma\varsigma}$	Symmetrical covariance matrix
d_i	Location of transistor i on the die with respect to a point of origin
D_i	Multiplier of reference voltage
D_{out}	Digital output
e	Noise, error, scaling parameter of transistor current

e_q	Quantization error
e^2	Noise power
$E\{.\}$	Expected value
E_{conv}	Energy per conversion step
f_{clk}	Clock frequency
f_{in}	Input frequency
$f_{p,n}(d_i)$	Eigenfunctions of the covariance matrix
f_S	Sampling frequency
f_{sig}	Signal frequency
f_{spur}	Frequency of spurious tone
f_T	Transit frequency
$f(x,t)$	Vector of noise intensities
F_Q	Function of the deterministic initial solution
g	Conductance
g_m	Transconductance
G_i	Interstage gain
G_m	Transconductance
h	Numerical integration stepsize, surface heat transfer coefficient
i	Index, circuit node, transistor on the die
$i_{\max}$	Number of iteration steps
I	Current
I_{amp}	Total amplifier current consumption
I_{diff}	Difussion current
I_D	Drain current
I_{DD}	Power supply current
I_{ref}	Reference current
j	Index, circuit branch
J_0	Jacobian of the initial data z_0 evaluated at p_i
k	Boltzmann's coefficient, error correction coefficient, index
K	Amplifier current gain, gain error correction coefficient
$K(t)$	Variance–covariance matrix of $\lambda(t)$
L	Channel length
L_i	Low-rank Cholesky factors
$L(\theta\|T_X)$	Log-likelihood of parameter θ with respect to input set T_X
m	Index
M	Number of terms, number of channels in BMI
n	Index, number of circuit nodes, number of bits
N	Number of bits
N_{aperture}	Aperture jitter limited resolution
P	Power
p	Process parameter
$p(d_i,\theta)$	Stochastic process corresponding to process parameter p
$\mathrm{p}_{X\|\Theta}(x\|\theta)$	Gaussian mixture model
p^*	Process parameter deviations from their corresponding nominal values

p_1	Dominant pole of amplifier
p_2	Nondominant pole of amplifier
q	Channel charge, circuit nodes, index, vector of state variables
r	Circuit nodes, number of iterations
R	Resistance
r_{ds}	Output resistance of a transistor
R_{eff}	Effective thermal resistance
R_{on}	Switch on-resistance
$R_{n\text{-}1}$	Process noise covariance
r_{out}	Amplifier output resistance
S_i	Silicon
S_n	Output vector of temperatures at sensor locations
s	Scaling parameter of transistor size, score
t	Time
T	Absolute temperature, transpose, time, transistor
t_{ox}	Oxide thickness
t_S	Sampling time
v_f	Fractional part of the analog input signal
v_n	Input-referred noise of the amplifier
u_n	Gaussian sensor noise
V	Voltage
V_{CM}	Common-mode voltage
V_{DD}	Positive supply voltage
V_{DS}	Drain-source voltage
$V_{\text{DS,SAT}}$	Drain-source saturation voltage
V_{FS}	Full-scale voltage
V_{GS}	Gate-source voltage
V_{in}	Input voltage
V_{LSB}	Voltage corresponding to the least significant bit
V_{off}	Offset voltage
V_{ref}	Reference voltage
V_T	Threshold voltage
U_T	Thermal voltage
w	Normal vector perpendicular to the hyperplane, weight
w_i	Cost of applying test stimuli performing test number i
W	Channel width, Wiener process parameter vector, loss function
W^*, L^*	Geometrical deformation due to manufacturing variations
x	Vector of unknowns
x_i	Vectors of observations
$x(t)$	Analog input signal
X	Input, observability Gramian
y_0	Arbitrary initial state of the circuit
$y[k]$	Output digital signal
y	Yield

Y	Output, controllability Gramian
z_0	Nominal voltages and currents
$z_{(1-\alpha)}$	(1-α)-quantile of the standard normal distribution Z
z[k]	Reconstructed output signal
Z	Low rank Cholesky factor
α	Neyman–Pearson significance level, weight vector of the training set
β	Feedback factor, transistor current gain, bound
γ	Noise excess factor, measurement correction factor, reference errors
γ_i	Iteration shift parameters
δ	Relative mismatch
ε	Error
ζ	Distributed random variable, forgetting factor
η	Random vector,
θ	Die, unknown parameter vector, coefficients of mobility reduction
$\vartheta_{p,n}$	Eigenvalues of the covariance matrix
κ	Converter transition code, subthreshold gate coupling coefficient
λ	Threshold of significance level α, white noise process
λ_κ	Central value of the transition band
μ	Carrier mobility, mean value, iteration step size
ν	Fitting parameter estimated from the extracted data
ξ	Yield bound
$\xi(t)$	Vector of independent Gaussian white noise sources
ξ_i	Degree of misclassification of the data x_i
$\xi_n(\theta)$	Vector of zero-mean uncorrelated Gaussian random variables
ρ	Correlation parameter reflecting the spatial scale of clustering
ς_p	Random vector accounting for device tolerances
σ	Standard deviation
U_n	Measurement noise covariance
τ	Time constant
ω	Matrix of normal vectors
Φ	Set of all valid design variable vectors in design space
φ	Clock phase, Mercer kernel
ϕ_T	Thermal voltage at the actual temperature
χ	Circuit performance function
$\Gamma_{rf}[.]$	Probability function
Δ	Relative deviation, yield constraint violation
Ξ_r	Boundaries of voltage of interest
Σ	Covariance matrix
Ω	Sampling space