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High-Ratio Voltage Conversion in CMOS for Efficient Mains-Connected Standby

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Preface

The focus of this work can be seen as making the bridge between the fields of Solid-State Integrated Circuits (IC) and Power Electronics. Multiple AC-DC and DC–DC power converters are investigated from the IC standpoint, this means a constant effort to realize converters that are fully integrated on a single chip, or have at least a very high level of integration. Moreover, it is of paramount importance to improve power conversion efficiency throughout the transport chain of energy from source (e.g., a battery, the mains) to load (i.e., the application which is the consumer). Creating new converter systems that are very efficient and integrated into chip-scale solutions enables the benefit of longer battery autonomy in portable devices, on top of enabling ever lighter and slimmer devices. In non-mobile applications, less power is required from the mains for the same functionality, and consequently, this helps to reduce emissions related to electricity generation, such as carbon dioxide, etc. To summarize this work, a few different research targets are introduced: (1) monolithic switched-capacitor DC–DC conversion for granular power delivery on-chip, (2) reduction of standby power in mains-connected devices through the addition of an efficient and compact auxiliary supply to provide power during standby mode, and (3) high-ratio DC–DC voltage conversion in a monolithic context.

Modern integrated circuits contain more and more functionality within a single chip. These are also called Systems on Chip, and examples of such systems are the Application Processing Unit chips at the heart of today's smartphones or personal computers. Because these single-chip systems house a large amount of subsystems, it is only logical that they require multiple different supply voltages to power these functions. In the past, most required voltages were generated off-chip on the printed circuit board, in the vicinity of the chip. This approach, however, is becoming less and less viable due the growing number of desired supply voltages and the associated number of interconnection pins to get the power from the off-chip power converters to the on-chip loads. Moreover, there are other negative aspects related to this approach. Therefore, a better approach is to provide the chip with one, or a few, different supply voltages, and use on-chip power converters to further provide the desired supply voltages. This requires less package pins and enables better regulation of the desired supply voltage, since the feedback loop

can now be performed locally on the chip. The goal of this work is to enable the above. To that end, an investigation of suitable fully integrated DC–DC converters is conducted. Specifically, the realization of a switched-capacitor DC–DC converter in a standard CMOS technology with a high power density was targeted. It is important to implement the converter in a standard CMOS process to enable co-integration with its loading circuits on the same chip. Secondly, a high power conversion density yields a lower chip area requirement to implement the converter. This work investigated circuit techniques to deliver top-notch specifications, given this context.

Standby power is caused by mains-connected devices in standby mode. They have a power supply that is optimized for the active mode, where power levels may be very large with respect to the low required power level of standby, a factor 100× or more. It cannot be expected that these converters are efficient both at their nominal power (active mode) and also at light-load (standby mode) condition. Therefore, the power consumption of mains-connected devices is much higher than what it could be. Since standby power on a global scale is associated to about 10 % of residential electricity consumption and 1 % of CO_2 emissions, standby power reduction could help to counter global warming. Therefore, this work aims to build the AC–DC converters that enable such reductions in standby power and prevent the associated emissions.

The research toward high-ratio voltage conversion in an integrated context is motivated by the research conclusion, of the previous work on AC–DC converters, that switched-capacitor DC–DC converters are particularly well suited for this task. Monolithic high-ratio DC–DC conversion can, for example, be used to deliver high voltages from a standard Li-ion battery in a very small and light form factor, which is particularly important for robotic insects, where high voltages are required in the drivers that power the wings. Switched-capacitor DC–DC converters do not rely on the duty cycle to set their voltage conversion ratio, as its popular inductive buck converter counterpart does, and can therefore maintain a 50 % duty cycle, regardless of the actual voltage conversion ratio. Instead, the conversion ratio is a consequence of the switched-capacitor topology. As such, it is a better candidate for high-ratio voltage conversion than the buck converter, which in this case is more affected by efficiency limiting drawbacks, due to its reliance on very low duty cycles in order to obtain high voltage conversion ratios. The research in this work explores, given the system-level choice for the SC DC–DC converter, which topology is expected to yield the best performance, considering the typical context of CMOS integration.

Contents

List of Abbreviations

AC	Alternating Current
ARG	Auxiliary Rail Generator
AVS	Adaptive Voltage Scaling
CMOS	Complementary Metal-Oxide Semiconductor
CO_2	Carbon dioxide
COTS	Commercial Off-The-Shelf
CVD	Chemical Vapor Deposition
DC	Direct Current
DFS	Dynamic Frequency Scaling
DVS	Dynamic Voltage Scaling
EEF	Efficiency Enhancement Factor
EMC	ElectroMagnetic Compatibility
ESR	Equivalent Series Resistance
FSL	Fast Switching Limit
GHG	Greenhouse gas
GO	Gate Oxide
IC	Integrated Circuit
ICR	Intrinsic Charge Recycling
IO	Input Output
IoE	Internet of Everything
IoT	Internet of Things

LDMOS	Laterally-Diffused Metal-Oxide Semiconductor
LDO	Low-DropOut
MIM	Metal-Insulator-Metal
MIMO	Multiple-Input Multiple-Output
MOM	Metal-Oxide-Metal
NMOS	N-type MOS
PCB	Printed Circuit Board
PDN	Power Delivery Network
PFC	Power Factor Correction
PFM	Pulse-Frequency Modulation
PMIC	Power Management Integrated Circuit
PMOS	P-type MOS
PMU	Power Management Unit
PSiP	Power System-in-Package
PSoC	Power System-on-Chip
ReSC	Resonant Switched-Capacitor
SO_2	Sulfur dioxide
SoC	System on Chip
SOI	Silicon On Insulator
SOS	Silicon On Sapphire
SSL	Slow Switching Limit
VCO	Voltage-Controlled Oscillator
VCR	Voltage Conversion Ratio
VHF	Very High Frequency
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

List of Symbols

α	Ratio of C_{par} to C_{fly}
η_x	Efficiency of x
γ	Ratio of V_o to $V_{o,id}$
ΔV_{C_x}	Voltage variation on capacitor x
$a_{c,i}$	Charge flow of capacitor i to the output charge
$a_{r,i}$	Charge flow of switch i to the output charge
C_{DC}	Decoupling capacitor
C_{fly}	Flying capacitor
C_{in}	Input decoupling capacitor in DC–DC conversion context; high-voltage input-series capacitor in AC–DC conversion context
C_{out}	Output capacitor
C_{par}	Bottom-plate parasitic capacitor
f_{sw}	Switching frequency
K_c	Topology-specific flying capacitor utilization value
k_c	Topology-specific flying capacitor utilization vector
k_s	Topology-specific power switch utilization vector
M_{sw}	Swing metric of the bottom-plate capacitor loss
N	Number of converter fragments in a multi-phase time-interleaved converter
P_i ; P_{in}	Input power
P_o ; P_{out}	Output power
R_L	Load impedance
R_o ; R_{out}	Converter output impedance
R_{dyn}	Impedance to model the dynamic converter loss
R_{esr}	Equivalent series resistance
R_{fsl}	Fast switching limit converter output impedance
R_{route}	Routing impedance
R_{ssl}	Slow switching limit converter output impedance
T_{CLK}	Clock period
t_{dead}	Dead-time between non-overlapping clock phases

t_{off}	Rectifier off-time
V_{AC}	Mains amplitude
V_{C_x}	Voltage of capacitor x
V_{dd}	Nominal supply voltage
V_i ; V_{in}	Input voltage
V_{min}	Lowest allowed supply voltage value
$V_{O,eff}$	Flying capacitor voltage value at the end of a charge-transfer phase
$V_{o,id}$	Open-circuit converter output voltage
$V_{O,max}$	Theoretical maximum flying capacitor voltage value at the beginning of a charge-transfer phase
V_o ; V_{out}	Output voltage
V_{R_o}	Voltage drop over converter output impedance
V_{ref}	Reference voltage
V_{reg}	Regulated voltage
V_{supply}	Supply voltage
V_{th}	Transistor threshold voltage