Analog Circuits and Signal Processing

More information about this series at http://www.springer.com/series/7381

Nele Reynders • Wim Dehaene

Ultra-Low-Voltage Design of Energy-Efficient Digital Circuits

Springer

Nele Reynders
ESAT-MICAS, KU Leuven
Heverlee, Belgium

Wim Dehaene
ESAT-MICAS, KU Leuven
Heverlee, Belgium

ISSN 1872-082X ISSN 2197-1854 (electronic)
Analog Circuits and Signal Processing
ISBN 978-3-319-16135-8 ISBN 978-3-319-16136-5 (eBook)
DOI 10.1007/978-3-319-16136-5

Library of Congress Control Number: 2015935431

Springer Cham Heidelberg New York Dordrecht London

Printed on acid-free paper

Springer International Publishing AG Switzerland is part of Springer Science+Business Media (www.springer.com)

Preface

These days the Internet of Things (IoT) is the big focus when conceiving digital systems. Given the billions of nodes that are ultimately projected for IoT, low energy signal processing is the holy grail. Ignoring the question whether or not the grail can actually be found, we thus embarked on a quest for a significant reduction of the energy consumption per digital operation. The first parameter that catches the eye when wishing to reduce energy is the power supply voltage. We all know that dynamic energy per operation is "cap-times-V_{dd}-square". So the obvious conclusion is: let us reduce the power supply voltage as much as possible. That was the starting point of the design.

As always in research, it is not that simple: the square is only dynamic energy, at low voltages the robustness reduces considerably and so on. Where this research journey will end, is the subject of the book you are holding. However, we can already tell you that it was an exciting journey. Among others, transmission gate logic was reborn and general purpose technologies proved to be more low power than actual low power technologies. The temporary end of the quest, the result of one Ph.D., is described in this book. It consists of novel circuits with lower than state-of-the-art energy consumption, at least at the time of this writing. These circuits, ranging from a small adder to a complete JPEG encoder, are proven on silicon in different technologies. Our research results will give you the practical inspiration to design ultra-low-energy circuits based on the novel principles we describe. There is no fully automated design flow yet. That is for a next book.

We hope, dear reader, that after reading this book you will share our enthusiasm. We are convinced that we have set important steps toward true low energy design. We actually show that mismatch can be dealt with despite the sub-threshold exponential current regime. As such we can guarantee sub-threshold robustness at ultra-low supply voltage. Enjoy!

Heverlee, Belgium — Nele Reynders
January 2015 — Wim Dehaene

Contents

Abstract

Nowadays, energy-efficiency is becoming more and more a decisive parameter for digital systems, driven by the ever increasing number of portable applications. Mobile phones are an obvious example, but many other portable electronic devices are emerging which have less stringent speed requirements but even more critical energy requirements. Since their stand-alone time is dependent on the fixed available energy budget, research toward significant improvements in energy consumption per operation is paramount. Especially medical applications such as biomedical sensor nodes can benefit greatly from a drastically increased energy-efficiency.

By extremely reducing the supply voltage of digital CMOS circuits, their dynamic energy consumption decreases quadratically. Therefore, operating digital systems at ultra-low supply voltages can result in significant energy savings. However, ultra-low-voltage circuits pose many challenges as well. The current decreases exponentially, causing the delay to increase considerably. Hence, inherently, it is only possible to achieve low to moderate circuit performance. Circuits operating at such low supply voltages are much more sensitive to variations, which can severely compromise the yield. Moreover, the decreased current ratios pose a threat to reliable functionality of the circuits.

This book aims to design ultra-low-voltage digital circuits which are not only energy-efficient, but also provide answers to these various challenges. A focus is given toward designing variation-resilient circuits, as this is key to guarantee high yield. Additionally, operating frequencies of $n \times 10\,\text{MHz}$ are targeted to establish ultra-low-voltage systems as an attractive option for industrial applications.

To accomplish these various research aims, careful attention must be paid to all abstraction levels of digital design. Therefore, a complete design methodology is presented, which follows a bottom-up approach from transistor-level circuit design up to architecture-level recommendations. This ultra-low-voltage design strategy is generally applicable for all types of signal processing applications. This is demonstrated by four implemented prototypes: three datapath elements, i.e. a

logarithmic adder and two multiply accumulate units, and a full JPEG encoder in 90 nm and 40 nm CMOS technologies. These prototypes have successfully obtained the predefined research goals and have thereby succeeded to effectively validate the proposed design methodology.

Acronyms

BAN	Body area network
CDF	Cumulative distribution function
CEF	Constant electric field
CMOS	Complementary metal-oxide-semiconductor
CPL	Complementary pass transistor logic
CV	Constant voltage
DCT	Discrete cosine transform
DIBL	Drain-induced barrier lowering
DPG	Datapath generator
DSP	Digital signal processor
ECG	Electrocardiogram
ECRL	Efficient charge recovery logic
EDP	Energy-delay product
EOB	End-of-block
FBB	Forward body biasing
FFT	Fast fourier transform
FIR	Finite impulse response
FOM	Figure of merit
FSM	Finite state machine
HVT	High threshold voltage
INWE	Inverse narrow width effect
I/O	Input/output
JPEG	Joint photographic experts group
LVT	Low threshold voltage
MAC	Multiply-accumulate unit
MC	Monte carlo
MEP	Minimum-energy point

MSB	Most significant bit
NM	Noise margin
nMOS	n-channel MOS transistor
NOCG	Non-overlapping clock generator
PDF	Probability density function
PDN	Pull-down network
PDP	Power-delay product
PFAL	Positive feedback adiabatic logic
pMOS	p-channel MOS transistor
PTM	Predictive technology model
PUN	Pull-up network
RBB	Reverse body biasing
RFID	Radio-frequency identification
RSCE	Reverse short-channel effect
SAPTL	Sense amplifier-based pass transistor logic
SCE	Short-channel effect
SOI	Silicon-on-insulator
SRAM	Static random access memory
STSCL	Sub-threshold source-coupled logic
SVT	Standard threshold voltage
TG	Transmission gate
VTC	Voltage transfer characteristic
ZRL	Zero runlength

Symbols

A_{V_T}	Pelgrom coefficient of the threshold voltage
C	Capacitance
C_D	Depletion layer capacitance
C_ox	Gate oxide capacitance per unit area
E_dyn	Dynamic energy
E_stat	Static energy
E_tot	Total energy
f_clk	Clock frequency
F_v	Variation factor
I_0	Transistor current when $V_\mathrm{gs} = V_\mathrm{T}$
I_ds	Drain-source current of a transistor
I_leak	Leakage current
I_off	Off-current of a transistor
I_on	On-current of a transistor
k	Boltzmann constant ($= 1.380650524 \cdot 10^{-23}\mathrm{J/K}$)
K_i	Relative dielectric constant of a material i
L	Length of a transistor
n	Technology-dependent parameter
N_A	Doping concentration of the substrate
n_i	Intrinsic carrier concentration
$NM_\mathrm{L/H}$	Low / high noise margin
P_dyn	Dynamic power
P_stat	Static power
P_tot	Total power
q	Electric charge of an electron ($= 1.602176565 \cdot 10^{-19}\mathrm{C}$)

S_S	Sub-threshold slope
T	Absolute temperature
t_{clk}	Clock cycle
t_d	Gate delay
t_f	Fall time
t_{ox}	Oxide thickness
t_p	Propagation delay
t_{pHL}	High-to-low propagation delay
t_{pLH}	Low-to-high propagation delay
t_r	Rise time
V_{BB}	Body biasing voltage
V_{dd}	Supply voltage
$V_{dd,MEP}$	Supply voltage at which the MEP occurs
$V_{dd,min}$	Minimal supply voltage
$V_{dd,nom}$	Nominal supply voltage
V_{ds}	Drain-source voltage of a transistor
V_{dsat}	Saturation drain voltage of a transistor
V_{FB}	Flatband voltage
V_{gs}	Gate-source voltage of a transistor
V_{IH}	Minimum high input voltage of an inverter
V_{IL}	Maximum low input voltage of an inverter
V_{in}	Input voltage
V_M	Switching threshold voltage of an inverter
V_{OH}	Minimum high output voltage of an inverter
V_{OL}	Maximum low output voltage of an inverter
V_{out}	Output voltage
V_{sb}	Source-bulk voltage of a transistor
V_{ss}	Ground voltage
V_T	Threshold voltage of a transistor
V_{T0}	Threshold voltage for $V_{sb} = 0$
V_{th}	Thermal voltage
W	Width of a transistor

α	Activity factor
γ	Body effect coefficient
Δ	Delay
ϵ_0	Permittivity of free space ($= 8.854 \cdot 10^{-14}$F/cm)
ϵ_i	Permittivity of a material i
η	DIBL coefficient
λ	Channel length modulation coefficient

μ	Mobility of the charge carriers
μ_x	Mean value of x
σ_x	Standard deviation of x
ϕ_F	Fermi potential