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System Reduction for Nanoscale IC Design

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Preface

The ongoing miniaturization of devices like transistors used in integrated circuits (ICs) has led to feature sizes on the nanoscale. The Intel Core 2 (Yorkfield), first presented in 2007, was produced using 45 nm technology. Recently, production has reached 14 nm processes, e.g., in the Intel Broadwell, Skylake, and Kaby Lake microprocessors. Although the main principles in IC design and production are those of microelectronics, nowadays, one therefore speaks of *nanoelectronics*.

With miniaturization now reaching double-digit nanometer length scales and the huge number of semiconductor devices employed, which result in a correspondingly significant rise in integration density, the influence of the wiring and supply networks (interconnect and power grids) on the physical behavior of an IC can no longer be neglected and must be modeled with the help of dedicated network equations in the case of computer simulations. Furthermore, critical semiconductor devices can often no longer be modeled by substitute schematics as done in the past, using, e.g., the Partial Element Equivalent Circuit (PEEC) method. Instead, complex mathematical models are used, e.g., the drift-diffusion model. In addition to shortened production cycles, these developments in the design of new nanoelectronic ICs now increasingly pose challenges in computer simulations regarding the optimization and verification of layouts. Even in the development stage, it has become indispensable to test all crucial circuit properties numerically. Thus, the field of *computational nanoelectronics* has emerged.

The complexity of the mathematical models investigated in computational nanoelectronics is enormous: small parts of an IC design alone may require millions of linear and nonlinear differential-algebraic equations for accurate modeling, allowing the prediction of its behavior in practice. Thus, the full simulation of an IC design requires tremendous computational resources, which are often unavailable to microprocessor designers. In short, one could justifiably claim that *the performance of today's computers is too low to simulate their successors!*—a statement that has been true for the last few decades and is debatably still valid today. Thus, the dimension reduction of the mathematical systems involved has become crucial over the past two decades and is one of the key technologies in computational nanoelectronics.

The dimension or model reduction at the system level, or *system reduction* for short, is mostly done by mathematical algorithms, which produce a much smaller (often by factors of 100 up to 10,000) model that reproduces the system's response to a signal up to a prescribed level of accuracy. The topic of *system reduction in computational nanoelectronics* is the focus of this book. The articles gathered here are based on the final reports for the network *System Reduction in Nanoscale IC Design (SyreNe)*, supported by Germany's Federal Ministry of Education and Research (BMBF) as part of its Mathematics for Innovations in Industry and Services program. It was funded between July 1, 2007, and December 31, 2010 (see syrene.org for a detailed description) and continued under the name *Model Reduction for Fast Simulation of new Semiconductor Structures for Nanotechnology and Microsystems Technology* (*MoreSim4Nano*) within the same BMBF funding scheme from October 1, 2010, until March 31, 2014 (see moresim4nano.org).

The goal of both research networks was to develop and compare methods for system reduction in the design of high-dimensional nanoelectronic ICs and to test the resulting mathematical algorithms in the process chain of actual semiconductor development at industrial partners. Generally speaking, two complementary approaches were pursued: the reduction of the nanoelectronic system as a whole (subcircuit model coupled to device equation) by means of a global method and the creation of reduced order models for individual devices and large linear subcircuits which are linked to a single reduced system. New methods for nonlinear model reduction and for the reduction of power grid models were developed to achieve this.

The book consists of five chapters, introducing novel concepts for the different aspects of model reduction of circuit and device models. These include:

- Model reduction for device models coupled to circuit equations in Chap. 1 by Hinze, Kunkel, Matthes, and Vierling
- Structure-exploiting model reduction for linear and nonlinear differential-algebraic equations arising in circuit simulation in Chap. 2 by Stykel and Steinbrecher
- The reduced representation of power grid models in Chap. 3 by Benner and Schneider
- Numeric-symbolic reduction methods for generating parameterized models of nanoelectronic systems in Chap. 4 by Schmidt, Hauser, and Lang
- Dedicated solvers for the generalized Lyapunov equations arising in balanced truncation based model reduction methods for circuit equations in Chap. 5 by Bollhöfer and Eppler

The individual chapters describe the new algorithmic developments in the respective research areas over the course of the project. They can be read independently of each other and provide a tutorial perspective on the respective aspects of System Reduction in Nanoscale IC Design related to the sub-projects within SyreNe. The aim is to comprehensively summarize the latest research results, mostly published in dedicated journal articles, and to present a number of new aspects never before

published. The chapters can serve as reference works, but should also inspire future research in computational nanoelectronics.

I would like to take this opportunity to express my gratitude to the project partners Matthias Bollhöfer and Heike Faßbender (both from the TU Braunschweig), Michael Hinze (University of Hamburg), Patrick Lang (formerly the Fraunhofer-Institut für Techno- und Wirtschaftsmathematik (ITWM), Kaiserslautern), Tatjana Stykel (at the TU Berlin during the project and now at the University of Augsburg), Carsten Neff (NEC Europe Ltd. back then), Carsten Hammer (formerly Qimonda AG and then Infineon Technologies AG), and Peter Rotter (Infineon Technologies AG back then). Only their cooperation within SyreNe and their valued work in the various projects made this book possible.

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Magdeburg, Germany Peter Benner
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