

# Sustained Simulation Performance 2013



Michael M. Resch • Wolfgang Bez • Erich Focht  
Hiroaki Kobayashi • Yevgeniya Kovalenko  
Editors

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*Front cover figure:* Volume renderings of a human Femur, a femoral head and cubes of cancellous bone micro structure with 1.2mm edge length. The cubes are used as base data to derive continuum mechanical material properties via direct numerical simulation. Illustration by Ralf Schneider, High Performance Computing Center Stuttgart, Stuttgart, Germany

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# Preface

The field of high-performance computing is currently witnessing a significant shift of paradigm. Ever larger raw number crunching capabilities of modern processors are in principle available to computational scientist. However, efficiently exploiting modern processors is getting more and more complex; this is particularly true for so-called accelerators as GPGPUs or many-cores as the MIC architecture. (GPGPU, many-cores, and MIC are very common technical terms which are not introduced in the preface, but in the later chapters).

On the other hand, many areas of computational science have reached a saturation in terms of problem size. Scientists often do no longer wish to solve larger problems. Instead they wish to solve smaller problems in a shorter time. The current architectures, however, are much more efficient for large problems than they are for the more relevant smaller problems.

This series of workshops focuses on *sustained simulation performance*, i.e., high-performance computing for real application use cases, rather than on peak performance, which is the scope of artificial benchmarks. The series was established in 2004, initially named Teraflop Workshop, and renamed to Workshop on Sustained Simulation Performance in 2012. In general terms, the scope of the workshop series has focussed on issues related to achieving high sustained performance on all kinds of architectures – from vector systems, to accelerator-based architectures, to clusters and state-of-the-art MPP systems. Special emphasis is given to programmer productivity in the setting of current and future trends in hardware and software developments.

This book presents the results of the 16th and 17th installment of the series. The 16th workshop was held at the High-Performance Computing Center, Stuttgart, Germany, in December 2012. The 17th workshop was held in March 2013 at the headquarters of NEC Corporation in Tokyo, Japan, and organized jointly with the University of Tohoku, Sendai, Japan.

The topics studied by the contributed papers include analysis and extrapolations of performance and energy efficiency of modern hardware architectures (Part I), frameworks and libraries aiming at increasing programmer productivity on future systems (Part II), and application use-cases studies (Part III).

We would like to thank all the contributors of this book and the Sustained Simulation Performance project. We thank especially Prof. Hiroaki Kobayashi for the close collaboration over the past years and are looking forward to intensify our cooperation in the future.

Stuttgart, Germany  
July 2013

José Gracia  
Michael Resch

# Contents

## Part I Challenges of Modern HPC Systems: Performance and Energy Efficiency Analysis

|  |    |
|--|----|
| <b>Feasibility Study of Future HPC Systems for Memory-Intensive Applications</b> .....         | 3  |
| Hiroaki Kobayashi  |    |
| 1 Introduction .....   | 3  |
| 2 Design Concept of the Target System .....  | 4  |
| 3 Summary .....  | 10 |
| References .....   | 11 |
| <b>Analysing the Performance Improvements of Optimizations on Modern HPC Systems</b> .....     | 13 |
| Kazuhiko Komatsu, Toshihide Sasaki, Ryusuke Egawa,<br>Hiroyuki Takizawa, and Hiroaki Kobayashi |    |
| 1 Introduction .....   | 14 |
| 2 Performance Differences Among Multiple Modern HPC Systems .....                              | 15 |
| 3 Optimization Methods Widely Used in HPC Codes .....  | 16 |
| 3.1 Uses of Temporal Variables .....   | 16 |
| 3.2 Loop Distribution .....  | 17 |
| 3.3 Loop Unswitching .....   | 17 |
| 3.4 Loop-Invariant Code Motion .....   | 17 |
| 3.5 Loop Collapsing .....  | 17 |
| 3.6 Loop Exchange .....  | 18 |
| 3.7 Uses of Mask Operations .....  | 18 |
| 3.8 Loop Unrolling .....   | 18 |
| 4 Performances of Optimizations on Multiple HPC Systems .....                                  | 18 |
| 4.1 Experimental Environments .....  | 18 |
| 4.2 Performance Improvement of Optimizations<br>among Multiple HPC Systems .....               | 19 |
| 4.3 Analysis of Combination of Optimizations .....   | 22 |

|     |   |    |
|-----|---|----|
| 5   | Conclusions .....   | 24 |
|     | References .....  | 24 |
|     | <b>Power Consumption of Kernel Operations</b> .....               | 27 |
|     | Dmitry Khabi and Uwe Küster                                       |    |
| 1   | Introduction .....  | 27 |
| 1.1 | Power Consumption of Computational Node .....                     | 27 |
| 1.2 | Power Measurement .....   | 28 |
| 1.3 | Kernel Operations .....   | 30 |
| 1.4 | Virtual CPU Frequency .....                                       | 31 |
| 2   | Electric Power of Processor (Watt, GHz) .....                     | 32 |
| 2.1 | Power Approximation .....   | 32 |
| 2.2 | Power of Kernel Operations .....                                  | 33 |
| 3   | Performance of Processor (Elements per Second, GHz) .....         | 35 |
| 3.1 | Performance of Kernel Operations .....                            | 35 |
| 3.2 | Performance Approximation .....                                   | 37 |
| 4   | Energy Consumption of Kernel Operations (Joule per Element) ..... | 39 |
| 4.1 | Dependencies of Energy and Performance .....                      | 39 |
| 4.2 | Compare Kernel Operations .....                                   | 42 |
| 5   | Outlook .....   | 42 |
|     | References .....  | 45 |

## **Part II Frameworks and Libraries for Simulations on New-Generation Computing Systems**

|     |   |    |
|-----|---|----|
|     | <b>Lattice Boltzmann Simulations on Complex Geometries</b> .....                  | 49 |
|     | Simon Zimny, Kannan Masilamani, Kartik Jain, and Sabine Roller                    |    |
| 1   | Introduction .....  | 50 |
| 2   | The Lattice Boltzmann Method .....  | 50 |
| 3   | Musubi as Part of the APES Framework .....  | 51 |
| 4   | Applications on Complex Geometries .....  | 53 |
| 4.1 | Thrombus Formation in Cerebral Aneurysms .....                                    | 53 |
| 4.2 | Spacer Filled Flow Channel in Electrodialysis .....                               | 56 |
| 5   | Scalability and Parallel Efficiency of Fluid Flows<br>in Complex Geometries ..... | 58 |
| 6   | Conclusion and Outlook .....  | 61 |
|     | References .....  | 61 |

## **IMD: A Typical Massively Parallel Molecular Dynamics Code for Classical Simulations – Structure, Applications,**

|     |  |    |
|-----|--|----|
|     | <b>Latest Developments</b> .....               | 63 |
|     | Johannes Roth                                  |    |
| 1   | Introduction .....                             | 63 |
| 2   | Classical Molecular Dynamics Simulations ..... | 64 |
| 2.1 | The Molecular Dynamics Steps .....             | 64 |



|     |  |     |
|-----|--|-----|
| 3   | Realistic Interactions and <i>potfit</i> .....   | 69  |
| 3.1 | Long-Range Interactions.....   | 70  |
| 4   | Some Examples of Recent Simulations .....  | 70  |
| 5   | Parallelization .....  | 71  |
| 6   | Benchmarking IMD .....   | 72  |
| 7   | Porting IMD to GPUs .....  | 72  |
| 8   | A Comment on World Records Molecular Dynamics Simulations .....  | 74  |
| 9   | Summary.....   | 74  |
|     | References .....   | 75  |
|     | <b>Evaluation of FastFlow Technology for Real-World Application</b> .....  | 77  |
|     | Kamran Idrees, Mathias Nachtmann, and Colin W. Glass   |     |
| 1   | Introduction.....  | 77  |
| 2   | Algorithms.....  | 78  |
| 2.1 | BasicN2 Algorithm .....  | 78  |
| 2.2 | MoleculeBlocks Algorithm.....  | 78  |
| 3   | Porting CMD to FastFlow .....  | 79  |
| 3.1 | Parallelization of BasicN2 Algorithm.....  | 79  |
| 3.2 | Parallelization of MoleculeBlocks Algorithm .....  | 80  |
| 4   | Evaluation .....   | 83  |
| 4.1 | Evaluation Metrics .....   | 83  |
| 4.2 | Results .....  | 83  |
| 5   | Conclusions.....   | 87  |
|     | References .....   | 88  |
|     | <b>Storage and Indexing of Fine Grain, Large Scale Data Sets</b> .....   | 89  |
|     | Ralf Schneider   |     |
| 1   | Introduction.....  | 89  |
| 1.1 | Description of Use Case .....  | 90  |
| 1.2 | Data Amount, File Numbers and Sizes .....  | 92  |
| 1.3 | Serial Applications and Fine Grain Data Sets .....   | 93  |
| 2   | From the Reduction of Input/Output Operations Per Second<br>(IOPS) Towards a Storage and Indexing Concept for Fine<br>Grained, Large Scale Data Sets ..... | 94  |
| 2.1 | Data Storage Concept.....  | 94  |
| 2.2 | Data Indexing Concept .....  | 95  |
| 2.3 | Implementation.....  | 96  |
| 3   | Implementation of a Parallel Indexing and Packaging<br>Algorithm by Means of the Proposed Concept .....  | 98  |
| 4   | Application Results .....  | 100 |
| 5   | Summary and Outlook .....  | 102 |
|     | References .....   | 103 |

### **Part III Computational Engineering Applications and Multi-Physics Simulations**

|  |            |
|--|------------|
| <b>Direct Numerical Simulations of Film Cooling in a Supersonic Boundary-Layer Flow on Massively-Parallel Supercomputers .....</b> | <b>107</b> |
| Michael Keller and Markus J. Kloker  |            |
| 1 Introduction .....   | 107        |
| 2 Numerical Method .....   | 109        |
| 2.1 Governing Equations .....  | 109        |
| 2.2 Spatial Discretization and Time Integration .....  | 110        |
| 2.3 Computational Domain, Boundary Conditions<br>and Initial Condition .....   | 116        |
| 2.4 Parallelization .....  | 118        |
| 3 Numerical Results .....  | 119        |
| 4 Conclusions and Outlook .....  | 126        |
| References .....   | 127        |
| <b>Large Scale Numerics Uncovering New States of Matter .....</b>  | <b>129</b> |
| A. Moreno, J.M.P. Carmelo, and A. Muramatsu  |            |
| 1 Introduction .....   | 130        |
| 2 Model and Algorithms .....   | 131        |
| 3 Results .....  | 131        |
| References .....   | 136        |
| <b>Towards Simulation of Electrolytic Sea Water Desalination .....</b>   | <b>137</b> |
| Kannan Masilamani, Jens Zudrop, and Sabine Roller  |            |
| 1 Introduction .....   | 137        |
| 2 Liquid Mixture Modelling .....   | 140        |
| 2.1 Lattice Boltzmann Mixture Modelling .....  | 140        |
| 3 Octree Based Simulations .....   | 142        |
| 4 Performance and Applications .....   | 143        |
| 5 Conclusion and Outlook .....   | 146        |
| References .....   | 146        |
| <b>A Regional Climate Model Simulation for EURO-CORDEX<br/>with the WRF Model .....</b>  | <b>147</b> |
| Kirsten Warrach-Sagi, Thomas Schwitalla, Hans-Stefan Bauer,<br>and Volker-Wulfmeyer  |            |
| 1 Introduction .....   | 147        |
| 2 Simulation with WRF-3.1.0 on the NEC Nehalem Cluster .....   | 149        |
| 3 Simulation with WRF-3.3.1 on the CRAY X6 .....   | 150        |
| 4 Results .....  | 151        |
| 5 Conclusion .....   | 153        |
| References .....   | 155        |