Wafer-Level Chip-Scale Packaging

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Analog and Power Semiconductor Applications

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ISBN 978-1-4939-1555-2 ISBN 978-1-4939-1556-9 (eBook)
DOI 10.1007/978-1-4939-1556-9
Springer New York Heidelberg Dordrecht London

Library of Congress Control Number: 2014946821

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Printed on acid-free paper

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Preface

A wafer-level chip-scale package (WLCSP) is a bare die package that offers not only the smallest possible footprints in all IC package forms, but also superior electrical and thermal performance, mostly credited to the direct solder interconnections that are low in electrical and thermal resistance and low in inductance between chip and application PCB it is assembled on. For mobile electronics, where performance needs to be high and size must be small, heat dissipation is limited to the conduction through PCB to the case of the mobile device; WLCSP is the best chip package option that balances the seemingly conflicting requirements.

Sharing the same root with the flip chip package, WLCSP took a bold step forward by placing sufficient size solder bumps on a semiconductor chip and allowing it to be flip mounted directly on an application board. With solder joints taking up a significant portion of chip/PCB CTE mismatching thermal/mechanical stresses, WLCSP has proved to be reliable in mobile-specific reliability tests, such as drop test, bending test, and temperature cycling tests, besides the basic device-specific reliability tests. The robustness of this packaging form is also demonstrated with lasting life of everyday use on billions of mobile consumer electronics devices. With continuous evolvement in the bumping technologies, such as polymer re-passivated bump on pad (BoP), copper redistribution layer (RDL), front side molded copper post on the RDL, aggressive silicon back grinding, advanced solder alloys, and design know-how, WLCSP has expanded the size range from early days under 2–3 mm to 8–10 mm silicon chip size, while at the same time continuously reducing the per unit cost with scaling factors of high volume production in 200 and 300 mm wafer sizes. The availability of package size range and favorable cost structure makes WLCSP a good packaging candidate for a wide array of semiconductor devices, from analog/mixed signal and wireless connectivity chips to optoelectronics, power electronics, and logic and memory chips. Innovations in wafer-level 3D chip stacking further enable WLCSP a viable option for MEMS and sensor chip packaging.

The beauty of WLCSP is the start-to-finish wafer-based processing. It blurs the line between semiconductor wafer fab processes and the backend packaging operations. There is no singulated die packaging operation typically seen in all other types of chip packaging operations. WLCSP packaging operations, including bumping, inspections, and tests, are fully automated from cassette to cassette,

which is known for high efficiency. Also benefiting from half a century of wafer processing know-how is the overall WLCSP packaging (often referred as bumping) yield, which is quite close to 100%. With this in mind, it is not a surprise at all to see even for die fan-out packages, wafer form processing, based on the reconstituted wafers in 200 or 300 mm size, is the preferred approach from start.

WLCSP has appreciated enormous growth in the past decade, largely because of global consumer demand for mobile communication and computing devices. With double-digit market value (wafer bumping, test, and die processing service including back grind, marking, saw, and tape and reel) growth still in sight, WLCSP is one of the most important packaging technologies for packaging engineers of all backgrounds.

It is the purpose of this book to provide readers a comprehensive overview of the general WLCSP packaging technology. It is also the intention of the authors to share specific knowledge of WLCSP in analog and power semiconductors. Advanced WLCSP technologies, such as 3D wafer-level stacking, TSV, MEMS, and opto-electronics applications, are also briefly introduced in this book.

The book consists of ten chapters, with an overview of the demand and challenges for analog and power WLCSP in Chap. 1; Chaps. 2 and 3 cover the basic concepts of fan-in and fan-out WLCSP, bumping process flow, design considerations, and reliability assessment. Chapter 4 is designated for the stackable packaging solutions involving WLCSP. Chapter 5 gets into the details of wafer-level discrete power MOSFET package design considerations. Chapter 6 discusses more on TSV/stack die WLCSP for the integration of analog and power solution. Chapter 7 is all on the critical topics of thermal management, design, and analysis for WLCSP. Chapter 8 continues on the electrical and multiple physics simulation for analog and power WLCSP, with the new progress on electromigraton study of 0.18 μm power technology. Chapter 9 touches on the assembly of WLCSP devices. Chapter 10 wraps up the book with reliability and general testing of WLCSP semiconductors.

Coming up with years of experience in semiconductor packaging, and with focus on wafer-level packaging, the authors attempted to provide well-balanced and yet up-to-date content in ten chapters. We wish this book is a good starting material for young engineers who need to learn the most important of WLCSP technology in a short time. At the same time, we also hope that seasoned engineers find this book good references for them to not only keep up with the rapid technology advancement, but also to help address daily engineering challenges.

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Acknowledgments

The book is impossible without the dedication of Merry Stuber, editor from Springer for timely reminder and coordination of draft submission and critical reviews. Doug Dolan from Fairchild Semiconductor deserves special thanks for taking time performing the primary legal review of all ten chapters. The authors would also like to thank Fairchild Semiconductor for general support of technical publications that led directly to the completion of this book. A few names are mentioned here for the support over the years, Suresh Belani, director for packaging, OS Jeon, senior director for packaging, Dan Kinzer, former chief technology officer, and Paul Hughes, general consults, all from Fairchild. Many coworkers contributed to the data quoted in this book and the author like to take this opportunity to express our sincere thanks as well: Mr. Richard Qian, Mr. Zhongfa Yuan, and Dr. Yumin Liu for simulation support; Dr. Qi Wang for wafer-level power MOSFET and process; Dr. Jun Cai (former Device and Process Senior Member of Technical Staff) and Mr. Andrew Schoenberger (former Fairchild wafer-level process engineer) for the WLCSP ball shearing test; Dr. Yangjian Xu, Mr. Ye Zhang, and Huixian Wu (Zhejiang University of Technology) for the WLCSP ball shearing test and stacking simulations; Dr. Jifa Hao for the wafer-level electromigration test of 0.18 μm power interconnects; Dr. Yuanxiang Zhang (Quzhou University) for building the wafer-level electromigration model; Ms. Jiamin Ni and Professor Antoinette Maniatty (Rensselaer Polytechnic Institute) for solder joint electromigration; Etan Schaham for inspiring discussions of WLCSP packaging challenges; Rob Travis and Dennis Tummy for insights of device reliability and fab process interactions; Mr. Doug Hawks (former Fairchild packaging engineer) for MCSP development; Mr. William Newberry for electrical simulation methodology; Jihwan Kim for the WLCSP drop test; and Steve Martin for support for routine WLCSP research and development activities. Several organizations within Fairchild are also mentioned here for the support WLCSP assembly and tests: Fairchild Bucheon site and Fairchild Cebu site.

Much of the material in this book was derived from previous papers and research notes by the authors. Here the authors like to thank several professional societies that published some of this material and allowed to reproduce some contents in this

book. They are the Institute of Electrical and Electronic Engineers (IEEE) and its Conferences, Proceedings, and Journals, including IEEE Transactions on Components and Packaging Technology and IEEE Transactions on Electronics Packaging Manufacturing. The authors also appreciate the following Conferences for allowing the reorganization and reproduction of previously published materials: IEEE Electronic Components and Technology Conference (ECTC), IEEE International Conference on Electronic Packaging Technology and High Density Packaging (ICEPT-HDP), and IEEE International Conference on Thermal, Mechanical and Mult-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE).

Lastly, but most importantly, the authors would like to thank their perspective families for the support that made it possible to spend numerous weekends and nights on this book. Shichun Qu likes to thank his wife Shan Huang and daughter Claire Qu, and Yong Liu likes to express his appreciation to his wife, Jane Chen, and sons Junyang Liu and Alexander Liu for their great love and patience throughout the 2+ years of writing this book.

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Biography

Shichun Qu started his career in research and development of PTFE-based IC low K dielectric materials at W. L. Gore & Associates' Eau Claire, Wisconsin R&D facility, after receiving a Ph.D. degree in Materials Science and Engineering from SUNY at Stony Brook. Post the 3 M acquisition of the Gore & Associates' IC substrate business, also located in Eau Claire, Wisconsin, he continued working on the manufacturing technology development of organic flip chip/BGA and wire bond/BGA substrates. In the meantime, he was also the lead engineer in the development of high-speed organic substrate dielectric materials: from materials formulation, coating and substrate manufacturing processes development and qualifications to the flip chip assembly process development. The latter work resulted in a very early industrial publication on the management of the flip chip substrate warpage through a differential heating reflow process back in 2003. Shichun Qu joined National semiconductor in Santa Clara, California, in 2007. There he was involved in the development of advanced lead frame package, high-temperature wire bond over pad metallization research and production qualification, and high pin count WLCSP technology research. After joining Fairchild Semiconductor in 2011, he has dedicated most of the time understanding the WLCSP chip/PCB interactions and fine-tuning WLCSP design and bumping process to achieve competitive manufacturing cost by extending the use of low mask count bumping technologies at higher pin count. Besides conventional WLCSP, Shichun Qu also played technical roles in various types of embedded WLCSP power module designs, test, and qualifications.

Besides a Ph.D. in Materials Science and Engineering, Shichun Qu also received a Master of Engineering and Bachelor of Science degree in Engineering Mechanics from Tsinghua University (Beijing, China). He was an assistant professor for four and a half years at the University of Petroleum (Beijing, China) before returning to school for the Ph.D. degree at SUNY Stony Brook and new careers in the USA.

Besides tackling engineering challenges, Shichun Qu enjoys other types of physical challenges. He finished his first half marathon (San Jose Rock n Roll) in 2013 and is eying on full marathon in the next few years. When not practicing long-distance running, he enjoys the time with his wife and daughter and sometimes hiking and biking as a family.

About the Author

Yong Liu has been with Fairchild Semiconductor Corp in South Portland, Maine, since 2001 as a Senior Member Technical Staff from 2008, a Member Technical Staff from 2004 to 2007, and a Principal Engineer from 2001 to 2004. He is now a Fairchild global team leader of electrical, thermal-mechanical modeling and analysis. His main interest area is advanced analog and power electronic packaging, modeling and simulation, reliability, and assembly process. In last a few years he and his team have been working on advanced IC packaging and power modules, modeling and simulation, including the pioneering work on assembly manufacture process, reliability analysis, and the electromigration-induced failures in chip-scale wafer-level packages. He has been invited to give keynote talks and presentations at international conferences Eurosime, ICEPT, EPTC, and universities in the USA, Europe, and China. He has coauthored over 170 papers in journals and conferences and has been granted over 45 US patents in the area of 3D/Stack/TSV IC and power electronic packaging. Dr. Liu obtained his BS, Master, and Ph.D. degrees in Nanjing Univeristy of Science and Technology in 1983, 1987, and 1990, respectively. He once was promoted by breaking rule as a full professor at Zhejiang University of Technology in 1994. Dr. Liu was awarded Alexander von Humboldt Fellowship and studied as a Humboldt fellow at Tech University of Braunschweig, Germany, in 1995. In 1997, he was awarded Alexander von Humboldt European Fellowship and studied as a Humboldt European fellow at University of Cambridge, England. In 1998, he worked as a post-doctor at Semiconductor Focus Center and Computational Mechanics Center, Rensselaer Polytechnic Institute (RPI). In 2000, he worked as a staff opto package engineer at Nortel Networks at Boston. Since he joined Fairchild in 2001, he was awarded the first Fairchild President Award in 2008, Fairchild Key Technologist in 2006 and 2009, Fairchild BIQ award in product innovation in 2005, and Fairchild award for power of pen first place in 2004, IEEE CPMT Exceptional Technical Achievement Award in 2013.