ASSESSING FAULT MODEL AND TEST QUALITY

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Printed on acid-free paper.

To Stephanie, Billene, Rebecca, Elizabeth, and our parents.

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Preface

For many years, the dominant fault model in automatic test pattern generation (ATPG) for digital integrated circuits has been the stuck-at fault model. The static nature of stuck-at fault testing when compared to the extremely dynamic nature of integrated circuit (IC) technology has caused many to question whether or not stuck-at fault based testing is still viable. Attempts at answering this question have not been wholly satisfying due to a lack of true quantification, statistical significance, and/or high computational expense. In this monograph we introduce a methodology to address the question in a manner which circumvents the drawbacks of previous approaches.

The method is based on symbolic Boolean functional analyses using Ordered Binary Decision Diagrams (OBDDs). OBDDs have been conjectured to be an attractive representation form for Boolean functions, although cases exist for which their complexity is guaranteed to grow exponentially with input cardinality. Classes of Boolean functions which exploit the efficiencies inherent in OBDDs to a very great extent are examined in Chapter 7. Exact equations giving their OBDD sizes are derived, whereas until very recently only size bounds have been available. These size equations suggest that straightforward applications of OBDDs to design and test related problems may not prove as fruitful as was once thought.

A new functional test generation scheme utilizing OBDDs called Difference Propagation is introduced in Chapter 8. Difference Propagation enables the generation of complete test sets more efficiently than is possible with conventional test generation tools. Furthermore, it has the capacity of addressing a wider array of logical models than simply the single stuck-at fault. The application of Difference Propagation to selected fault sets and benchmark circuits has provided insights into fault model behavior. Clues are revealed as to how to best enhance fault detection using design for testability techniques.

A novel probabilistic model expressing the essential behavior of ATPG has also been developed. The model is used in conjunction with the test set information derived previously to help predict the trends of stuck-at testing

with increasing circuit complexity. The results, which are detailed in Chapter 11, seem to indicate that traditional stuck-at testing methods will, below some defect level, fail to provide acceptable IC quality.

The bulk of the new material presented in this monograph comprised part of the first author's PhD research at the University of Texas at Austin. The authors gratefully acknowledge the support of this research by the Semiconductor Research Corporation under Contract #91-DP-142, by the National Science Foundation under Grant MIP-8552537, by the Innovative Science and Technology Office of the Strategic Defense Initiative Organization, administered through the Office of Naval Research under Contract N00014-86-K-0554, by the Texas Advanced Technology Program – Project No. 003658-541, and by a Departmental Grant from IBM Corporation.

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