Simultaneous Switching Noise of CMOS Devices and Systems

**THE KLUWER INTERNATIONAL SERIES
IN ENGINEERING AND COMPUTER SCIENCE**

ELECTRONIC PACKAGING AND INTERCONNECTS

Consulting Editor

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Simultaneous Switching Noise of CMOS Devices and Systems

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SPRINGER SCIENCE+BUSINESS MEDIA, LLC

Library of Congress Cataloging-in-Publication Data

Senthinathan, Ramesh, 1961 -

Simultaneous switching noise of CMOS devices and systems / by
Ramesh Senthinathan, John L. Prince.

p. cm. -- (The Kluwer international series in engineering and
computer science. Electronic packaging and interconnects)

Includes bibliographical references (p.) and index.

ISBN 978-0-7923-9400-6 ISBN 978-1-4615-3204-0 (eBook)

DOI 10.1007/978-1-4615-3204-0

1. Metal oxide semiconductors--Design and construction.
2. Electronic circuits--Noise. I. Prince, John L., 1941 - .
- II. Title. III. Series.

TK7871.99.M44S5 1994

621.3815--dc20

93-32572

CIP

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Originally published by Kluwer Academic Publishers in 1994

Softcover reprint of the hardcover 1st edition 1994

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This book is dedicated to the
Center for Electronic Packaging Research (CEPR),
Department of Electrical and Computer Engineering at the
University of Arizona,
Tucson, Arizona.

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PREFACE

This monograph presents our recent research on Simultaneous Switching Noise (SSN) and related issues for CMOS based systems. Although some SSN related work was previously reported in the literature, it were mainly for Emitter Coupled Logic (ECL) gates using Bipolar Junction Transistors (BJTs). This present work covers in-depth analysis on estimating SSN and its impact for CMOS based devices and systems. At present semiconductor industries are moving towards scaled CMOS devices and reduced supply voltage. SSN together with coupled noise may limit the packing density, and thereby the frequency of operation of packaged systems. Our goal is to provide efficient and yet reliable methodologies and algorithms to estimate the overall noise containment in single chip and multi-chip package assemblies.

We hope that the techniques and results described in this book will be useful as guides for design, package, and system engineers and academia working in this area. Through this monograph, we hope that we have shown the necessity of interactions that are essential between chip design, system design and package design engineers to design and manufacture optimal packaged systems.

Work reported in this monograph was partially supported by the grant from Semiconductor Research Corporation (SRC Contract No. 92-MP-086).

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ACKNOWLEDGMENTS

Our most sincere thanks to Prof. Andreas C. Cangellaris for his valuable advice, comments and suggestions. We also thank Professors Olgierd Palusinski, Michael Scheinfein, Douglas Hamilton, and Ronald Schrimpf for their help and advice in many areas. Thanks to Semiconductor Research Corporation (SRC) for their support for this work.

We thank many of our SRC member company mentors for their guidance in steering this research work. The authors are thankful to many students and faculty in the electrical and computer engineering department and Professors M. Scadron, J. Leavitt, S. Koch and C. Falco in the physics and optical sciences department at the University of Arizona for their constructive criticism and advice. We thank Arun Vaidyanath for his help in formatting this monograph. Authors acknowledge Srinivas Nimmagadda for his help on several SPICE simulations. We thank our CEPR administrative advisor Kristin Kreamer for her help.

Ramesh Senthinathan is very thankful to many members from APDC Motorola, especially his managers Mali Mahalingam, Kent Hansen and Barry Johnson for their encouragement. Ramesh thanks his previous manager George Katopis (IBM) for his encouragement. He is also thankful to IBM (Fishkill, New York) and Intel (Chandler, Arizona) corporations for very valuable experience. Thanks to IBM (Yorktown), Hestia (Sunnyvale), GTE (Phoenix), and Honeywell (Minnesota) corporations for valuable summer intern experience.

At Kluwer Academic Publishers, we wish to acknowledge Ken Tennity who encouraged us to undertake this project. A very special thanks to our wives Logini and Martha for their patience, support, and encouragement.

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