DIGITAL BiCMOS INTEGRATED CIRCUIT DESIGN

THE KLUWER INTERNATIONAL SERIES IN ENGINEERING AND COMPUTER SCIENCE

VLSI, COMPUTER ARCHITECTURE AND DIGITAL SIGNAL PROCESSING

Consulting Editor
Jonathan Allen

Latest Titles

- Neural Models and Algorithms for Digital Testing*, S. T. Chakradhar,
V. D. Agrawal, M. L. Bushnell,
ISBN: 0-7923-9165-9
- Monte Carlo Device Simulation: Full Band and Beyond*, Karl Hess, editor
ISBN: 0-7923-9172-1
- The Design of Communicating Systems: A System Engineering Approach*,
C. J. Koomey
ISBN: 0-7923-9203-5
- Parallel Algorithms and Architectures for DSP Applications*,
M. A. Bayoumi, editor
ISBN: 0-7923-9209-4
- Digital Speech Processing: Speech Coding, Synthesis and Recognition*
A. Nejat Ince, editor
ISBN: 0-7923-9220-5
- Sequential Logic Synthesis*, P. Ashar, S. Devadas, A. R. Newton
ISBN: 0-7923-9187-X
- Sequential Logic Testing and Verification*, A. Ghosh, S. Devadas, A. R. Newton
ISBN: 0-7923-9188-8
- Introduction to the Design of Transconductor-Capacitor Filters*,
J. E. Kardontchik
ISBN: 0-7923-9195-0
- The Synthesis Approach to Digital System Design*, P. Michel, U. Lauther, P. Duzy
ISBN: 0-7923-9199-3
- Fault Covering Problems in Reconfigurable VLSI Systems*, R. Libeskind-Hadas,
N. Hassan, J. Cong, P. McKinley, C. L. Liu
ISBN: 0-7923-9231-0
- High Level Synthesis of ASICs Under Timing and Synchronization Constraints*
D.C. Ku, G. De Micheli
ISBN: 0-7923-9244-2
- The SECD Microprocessor, A Verification Case Study*, B.T. Graham
ISBN: 0-7923-9245-0
- Field-Programmable Gate Arrays*, S.D. Brown, R. J. Francis, J. Rose,
Z.G. Vranesic
ISBN: 0-7923-9248-5
- Anatomy of A Silicon Compiler*, R.W. Brodersen
ISBN: 0-7923-9249-3
- Electronic CAD Frameworks*, T.J. Barnes, D. Harrison, A.R. Newton,
R.L. Spickelmier
ISBN: 0-7923-9252-3
- VHDL for Simulation, Synthesis and Formal Proofs of Hardware*, J. Mermet
ISBN: 0-7923-9253-1
- Wavelet Theory and its Applications*, R. K. Young
ISBN: 0-7923-9271-X

DIGITAL BiCMOS INTEGRATED CIRCUIT DESIGN

by

Sherif H.K. Embabi
Texas A & M University

Abdellatif Bellaouar
University of Waterloo

Mohamed I. Elmasry
University of Waterloo

Springer Science+Business Media, LLC

Library of Congress Cataloging-in-Publication Data

Embabi, S. H. K. (Sherif H. K.)

Digital BiCMOS integrated circuit design / by S.H.K. Embabi, A.
Bellaour, M.I. Elmasry.

p. cm. -- (Kluwer international series in engineering and
computer science)

Includes bibliographical references and index.

ISBN 978-1-4613-6391-0 ISBN 978-1-4615-3174-6 (eBook)

DOI 10.1007/978-1-4615-3174-6

1. Digital integrated circuits--Design and construction. 2. Metal
oxide semiconductors, Complementary. 3. Bipolar integrated
circuits. I. Bellaouar, A. II. Elmasry, Mohamed I., 1943-
III. Title. IV. Series.

TK7874.E52 1993

621.3815--dc20

92-29636

CIP

Copyright © 1993 by Springer Science+Business Media New York
Originally published by Kluwer Academic Publishers in 1993
Softcover reprint of the hardcover 1st edition 1993

All rights reserved. No part of this publication may be reproduced, stored in a retrieval system or transmitted in any form or by any means, mechanical, photo-copying, recording, or otherwise, without the prior written permission of the publisher, Springer Science+Business Media, LLC.

Printed on acid-free paper.

To

Afaf, Hassan, Dina, Ahmed, and Aya Embabi

Mohamed and Massaouda Bellaouar

Elizabeth, Carmen, Samir, Nadia, and Hassan Elmasry

Table of Contents

Preface	xiii
Acknowledgments	xv
List of Symbols	xvi
Chapter 1. Introduction	1
1.1. Why BiCMOS ?	1
1.2. This Book	4
1.3. Process Technology	5
1.4. Device Design Considerations	6
1.5. Device Modeling	7
1.6. MOS Digital Integrated Circuits	7
1.7. Bipolar CML Integrated Circuits	8
1.8. BiCMOS Digital Integrated Circuits	8
1.9. BiCMOS Digital Circuit Applications	9
References	9
.....	
Chapter 2. Process Technology	11
2.1. CMOS Process Technology	11
2.1.1. N-well CMOS Process	12
2.1.2. Twin-Tub CMOS Process	14
2.2. Bipolar Process Technology	16
2.3. Isolation in CMOS and Bipolar Technologies	23
2.3.1. CMOS Device Isolation Techniques	23
2.3.2. Bipolar Device Isolation Techniques	28
2.4. CMOS and Bipolar Process Convergence	31
2.5. BiCMOS Technology	32
2.5.1. Example 1: Low-Cost BiCMOS Process	32

2.5.2. Example 2: Medium-Performance BiCMOS Process	33
2.5.3. Example 3: High-Performance BiCMOS Process	36
2.6. Complementary BiCMOS Technology	39
2.7. BiCMOS Design Rules	41
2.8. Chapter Summary	41
References	48
.....	
Chapter 3. Device Design Considerations	53
3.1. Design Considerations for MOSFET's	53
3.1.1. Threshold Voltage	54
3.1.2. Body Effect	54
3.1.3. Breakdown Voltage	55
3.1.4. Short-Channel Effects	56
3.1.5. Hot Carrier Effects	58
3.1.6. Latchup in CMOS	60
3.2. Design Considerations for Bipolar Transistors	62
3.2.1. Current Gain	63
3.2.2. Cutoff Frequency	66
3.2.3. Breakdown Voltages	67
3.2.4. Reachthrough Voltage	68
3.2.5. Base-Emitter Punchthrough	69
3.2.6. Parasitical Resistances	69
3.2.7. Junction Capacitances	72
3.3. BiCMOS Device Design Considerations	72
3.4. BiCMOS Device Scaling	76
3.4.1. MOS Device Scaling	76
3.4.2. Bipolar Device Scaling	79
3.5. Chapter Summary	84
References	84
.....	

Chapter 4. Device Modeling	87
4.1. Modeling of the MOS Transistor	87
4.1.1. MOSFET Structure and Operation	87
4.1.2. SPICE Models of the MOS Transistor	93
4.1.2.1. The Simple MOS DC Model	93
4.1.2.2. MOS Model (LEVEL 2)	98
4.1.2.3. Semi-Empirical Short-Channel Model (LEVEL 3)	107
4.1.2.4. BSIM Model (LEVEL 4)	112
4.1.2.5. MOS Capacitances	116
4.1.3. Analytical Model for Short-Channel MOS Devices	120
4.2. Modeling of the Bipolar Transistor	122
4.2.1. BJT Structure and Operation	122
4.2.2. Ebers-Moll Model	126
4.2.3. Bipolar Models in SPICE	134
4.3. Chapter Summary	140
References	141
.....	
Chapter 5. MOS Digital Integrated Circuits	145
5.1. The Static NMOS Inverter	145
5.1.1. DC Analysis	147
5.1.1.1. Saturated Enhancement-Type Load	147
5.1.1.2. Nonsaturated Enhancement-Type Load	150
5.1.1.3. Depletion-Type Load	151
5.1.1.4. Resistive Load	152
5.1.2. Transient Analysis	154
5.1.2.1. The Discharging Time	155
5.1.2.2. The Charging Time	157
5.1.3. NMOS Delay-Power Tradeoffs	160
5.2. NMOS Circuit Configurations	612
5.2.1. NMOS Source-Followers and Push-Pull Drivers	161

5.2.2. Bootstrapped Loads	163
5.2.3. NMOS Transmission Gates	165
5.2.4. NMOS Current Mode Logic	166
5.3. Dynamic NMOS Circuits	169
5.4. Complementary MOS (CMOS) Circuits	175
5.4.1. The CMOS Static Inverter	177
5.4.1.1. DC Analysis	177
5.4.1.2. Transient Analysis	179
5.4.1.3. Transient Power Dissipation	181
5.4.2. CMOS Static Gates	183
5.4.2.1. NAND/NOR CMOS Gates	183
5.4.2.2. Complex CMOS Logic Gates	185
5.4.2.3. CMOS Transmission Gates (CMOS TGs)	185
5.4.2.4. CMOS TG Logic	188
5.4.3. CMOS Static Flip-Flops	189
5.4.4. CMOS Dynamic Flip-Flops	191
5.4.5. Pseudo-NMOS CMOS Logic	193
5.4.6. Tristate CMOS Logic	194
5.4.7. Dynamic CMOS Circuits	194
5.4.7.1. NORA Logic	199
5.4.7.2. Zipper CMOS Logic	200
5.4.8. CMOS Nonthreshold Logic (NTL)	200
5.4.9. Cascode Voltage Switch Logic (CVSL)	203
5.5. Chapter Summary	203
References	205
.....	
Chapter 6. Bipolar CML Integrated Circuits	207
6.1. Emitter Coupled Logic (ECL)	207
6.1.1. Transient Analysis of ECL and CML Gates	214
6.1.1.1. Transient Analysis of the CML Gate	215

6.1.1.2. Transient Analysis of the ECL Gate	221
6.1.2. ECL Current Sources	224
6.1.3. ECL Reference Voltages	226
6.2. Emitter Function Logic (EFL)	227
6.2.1. EFL Cell Implementation	232
6.2.2. EFL Logic Building Blocks: Combinatorial Logic Elements	234
6.2.3. EFL Logic Building Blocks: Sequential Logic Elements	240
6.3. DC Specifications for a Practical EFL	247
6.4. Chapter Summary	249
References	249
.....	
Chapter 7. BiCMOS Digital Integrated Circuits	251
7.1. Comparison between Bipolar and MOS Transistors	251
7.2. BiCMOS Totem-Pole Inverter	255
7.2.1. DC Characteristics of the BiCMOS Inverter	259
7.2.2. Transient Analysis of the Totem-pole BiCMOS Inverter	265
7.2.3. Delay Dependence on the Device Parameters	278
7.2.4. BiCMOS Circuit Design	278
7.2.5. Comparing CMOS and BiCMOS Inverters' Speed	283
7.2.6. Layout of the BiCMOS Inverter	287
7.2.7. BiCMOS Gates	289
7.3. Full-Voltage-Swing BiCMOS Drivers	290
7.3.1. The AC Effects on the Swing of the Conventional BiCMOS Gate ...	290
7.3.2. BiNMOS Circuits	294
7.3.3. Full-Swing BiCMOS Circuits with Shunting Techniques	295
7.3.4. Full-Swing Common-Follower Complementary BiCMOS Circuits .	300
7.3.5. Full-Swing Common-Emitter Complementary BiCMOS Circuits ...	303
7.3.6. CMOS versus BiCMOS under Supply Voltage Scaling	310
7.4. Current Mode BiCMOS Circuits	313
7.4.1. The Basic MOS/Bipolar Merged CMS Cell	315

7.4.2. MOS/Bipolar Merged CML Gates	317
7.4.3. Multi-Emitter MOS/Bipolar Merged CML Gates	321
7.5. Chapter Summary	323
References	325
.....	
Chapter 8. BiCMOS Digital Circuit Applications	329
8.1. Adders	329
8.1.1. Combinational Full-Adder	329
8.1.2. Carry Lookahead Adder	332
8.1.3. Carry Propagation Adder	341
8.2. Multiplier	346
8.3. Random Access Memory	348
8.3.1. Read Only Memory	348
8.3.2. Static RAM	353
8.3.3. Dynamic RAM	366
8.3.4. Content Addressable Memory	367
8.4. Programmable Logic Arrays	371
8.5. Data Path	376
8.5.1. Arithmetic Logic Unit	376
8.5.2. Shifter	377
8.5.3. Register File	378
8.6. BiCMOS Logic Cells	380
8.7. BiCMOS Gate Arrays	381
8.8. Chapter Summary	389
References	390
Index	395

Preface

BiCMOS has faced, as any emerging technology, fierce opposition, but nevertheless has been widely accepted. The need for BiCMOS has been and still is a controversial issue. The cost of high-performance BiCMOS process speaks against it. However, there are other arguments supporting the need for such a technology. The comparison between the cost of CMOS and BiCMOS is not trivial especially if we account for the increasing expenses of scaling CMOS. In other words, adding bipolar to an existing CMOS process might be cheaper than scaling CMOS to obtain the same performance improvement. On the other hand, the high cost of BiCMOS may be justified by the high performance it can offer. In general, the application itself will dictate the technology that is to be used. If CMOS alone can satisfy the requirements, then it is more cost effective to use CMOS. Yet there are applications where the requirements can be only satisfied by using BiCMOS. There are currently commercial BiCMOS digital products such as high-speed SRAMs, fast microprocessors, gate arrays, in addition to digital, analog and mixed signal BiCMOS ASICs.

The technology for BiCMOS fabrication has matured over the last decade, yet the development of circuits and systems for such a technology is still lagging. There is a great interest among digital/analog circuit and system designers to develop techniques to exploit the flexibility that BiCMOS offers.

A large number of reports and technical papers have been published on the development of BiCMOS processes, circuits and systems. This book is an attempt to introduce many of the published ideas and concepts in order to assist students, researchers and design engineers to review the progress achieved so far. For example, in Chapter 2, we introduce the main BiCMOS processes and their performance/cost tradeoffs. In Chapter 7, we present the basic digital BiCMOS structures. The advantages of such circuits over CMOS are explained as well as their limitations. The application of BiCMOS for digital circuits and systems is illustrated in Chapter 8. Moreover, we have added two overview chapters; Chapter 5 on MOS IC's and Chapter 6 on bipolar current mode logic circuits. These two chapters were added because it is expected that future BiCMOS systems will not be limited to the use of BiCMOS circuit structures. The synergy of different structures and logic families will allow for better management of the overall speed and power. Therefore, we believe that those who work in this field should be familiar with the fundamentals of MOS and bipolar CML as well.

This book is also intended for senior undergraduate and graduate Electrical and Computer Engineering students who are interested in digital circuit design. Exposing the students at an early stage to the different technologies and design styles

is of great benefit to them. To those students we have also included Chapters 3 and 4, which introduce important basic information regarding the structures, operation and modeling of MOS and bipolar transistors. Such basic knowledge is essential for circuit designers because of the close interaction between device characteristics and circuit performance.

This book is an early contribution to the field of digital BiCMOS circuit design. It contains a collection of the contributions of all those who have devoted their time and effort to help us learn more about this field. We do not claim that this text is complete. In many instances, we have tried to summarize the work of others. So those who have special interest in one of the topics have to refer to the given references.

There is still the need for more research, investigation and experimentation to find answers to many of the unanswered questions regarding the optimum use of BiCMOS circuit structures. We are sure that the relentless search for better performance and quality will continue and will result in interesting and innovative ideas.

We hope that the readers of this book will find it useful and that it will add to their knowledge and assist them in contributing to the state-of-the-art of BiCMOS digital circuit design.

S.H.K. Embabi
A. Bellaouar
M.I. Elmasry

Acknowledgements

We would like, first of all, to acknowledge the countless blessings of God Almighty throughout our lives.

We would also like to thank our families whose support and endurance helped us to complete writing this book.

Writing this book would have been impossible without the knowledge contributed by the researchers and workers in this area. Their effort is deeply appreciated.

We also extend our thanks to Mr. Carl Harris from Kluwer Academic Publishers for encouraging us to work on this project.

We would also like to thank the reviewers for their careful and thorough review as well as their valuable comments and suggestions which resulted in some improvements. Special thanks to Drs. S. Rofail and Ali Salama for their critical review of the manuscript and fruitful discussions.

Our gratitude goes to all our colleagues in the Department of Electrical and Computer Engineering at the University of Waterloo for their support and encouragement, in particular, M. Elrabaa, W. Al-Mulla and P. Harvey.

The research work of the authors reported in this book has been supported in part by NSERC, BNR, NTE, ITRC and MICRONET. This support is greatly appreciated.

One of the authors, S.H.K. Embabi, would like to thank his colleagues in the Department of Electrical Engineering at Texas A&M University for their support, in particular, Professor E. Sanchez-Sinencio and Professor J.W. Howze.

We appreciate the effort of those who assisted us in various ways to prepare the manuscript and the figures, in particular, J. Pache, D. Pu, A. Dajani, P. Regier and T. Creasy.

List of Symbols

A_E	emitter area
A_C	collector area
β_f (or β_o)	maximum forward current gain.
β	forward current gain as function of the collector current.
BV_{DS}	drain-source breakdown voltage.
BV_{CBO}	collector-base breakdown voltage.
BV_{CEO}	collector-emitter breakdown voltage.
C_c	base-collector capacitance.
C_e	base-emitter capacitance.
C_s	collector-substrate capacitance.
C_{ox}	Gate capacitance.
C_d	source (drain) depletion capacitance.
C_{ov}	gate to source (drain) overlap capacitance.
C_L	external load capacitance.
C_D	diffusion capacitance.
C_o	total output capacitance.
D_{nB}	diffusion constant for the electrons in the base.
D_{pE}	diffusion constant for the holes in the emitter.
D_I	implantation dose to adjust the threshold voltage.
ϵ_o	permittivity of oxide.
ϵ_s	permittivity of silicon.
f_T	cutoff frequency.
γ	body effect coefficient.
γ_E	emitter injection efficiency.
I_{DS}	drain-source current.
I_{DSsat}	drain-source saturation current.
I_B	base current.
I_C	collector current.

I_E	emitter current.
I_K	forward knee current.
I_{HLI}	high level injection current.
I_s	transport saturation current.
I_{ss}	CML current
ITF	τ_{fo} high-current parameter.
J_K	forward knee current density.
k	Boltzman constant.
K_N	NMOS saturation current factor
K_P	PMOS saturation current factor
L	drawn channel length.
L_{eff}	effective channel length.
λ	channel length modulation factor.
N_s	channel doping concentration at the surface.
N_{bs}	channel doping concentration below the surface.
N_B	base doping concentration.
N_C	collector doping concentration.
N_E	emitter doping concentration.
N_{epi}	epitaxial layer doping concentration.
N_a	acceptor doping concentration.
N_d	donor doping concentration.
M_j	junction exponent (grading factor).
ϕ_j	junction built-in potential.
ϕ_s	surface potential of silicon.
ϕ_{ms}	gate electrode and silicon work function difference.
R_B	base resistance.
R_{Be}	extrinsic base resistance.
R_{Bi}	intrinsic base resistance.
R_C	collector resistance.
R_E	emitter resistance.

T	temperature.
τ_{fo}	minimum forward transit time.
τ_f	forward transit time.
t_{ox}	gate oxide thickness.
S	subthreshold swing.
V_{AF}	forward early voltage
V_{AR}	reverse early voltage
V_B	MOS bulk (substrate) voltage.
V_{BC}	base-collector voltage.
V_{BE}	base-emitter voltage.
V_{BEon}	turn ON base-emitter voltage.
V_{CE}	collector-emitter voltage.
V_{CEsat}	saturation collector-emitter voltage.
V_{FB}	flat band voltage.
V_{GS}	gate-source voltage.
V_{DS}	drain-source voltage.
V_{DSsat}	saturation drain-source voltage.
V_{dd}	power supply voltage.
V_{in}	input voltage.
V_o	output voltage.
V_{pt}	punchthrough voltage.
V_{rt}	reachthrough voltage.
V_s	Voltage swing.
V_i	thermal voltage.
VTF	$\tau_f V_{BC}$ dependence coefficient.
V_T	MOS threshold voltage.
V_{TO}	MOS threshold voltage when $V_B=0$.
V_{TN}	NMOS threshold voltage.
V_{TP}	PMOS threshold voltage.
v_{sat}	carrier saturation velocity.

W_{eff}	effective channel width.
W_D	depletion layer width in the bulk of the MOSFET.
W_N	NMOSFET device width.
W_P	PMOSFET device width.
W_E	emitter width.
W_B	base width.
W_C	collector width.
XTF	τ_f dependence coefficient.
x_j	source/drain junction depth.
x_{jE}	emitter junction depth.

DIGITAL BiCMOS INTEGRATED CIRCUIT DESIGN