Multi-Net Optimization of VLSI Interconnect

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To our many Intel colleagues and friends,
who taught us and learned from us.

Preface

Interconnect has become a crucial element in advanced electronic systems. State-of-the-art CMOS processes utilize 10 or more layers of metal above the active transistors, so these interconnect layers dominate processing costs. In recent years, *interconnect power* and *interconnect delay* have become major limiters for VLSI technology. Interconnect engineering—designing on-chip wires to satisfy performance requirements while meeting power, reliability, and cost specifications—is currently one of the most challenging tasks faced by product development teams. Significant difficulties arise because traditional approaches to the physical design of wires do not capture the interaction among multiple nets in complex interconnect structures.

While the downscaling of device sizes led to continuous improvement in the properties of transistors, it caused significant degradation in properties of the metal wires that are used as system interconnects. Wires have become limiters of speed, power dissipation, and reliability because of their growing resistance and capacitance in scaled fabrication processes. Interconnect issues have major implications on circuit architecture, design methodologies, and CAD tools. Timing/power/noise trade-offs have become interconnect centric, hence such trade-offs must be made during placement and routing of cells and wires.

Due to nonuniform scaling of wire thickness and wire width, net-to-net cross-capacitance between adjacent wires constitutes the largest part of total interconnect capacitance. Line-to-line cross-capacitances within the same metal layer are important determinants of speed and power so that mutual effects between parallel adjacent wires must be considered during the physical design of the circuit layout. Consequently, the spacing distance between wires on the chip has become a highly important resource, which deserves careful allocation and optimization. Since each space represents mutual interaction between two adjacent wires, simultaneous optimization of multiple wires is called for. However, tools and methodologies for VLSI layout generation typically work net by net, handling a single wire at a time.

This book integrates our research, our industrial experience, and our teaching experience in the field. It is focused on *simultaneous optimization of multiple nets*, considering the mutual interaction between wires. New techniques for layout migration and optimization are presented, employing *multinet optimization*. The interconnect layout area in each metal layer is regarded as a common resource shared by the wires. Multinet optimization allocates this resource by applying novel algorithms based on unique properties of the optimization problems considered. The material includes optimization under discrete (gridded) design rules for advanced lithography processes. Mathematical properties and conditions for optimality of multiwire layout structures are derived, algorithmic solutions are described and analyzed, design automation flows are described, and industrial examples in advanced nanoscale technology are presented.

The book is comprised of three major parts. The first part includes background material and introduction to the field, the second part is mostly a survey of classical net-by-net optimization techniques in VLSI circuit design, and the third part covers research on multinet optimization.

In the first part of the book, evolution of the interconnect scalability problem is described in Chapter 1 from both theoretical and practical viewpoints. In Chapter 2, interconnect aspects in design methodology and CAD tools are briefly reviewed, primarily for readers who are not familiar with practical details of layout design. In Chapter 3, a tutorial of scaling theory and electrical modeling of interconnects is given.

In the second part, Chapter 4 provides a classification of optimization problems and solution techniques in interconnect layout design, emphasizing the overall differences between net-by-net approaches and multinet approaches, and stressing the advantages of the latter approach. Chapter 5 contains a concise summary of methods in net-by-net interconnect and circuit optimization, covering both classical results and recent research results, such as a new unified logical effort theory.

The third and largest part of the book consists of Chapters 6–9, covering new multinet optimization approaches. Chapter 6 is focused on a simple (but very common) layout structure called a *bundle* of wires. It is simply a set of adjacent equal-length parallel wires in a single layer. Due to its simplicity, this specific layout pattern provides good insight, analytic results, and properties that are useful for optimizing various design objectives where the optimization variables are the individual *wire widths* and the *spaces* between adjacent wires. In Chapter 7, the same optimization problems are applied to *general wire layouts* rather than bundles, where the generalized wire structure is described by a visibility graph. In Chapter 8, the simple bundle of wires is revisited, but a different kind of optimization is used, namely, *reordering of the wires* within the bundle in addition to sizing and spacing. In Chapter 9, a hierarchical solution is presented for the problem of *layout migration*. The contribution of Ron Pinter and Yuval Shaphir to this chapter is hereby gratefully acknowledged. In Chapter 10, future research and development directions in interconnect design are outlined.

For us, this book is a summary of many exciting endeavors performed over many years of work in this field. We hope it will help students, researchers, and engineers and inspire them to find creative solutions to system interconnect issues in future generations of technology.

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Contents

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Konstantin Moiseev received his B.Sc. and M.Sc. in Computer Engineering and Ph.D. in Electrical Engineering from the Technion – Israel Institute of Technology, Haifa, Israel, in 2001, 2006, and 2011, respectively. Since 2006, he has been working with Intel Israel Design Center, Haifa, Israel. His general interests include computer-aided design systems, combinatorial optimization, heuristic methods, VLSI system design, and interconnect design.

Avinoam Kolodny is an associate professor of electrical engineering at Technion – Israel Institute of Technology. He joined Intel after completing his doctorate in microelectronics at the Technion in 1980. During 20 years with the company, he was engaged in diverse areas, including nonvolatile memory device physics, electronic design automation, and organizational development. He pioneered static timing analysis of processors, served as Intel's corporate CAD system architect at the introduction of logic synthesis, and was manager of Intel's performance verification CAD group in Israel. He has been a member of the Faculty of Electrical Engineering at the Technion since 2000. His current research is focused primarily on interconnect issues in VLSI systems, covering all levels from physical design of wires to networks on chips and multicore system architecture.

Shmuel Wimer received his B.Sc. and M.Sc. degrees in Mathematics from Tel Aviv University, Tel Aviv, Israel, and his D.Sc. degree in Electrical Engineering from the Technion-Israel Institute of Technology, Haifa, Israel, in 1978, 1981, and 1988, respectively. He worked for 32 years at industry R&D, engineering, and managerial positions. From 1999 to 2009, he was with Intel Design Center in Haifa, Israel, where he was responsible for the development, implementation, and execution of Intel's microprocessors' physical layout design migration (a.k.a. Tick-Tock). Prior to that, he worked for IBM, National Semiconductor, and Israeli

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