

# Oversampling A/D Converters with Improved Signal Transfer Functions

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Bupesh Pandita

# Oversampling A/D Converters with Improved Signal Transfer Functions

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# Abstract

This book proposes a low-IF receiver architecture suitable for the realization of single-chip receivers. To alleviate the image-rejection requirements of the front-end filters an oversampling complex discrete-time  $\Delta\Sigma$  ADC with a signal-transfer function that achieves a significant filtering of interfering signals is proposed. A filtering ADC reduces the complexity of the receiver by minimizing the requirements of analog filters in the IF digitization path. Discrete-time  $\Delta\Sigma$  ADCs have precise resonant frequency and clock frequency ratios and, hence, do not require the calibration or tuning that is necessary in the case of continuous-time  $\Delta\Sigma$  modulator implementations. This feature makes the proposed discrete-time  $\Delta\Sigma$  ADC ideal for multistandard receiver applications.

The  $\Delta\Sigma$  modulator signal-transfer function (STF) and noise-transfer function (NTF) have been designed using complex filter routines based on classical filter design procedures. With a filtering STF and stop band attenuation greater than 30 dB, the  $\Delta\Sigma$  modulator reduces intermodulation of the desired signal and the interfering signals at the input of the quantizer, and also avoids feedback of the high-frequency interfering signals at the input of the modulator.

The reported complex  $\Delta\Sigma$  ADC is intended for DTV receiver applications. With a maximum intended sampling frequency of 128 MHz and an OSR of 16, the ADC has been designed to support a maximum DTV signal bandwidth of 8 MHz. Except for a somewhat reduced maximum sampling frequency, the test results of the prototype complex  $\Delta\Sigma$  modulator are very close to the simulated results. The IC achieved 70.9 dB SNDR over a 6 MHz band centered around 3 MHz. The image rejection ratio (IRR) of the  $\Delta\Sigma$  ADC was measured to be greater than 65 dB. The measurement results confirm the filtering characteristics of the ADC. The fabricated chip consumes 177 mW and occupies a silicon area of 2.15 mm<sup>2</sup>.



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