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Soft Errors in Modern Electronic Systems

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Foreword

The ideas of reliability, or should I say unreliability, in computing began with von Neumann's 1963 paper [1]. In the intervening years, we flip-flopped between thoughts such as "semiconductors are inherently reliable" and "increasing complexity can lead to error buildup".

Change over to digital technology was a welcome relief from a variety of electrical noises generated at home. While we continue to fictionalize the arrival of extraterrestrial beings, we did not suspected that they would arrive early to affect our electronic systems. Let me quote from a recent paper, "From the beginning of recorded history, man has believed in the influence of heavenly bodies on the life on the Earth. Machines, electronics included, are considered scientific objects whose fate is controlled by man. So, in spite of the knowledge of the exact date and time of its manufacture, we do not draft a horoscope for a machine. Lately, however, we have started noticing certain behaviors in the state of the art electronic circuits whose causes are traced to be external and to the celestial bodies outside our Earth [2]".

May and Woods of Intel Corporation reported on alpha particle induced *soft errors* in the 2107-series 16-KB DRAMs. They showed that the upsets were observed at sea level in dynamic RAMs and CCDs. They determined that these errors were caused by α particles emitted in the radioactive decay of uranium and thorium present just in few parts per million levels in package materials. Their paper represents the first public account of radiation-induced upsets in electronic devices at the sea level and those errors were referred to as "soft errors" [3].

It has been recognized since 1940s that an *electromagnetic pulse* (EMP) can cause temporal malfunction or even permanent damage in electronic circuits. The term EMP refers to high energy electromagnetic radiation typically generated by lightning or through interaction of charged particles in the upper atmosphere with γ rays or X rays. Carl E. Baum, perhaps the most significant contributor to the EMP research, traces the history of the EMP phenomenon and reviews a large amount of published work in his 188-reference survey article [4]. Besides providing techniques of radiation hardening, shielding and fault-tolerance, significant amount of experimental work has been done on developing EMP simulator hardware. I particularly mention this because I believe that collaboration between soft error and EMP research communities is possible and will be beneficial.

The publication of this book is the latest event in the history I have cited above. Its contributing editor, Michael Nicolaidis, is a leading authority on soft errors. He is an original contributor to research and development in the field. Apart from publishing his research in a large number of papers and patents he cofounded iROC Technologies. His company provides complete soft-error analysis and design services for electronic systems.

Nicolaidis has gathered an outstanding team of authors for the ten chapters of this book that cover the breadth and depth. This is the first book to include almost all aspects of soft errors. It comprehensively includes historical views, future trends, the physics of SEU mechanisms, industrial standards and practices of modeling, error mitigation methods, and results of academic and industry research. There is really no other published book that has such a complete coverage of soft errors.

This book fills a void that has existed in the technical literature. In the words of my recently graduated student, Fan Wang, "During the time I was a graduate student I suffered a lot trying to understand different topics related to soft errors. I have read over two hundred papers on this topic. Soft error is mentioned in most books on VLSI reliability, silicon technology, or VLSI defects and testing, however, there is no book specifically on soft errors. Surprisingly, the reported measurements and estimated results in the scattered literature vary a lot sometimes even seem to contradict each other. I believe this book will be very useful for academic research and serve as an industry guide".

The book provides some interesting reading. The early history of soft errors is like detective stories. Chapter 1 documents the case of soft errors in the Intel 2107-series 16-kb DRAMs. Culprits are found to be alpha particles emitted through the radioactive decay of uranium and thorium impurities in the packaging material. The 1999 case of soft errors in Sun's Enterprise server results in design reforms leading to the applications of coding theory and inventions of new design techniques.

A serious reader must go through Chap. 2 to learn the terms and definitions and Chap. 3 that provides the relevant standards. Chapters 4 and 5 discuss methodologies for modeling and simulation at gate and system levels, respectively. Hardware fault injection techniques are given in Chap. 6, with accelerated testing discussed in Chap. 7. Chapters 8 and 9 deal with soft-error mitigation techniques at hardware and software levels, respectively. Chapter 10 gives techniques for evaluating the soft-error tolerance of systems.

Let us learn to deal with soft errors before they hurt us.

Vishwani D. Agrawal

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Preface

In the early computer era, unreliable components made fault-tolerant computer design mandatory. Dramatic reliability gains in the VLSI era restricted the use of fault-tolerant design in critical applications and hostile environments. However, as we are approaching the ultimate limits of silicon-based CMOS technologies, these trends have been reversed. Drastic device shrinking, very low operating voltages, increasing complexities, and high speeds made circuits increasingly sensitive to various kinds of failures. Due to these trends, soft errors, considered in the past as a concern for space applications, became during the past few years a major source of system failures of electronic products even at ground level. Consequently, soft-error mitigation is becoming mandatory for an increasing number of application domains, including networking, servers, avionics, medical, and automotive electronics. To tackle this problem, chip and system designers may benefit from several decades of soft error related R&D from the military and space. However, as ground-level applications concern high-volume production and impose stringent cost and power dissipation constraints, process-based and massive-redundancy-based approaches used in military and space applications are not suitable in these markets.

Significant efforts have therefore been made during the recent years in order to benefit from the fundamental knowledge and engineering solutions developed in the past and at the same time develop new solutions and tools for supporting the constraints of ground-level applications. After design for test (DFT), design for manufacturability (DFM), and design for yield (DFY), the design for reliability (DFR) paradigm is gaining importance starting with design for soft error mitigation. Dealing with soft errors is a complex task that may involve high area and power penalties, as copying with failures occurring randomly during system operation may require significant amounts of redundancy. As a consequence, a compendium of approaches is needed for achieving product reliability requirements at low area and power penalties. Such approaches include:

- Test standards for characterizing the soft-error rate (SER) of the final product and of circuit prototypes in the terrestrial environment. Such standards are mandatory for guarantying the accuracy of test results and for having a common

reference when comparing the SER, measured in terms of Failure in Time (FIT), of devices provided by different suppliers.

- SER-accelerated testing platforms, approaches, and algorithms for different devices, including SRAMs, DRAMs, TCAMs, FPGAs, processors, SoCs, and complete systems.
- SER-accelerated testing platforms, approaches, and algorithms for cell libraries.
- Software/hardware methodologies and tools for evaluating SER during the design phase. Such tools become increasingly important for two major reasons. Characterizing SER during the design phase is the only way for avoiding bad surprises when the circuit prototype or the final product is tested, which could lead to extra design and fabrication cycles and loss of market opportunities. Interactive SER estimation during the design cycle is the only way for making the necessary tradeoffs, determining the circuit critical parts and selecting the most efficient mitigation approaches for meeting a reliability target at minimal cost in terms of power, speed, and area. Software and hardware tools at various levels are required such as:

  - TCAD tools for characterizing the transient current pulses produced by alpha particles and secondary particles.
  - Cell FIT estimation tools to guide the designers of memory cells and cell libraries for meeting their SER budget at minimal cost, and for providing the cell FIT to the higher level SER estimation tools.
  - Spice-level FIT estimation, usually for evaluating the impact of transient pulses in sequential cells and in combinational logic.
  - Gate-level FIT estimation tools for characterizing IP blocks: based on exact, statistical or probabilistic approaches; considering the logic function only (for logic derating computation) or both the logic function and the SDF files (for combined logic and time derating computation).
  - RTL FIT estimation.
  - SoC FIT estimation, for taking into account the functional derating at the SoC level.
  - Fault injection in hardware platforms for accelerating the FIT estimation task at IP level and SoC level.

- Soft-error mitigation approaches at hardware level including: error detecting and correcting codes, hardened cells, self-checking circuits, double sampling approaches, instruction-level retry.
- Soft-error mitigation approaches at software level, operating system level, as well as check-pointing and rollback recovery.

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Michael Nicolaidis

Purpose

The purpose of this book is to provide a comprehensive description of the highly complex chain of physical processes that lead to the occurrence of soft errors. Mastering soft errors and the related chain of physical processes requires mastering numerous technological domains, including: nuclear reactions of cosmic rays with the atmosphere (neutron and proton generation at ground level); nuclear reactions of atmospheric neutrons and protons with die atoms (secondary particles generation); coulomb interaction (ionization); device physics (charge collection); electrical simulation (SEU creation, SET propagation); event-driven simulation (for combined logic and time derating estimation); logic domain simulation (for logic derating estimation); RTL simulation; and hardware emulation. Most of these domains are extremely challenging and may lead to unacceptable simulation time for achieving good accuracy. Past and recent developments in these domains are reported in the book.

The book is also aimed at providing a comprehensive description of various hardware and software techniques enabling soft-error mitigation at moderate cost. This domain is also challenging, since coping with failures occurring randomly during system operation is not trivial and usually requires significant amounts of redundancy. Recent developments dealing with these issues are also reported.

Finally, as other reliability threats, including variability, EMI and accelerating aging are gaining significance, solutions that could be used to simultaneously address all of them are also discussed.

To reach its goals, the book is organized in ten chapters following a coherent sequence, starting with Chap. 1:

- *Soft Errors, from Space to Ground: Historical Overview, Empirical Evidence and Future Trends*

and finishing with Chap. 10:

- *Specification and Verification of Soft Error Performance in Reliable Electronic Systems, dealing with Soft-Errors in Complex Industrial Designs*

through eight chapters dealing with:

- *Single Event Effects: Mechanisms and Classification*
- *JEDEC Standards on Measurement and Reporting of Alpha Particles and Terrestrial Cosmic Ray-Induced Soft Errors*
- *Gate Level Modeling and Simulation*
- *Circuit and System Level Single Event Effects Modeling and Simulation*
- *Hardware Fault Injection*
- *Integrated circuit qualification for Space and Ground-level Applications: Accelerated tests and Error-Rate Predictions*
- *Circuit-level Soft-Error Mitigation*
- *Software-Level Soft-Error Mitigation Techniques*

The aim of this volume is to be a reference textbook describing: all the basic knowledge on soft errors for senior undergraduate students, graduate students in MSc or PhD tracks and teachers; the state-of-the-art developments and open issues in the field for researchers and professors conducting research in this domain; and a comprehensive presentation of soft errors-related issues and challenges that may face circuit and system designers and managers, together with the most efficient solutions, methodologies, and tools that they can use to deal with.

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