Integrated Circuits and Systems

Series Editor
Anantha Chandrakasan, Massachusetts Institute of Technology
Cambridge, Massachusetts

For other titles published in this series, go to
www.springer.com/series/7236

Ron Ho • Robert Drost
Editors

Coupled Data Communication Techniques for High-Performance and Low-Power Computing

Springer

Editors
Ron Ho
Oracle Corporation
Sun Labs
VLSI Research Group
16 Network Circle
UMPK 16-161
Menlo Park, CA 94025
USA
ron.ho@oracle.com

Robert Drost
Los Altos, CA 94024
USA

ISSN 1558-9412
ISBN 978-1-4419-6587-5 e-ISBN 978-1-4419-6588-2
DOI 10.1007/978-1-4419-6588-2
Springer New York Dordrecht Heidelberg London

Library of Congress Control Number: 2010927932

Printed on acid-free paper

Springer is part of Springer Science+Business Media (www.springer.com)

For Christina, Sawyer, and Finley – RH
For Sharon and Juliet – RJD

Foreword

Wafer-scale integration has long been the dream of system designers. Instead of chopping a wafer into a few hundred or a few thousand chips, one would just connect the circuits on the entire wafer. What an enormous capability wafer-scale integration would offer: all those millions of circuits connected by high-speed on-chip wires. Unfortunately, the best known optical systems can provide suitably fine resolution only over an area much smaller than a whole wafer. There is no known way to pattern a whole wafer with transistors and wires small enough for modern circuits.

Statistical defects present a firmer barrier to wafer-scale integration. Flaws appear regularly in integrated circuits; the larger the circuit area, the more probable there is a flaw. If such flaws were the result only of dust one might reduce their numbers, but flaws are also the inevitable result of small scale. Each feature on a modern integrated circuit is carved out by only a small number of photons in the lithographic process. Each transistor gets its electrical properties from only a small number of impurity atoms in its tiny area. Inevitably, the quantized nature of light and the atomic nature of matter produce statistical variations in both the number of photons defining each tiny shape and the number of atoms providing the electrical behavior of tiny transistors. No known way exists to eliminate such statistical variation, nor may any be possible.

Proximity communication, or coupled data communication in general, may make possible the long-sought dream of wafer scale integration. Proximity communication permits assembly of wafer-scale systems from small parts. We can make circuit chips small enough for low defect rates, cast aside bad chips, and reassemble the good chips into wafer-scale systems.

Two properties of proximity communication suit it to wafer-scale use. First, quality: the connections between chips are nearly as good as wires on a single chip. As this book describes, proximity connections are fast, occupy small area, and consume little energy. Second, and I think much more important, is replacement: proximity communication permits one to replace chips in a big system. Together, quality and replacement make wafer-scale integration possible. Because I think replacement is so important, Im going to devote a few more lines to it.

What makes replacement possible? Proximity communication needs neither welds nor solder. The parts are joined electrically only by the electric fields between them. These fields pass right through the top layers of glass that protect the chips. Within error limits, the communication is also insensitive to chip separation and chip alignment. If one chip in a wafer-scale assembly of hundreds of chips proves unsuitable because of a hidden defect, or through aging, or simply for product upgrade, no physical bonds prevent its replacement.

I believe that replacement will prove most useful for test. A complete system could serve as a jig that would test fresh chips in their real environment. Each fresh chip would spend only long enough in the complete system for a thorough test. A test jig smaller than a complete system might also serve to test only a single type of chip, providing it an environment indistinguishable from a full system. Such a test jig would have full speed access to every connection to or from the fresh chip. I see a huge potential for replacement to simplify and improve test.

I also see that replacement may permit a profound change in the business alliances that produce products. Without the ability to replace, one bad chip destroys an entire multi-chip module, making specialization in module assembly a poor business. Because one bad chip spoils the entire module, a contractor who assembles multi-chip modules must take responsibility not only for defects in his own process, but also for defects in separate chips. This dual responsibility is a very high barrier to contract assembly.

Board-level assembly houses are common because they avoid this dual barrier in two ways. First, not only is board-level assembly an old art with a well known low defect density but also it uses packaged and well tested parts. Second and more important, at the board-level some, albeit limited, replacement is possible. It is possible to remove and reuse at least the high-value chips on a board-level assembly, greatly reducing the high cost of bad parts. I believe that because proximity communication permits replacement it will also foster wafer-scale assembly houses.

Bob Johnson, formerly technical head of Burroughs, talked about using conductive grease to connect the ordinary pads on chips placed face-to-face. A large area of thin grease between facing pads would provide a connection. The thinner and much longer layer of grease reaching to other pads would produce small but manageable cross talk. I merely replaced Johnson's grease with electric fields. Robert Drost's fiendishly clever diagonal arrangement of pads greatly reduces cross talk.

Bob Bosnyak designed and measured some early proximity communication test chips. I recall one flawed ring oscillator test chip built for us by the MOSIS foundry service. The flaw turned out to be total omission of the metal plates on adjacent levels of metal that were to form the bulk of Bosnyak's test structure. Nevertheless, the test chip worked, albeit at a mystifying small fraction of its intended speed. The mystery vanished when we discovered the omitted plates. MOSIS rebuilt the test chip for free.

The late Bob Proebsting, a pioneer and life-long designer of fine memory parts, contributed to us much knowledge about sense amplifiers. For a period, the authors of this book were, in effect, Proebsting's post-doc students. As usual in such relationships, both the brilliant teacher and the apt students took much delight from the process. It was my joy to assemble such a mass of brainpower and to watch both its progress and the continuing delight of its participants.

Portland, Oregon, September 2009 *Ivan Sutherland*

Contents

Part I Introduction

Part II Overview of 3D Technologies

Part III Coupled Data Technologies

Part IV Enabling Coupled Data Technologies

Part V Extending Data Coupling Technologies

List of Contributors

Dr. Ron Ho
Sun Microsystems Research Labs, 16 Network Circle, Menlo Park, CA 94025,
USA, e-mail: ron.ho@sun.com

Dr. Robert Drost
Sun Microsystems Research Labs, 16 Network Circle, Menlo Park, CA 94025,
USA, e-mail: robert.drost@sun.com

Dr. Muhannad Bakir
Microelectronics Research Center, Georgia Institute of Technology, 791 Atlantic
Dr. NW, Atlanta, GA 30332-0269, USA, e-mail: muhannad.bakir@mirc.gatech.edu

Alex Chow
Sun Microsystems Research Labs, 16 Network Circle, Menlo Park, CA 94025,
USA, e-mail: alex.chow@sun.com

Dr. John E. Cunningham
Sun Microsystems Chief Technology Organization, 9515 Towne Centre Drive, San
Diego, CA 92121, USA, e-mail: john.cunningham@sun.com

Dr. Bing Dang
IBM T. J. Watson Research Center, 1101 Kitchawan Rd, RM 6-242, Yorktown
Heights, NY 10598, USA, e-mail: dangbing@us.ibm.com

Dr. Hans Eberle
Sun Microsystems Research Labs, 16 Network Circle, Menlo Park, CA 94025,
USA, e-mail: hans.eberle@sun.com

Prof. Paul Franzon
Department of Electrical and Computer Engineering, North Carolina State
University, Box 7914, Raleigh, NC, 27695, USA, e-mail: paulf@ncsu.edu

David Hopkins
Sun Microsystems Research Labs, 16 Network Circle, Menlo Park, CA 94025,

USA, e-mail: robert.hopkins@sun.com

Dr. Gang Huang
Intel Corporation, Ultra Mobility Group, 1501 S. MO-Pac Expy, Austin, TX 78746
USA, e-mail: gang.huang@intel.com

Dr. Ashok V. Krishnamoorthy
Sun Microsystems Chief Technology Organization, 9515 Towne Centre Drive, San Diego, CA 92121, USA, e-mail: ashok.krishnamoorthy@sun.com

Professor Tadahiro Kuroda
Department of Electrical Engineering, Keio University, 3-14-1, Hiyoshi, Kohoku-ku, Yokohama 223-8522, JAPAN, e-mail: kuroda@elec.keio.ac.jp

Jon K. Lexau
Sun Microsystems Research Labs, 16 Network Circle, Menlo Park, CA 94025, USA, e-mail: jon.lexau@sun.com

Dr. Frankie Liu
Sun Microsystems Research Labs, 16 Network Circle, Menlo Park, CA 94025, USA, e-mail: frankie.liu@sun.com

Professor Noriyuki Miura
Department of Electrical Engineering, Keio University, 3-14-1 Hiyoshi, Kohoku-ku, Yokohama 223-8522 JAPAN, e-mail: miura@kuro.elec.keio.ac.jp

Dr. James G. Mitchell
Sun Microsystems Chief Technology Organization, 16 Network Circle, Menlo Park, CA 94025, USA, e-mail: jim.mitchell@sun.com

Dr. Kohei Onizuka
Formerly with the Institute of Industrial Science, University of Tokyo, and now with Toshiba Corporation.

Dr. Dinesh D. Patil
Sun Microsystems Research Labs, 16 Network Circle, Menlo Park, CA 94025, USA, e-mail: dinesh.d.patil@sun.com

Professor Takayasu Sakurai
Institute of Industrial Science, University of Tokyo, 4-6-1 Komaba, Meguro-ku, Tokyo 153-8505, JAPAN, e-mail: tsakurai@iis.u-tokyo.ac.jp

Dr. Ivan Shubin
Sun Microsystems Chief Technology Organization, 9515 Towne Centre Drive, San Diego, CA 92121, USA, e-mail: ivan.shubin@sun.com

Professor Makoto Takamiya
VLSI Design and Education Center, University of Tokyo, 4-6-1 Komaba, Meguro-ku, Tokyo 153-8505, JAPAN, e-mail: mtaka@iis.u-tokyo.ac.jp

Dr. Xuezhe Zheng
Sun Microsystems Chief Technology Organization, 9515 Towne Centre Drive, San Diego, CA 92121, USA, e-mail: xuezhe.zheng@sun.com