

High-Speed DSP and Analog System Design

Thanh T. Tran

High-Speed DSP and Analog System Design

 Springer

Thanh T. Tran
Texas Instruments Incorporated
12203 Southwest Freeway, MS 722
Stafford, TX 77477
USA

ISBN 978-1-4419-6308-6 e-ISBN 978-1-4419-6309-3
DOI 10.1007/978-1-4419-6309-3
Springer New York Dordrecht Heidelberg London

Library of Congress Control Number: 2010926196

© Springer Science+Business Media, LLC 2010

All rights reserved. This work may not be translated or copied in whole or in part without the written permission of the publisher (Springer Science+Business Media, LLC, 233 Spring Street, New York, NY 10013, USA), except for brief excerpts in connection with reviews or scholarly analysis. Use in connection with any form of information storage and retrieval, electronic adaptation, computer software, or by similar or dissimilar methodology now known or hereafter developed is forbidden. The use in this publication of trade names, trademarks, service marks, and similar terms, even if they are not identified as such, is not to be taken as an expression of opinion as to whether or not they are subject to proprietary rights.

Printed on acid-free paper

Springer is part of Springer Science+Business Media (www.springer.com)

To my family, Nga, Lily, Kevin and Robin

Preface

This book covers the high-speed DSP and analog system design techniques and highlights common pitfalls causing noise and electromagnetic interference problems engineers have been facing for many years. The material in this book originated from my high-speed DSP system design guide (Texas Instruments SPRU 889), my system design courses at Rice University and my experience in designing computers and DSP systems for more than 25 years. The book provides hands-on, practical advice for working engineers, including:

- Tips on cost-efficient design and system simulation that minimize late-stage redesign costs and product shipment delays.
- 11 easily-accessible chapters in 210 pages.
- Emphasis on good high-speed and analog design practices that minimize both component and system noise and ensure system design success.
- Guidelines to be used throughout the design process to reduce noise and radiation and to avoid common pitfalls while improve quality and reliability.
- Hand-on design examples focusing on audio, video, analog filters, DDR memory, and power supplies.

The inclusion of analog systems and related issues cannot be found in other high-speed design books.

This book is intended for practicing engineers and is organized as follows:

- **Chapter 1:** Highlights challenges in designing video, audio, and communication systems.
- **Chapter 2:** Covers transmission line theories and effects. Demonstrates different signal termination schemes by performing signal integrity simulations and lab measurements.
- **Chapter 3:** Shows the effects of crosstalk and methods to reduce interference.
- **Chapter 4:** Provides an overview of switching and linear power supplies and highlights the importance of having proper power sequencing schemes and power supply decoupling.
- **Chapter 5:** Covers the analytical and general power supply decoupling techniques.
- **Chapter 6:** Covers design considerations of analog phase-locked loop (APLL) and digital phase-locked loop (DPLL) and how to isolate noise from affecting APLL and DPLL jitter.
- **Chapter 7:** Presents an overview of data converter, sampling techniques and quantization noise.
- **Chapter 8:** Covers analog active and passive filter design including operational amplifier design with single-rail and dual-rail power supplies.
- **Chapter 9:** Provides memory sub-system design considerations. Includes DDR overview, signal integrity and design example.
- **Chapter 10:** Covers printed circuit board (PCB) stackup and signal routing considerations.
- **Chapter 11:** Describes sources of electromagnetic interference (EMI) and how to mitigate them.

ACKNOWLEDGMENTS

I would like to thank many of my colleagues at Texas Instruments Incorporated who encouraged me to write this manuscript, Kevin Jones for doing the lab measurements to validate some of the theoretical concepts and simulations and Cathy Wicks for her outstanding support in many ways. Also special thanks to Jennifer Maurer and Jennifer Evans of Springer for giving me this writing opportunity and for reviewing and providing great suggestions. This book would not have been possible without the help and support from all these great individuals.

And, I just can't thank my brother, Nhut Tran, enough for tirelessly spending weeks to review and edit every chapter in this book. As for my daughter, Lily Tran, instead of relaxing over the Christmas break from months of extremely hard work at Massachusetts Institute of Technology, she voluntarily reviewed the entire manuscript and provided invaluable inputs. Again, sincere thanks to both Nhut and Lily for doing this!

Finally, for my wife, Nga, I am still amazed with how she can hold a very demanding full-time job at HP and still find time to provide great support to me and care to our kids. She is truly an amazing friend and a remarkable soccer mom.

Thanh T. Tran
Houston, Texas, 2010

Contents

| | |
|---|-----------|
| Chapter 1: Challenges of DSP Systems Design..... | 1 |
| 1.1 High-Speed Dsp Systems Overview..... | 2 |
| 1.2 Challenges Of Dsp Audio System | 5 |
| 1.3 Challenges Of Dsp Video System | 6 |
| 1.4 Challenges Of Dsp Communication System | 8 |
| References..... | 11 |
| Chapter 2: Transmission Line (TL) Effects..... | 13 |
| 2.1 Transmission Line Theory..... | 14 |
| 2.2 Parallel Termination Simulations | 19 |
| 2.3 Practical Considerations Of TL | 21 |
| 2.4 Simulations And Experimental Results Of TL..... | 22 |
| 2.4.1 TL Without Load Or Source Termination | 22 |
| 2.4.2 TL With Series Source Termination | 24 |
| 2.5 Ground Grid Effects On TL..... | 27 |
| 2.6 Minimizing TL Effects | 28 |
| References..... | 30 |
| Chapter 3: Effects of Crosstalk..... | 31 |
| 3.1 Current Return Paths..... | 31 |
| 3.2 Crosstalk Caused By Radiation | 36 |
| 3.3 Summary..... | 41 |
| References..... | 43 |

| | |
|--|------------|
| Chapter 4: Power Supply Design Considerations | 45 |
| 4.1 Power Supply Architectures | 45 |
| 4.2 DSP Power Supply Architectural Considerations | 55 |
| 4.2.1 Power Sequencing Considerations..... | 61 |
| 4.3 Summary..... | 64 |
| References..... | 65 |
| Chapter 5: Power Supply Decoupling | 67 |
| 5.1 Power Supply Decoupling Techniques..... | 67 |
| 5.1.1 Capacitor Characteristics | 69 |
| 5.1.2 Inductor Characteristics | 72 |
| 5.1.3 Ferrite Bead Characteristics..... | 74 |
| 5.1.4 General Rules-Of-Thumb Decoupling Method | 75 |
| 5.1.5 Analytical Method of Decoupling | 77 |
| 5.1.6 Placing Decoupling Capacitors..... | 91 |
| 5.2 High Frequency Noise Isolation | 94 |
| 5.2.1 Pi Filter Design | 95 |
| 5.2.2 T Filter Design | 98 |
| 5.3 Summary..... | 102 |
| References..... | 104 |
| Chapter 6: Phase-Locked Loop (PLL) | 105 |
| 6.1 Analog PLL (APLL)..... | 105 |
| 6.1.1 PLL Jitter | 107 |
| 6.2 Digital PLL (DPLL) | 111 |
| 6.3 PLL Isolation Techniques..... | 114 |
| 6.3.1 Pi and T Filters..... | 114 |
| 6.3.2 Linear Voltage Regulator..... | 118 |
| 6.4 Summary..... | 119 |
| References..... | 120 |
| Chapter 7: Data Converter Overview | 121 |
| 7.1 Dsp Systems..... | 121 |
| 7.2 Analog-To-Digital Converter (ADC) | 122 |
| 7.2.1 Sampling | 124 |
| 7.2.1 Quantization Noise..... | 126 |
| 7.3 Digital-To-Analog Converter (DAC) | 130 |

| | |
|---|------------|
| 7.4 Practical Data Converter Design Considerations | 132 |
| 7.4.1 Resolution and Signal-to-Noise | 133 |
| 7.4.2 Sampling Frequency | 134 |
| 7.4.3 Input and Output Voltage Range | 134 |
| 7.4.4 Differential Non-Linearity (DNL) | 135 |
| 7.4.5 Integral Non-Linearity (INL) | 137 |
| 7.5 Summary | 138 |
| References | 140 |
| Chapter 8: Analog Filter Design | 141 |
| 8.1 Anti-Aliasing Filters | 141 |
| 8.1.1 Passive and Active Filters Characteristics | 142 |
| 8.1.2 Passive Filter Design | 143 |
| 8.1.3 Active Filter Design | 146 |
| 8.1.4 Operation Amplifier (op amp) Fundamentals | 147 |
| 8.1.5 DC and AC Coupled | 155 |
| 8.1.6 First Order Active Filter Design | 164 |
| 8.1.7 Second Order Active Filter Design | 169 |
| 8.2 Summary | 175 |
| References | 176 |
| Chapter 9: Memory Sub-System Design Considerations | 177 |
| 9.1 DDR Memory Overview | 177 |
| 9.1.1 DDR Write Cycle | 179 |
| 9.1.2 DDR Read Cycle | 181 |
| 9.2 DDR Memory Signal Integrity | 181 |
| 9.3 DDR Memory System Design Example | 183 |
| References | 186 |
| Chapter 10: Printed Circuit Board (PCB) Layout | 187 |
| 10.1 Printed Circuit Board (PCB) Stackup | 187 |
| 10.2 Microstrip And Stripline | 190 |
| 10.3 Image Plane | 192 |
| 10.4 Summary | 193 |
| References | 194 |

| | |
|---|------------|
| Chapter 11: Electromagnetic Interference (EMI) | 195 |
| 11.1 FCC Part 15B Overview | 195 |
| 11.2 EMI Fundamentals..... | 197 |
| 11.3 Digital Signals | 199 |
| 11.4 Current Loops | 201 |
| 11.5 Power Supply..... | 202 |
| 11.6 Transmission Line | 204 |
| 11.7 Power And Ground Planes..... | 206 |
| 11.8 Summary: EMI Reduction Guidelines..... | 208 |
| References..... | 210 |
| Glossary | 211 |
| Index | 213 |

About The Author

DR. THANH TRAN has over 25 years of experience in high-speed DSP, computer and analog system design and is an engineering manager at Texas Instruments Incorporated. He currently holds 22 issued patents and has published more than 20 contributed articles. He is also an adjunct faculty member at Rice University where he teaches analog and digital embedded systems design courses. Tran received a BSEE degree from the University of Illinois at Urbana-Champaign, Illinois in 1984 and Master of Electrical Engineering and Ph.D. in Electrical Engineering degrees from the University of Houston, Houston, Texas in 1995 and 2001 respectively.