
INTEGRATED CIRCUIT PACKAGING, ASSEMBLY AND INTERCONNECTIONS

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ASSEMBLY AND INTERCONNECTIONS**

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 Springer

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DEDICATION

To my family,

my wife Joan

and

our children, their spouses and grandchildren

Karen – Christopher, Ryan, Kevin

Billy and Cathy – Alli, Jeff, Shauna

Joni and Fred – Danny, Kerri, Traci Jo

Jimmy and Colleen – Maggie, Molly, Katie, Claire

Ronny and Meryl – RJ, Connor

Steven

Kenny

Table of Contents

List of Figures	xiii
List of Tables.....	xxi
Preface	xxiii
Acknowledgements	xxv
About the Author.....	xxvii
1 Electronic Manufacturing and the Integrated Circuit.....	1
1 — MICROELECTRONICS AND THE TRANSISTOR.....	1
1.1 — The Integrated Circuit and Moore’s Law (2-5).....	1
1.2 — Electronics Manufacturing and the Technology Drivers.....	3
1.3 — A Technology Driver—The Integrated Circuit.....	8
1.4 — The International Roadmap for Semiconductors (ITRS)	10
2 Integrated Circuit Manufacturing: A Technology Resource... 	15
2 — IC MANUFACTURING TECHNOLOGIES	15
2.1 — Overview of the IC Manufacturing Processes.....	15
2.2 — The Manufacturing Environment	17
2.3 — The Photolithographic Process.....	20
2.4 — IC Methodologies and Packaging, Assembly, Interconnections	28
3 Packaging the IC—Single Chip Packaging	31
3 — THE IC PACKAGE.....	31
3.1 — Trends in IC Packaging.....	32
3.2 — Area Array Packages—PGA, BGA	36
3.3 — BGA Surface Mount Assembly.....	41
3.4 — BGA Attributes	42
3.5 — BGA Concerns	42
3.6 — The Future	43
3.7 — Lead-Free Manufacturing.....	43

4	The Chip Scale Package	47
4	— THE CHIP SCALE PACKAGE, CSP	47
4.1	— Chip Scale Package Manufacturing Technologies	48
4.2	— The μ BGA TM	52
4.3	— Wafer Level Packaging—The WLP	55
4.4	— Reliability Concerns	57
4.5	— Summary	58
5	Multichip Packaging.....	61
5	— MULTICHIP PACKAGING (MCP).....	61
5.1	— MCP Substrate/Package Technologies	62
5.2	— The Hybrid Circuit	62
5.3	— The Multichip Module (MCM)	65
5.4	— 3-D Packaging	67
5.5	— 3-D Packaging and the Flex Circuit	71
5.6	— Die Stacking Using Silicon Thru-Vias	75
5.7	— System in Package (SiP)/System on Package (SoP)	77
5.8	— Summary—Benefits of Multichip Packaging	79
6	Known Good Die (KGD)	81
6	— THE KGD STORY	81
6.1	— The Semiconductor Assembly/Packaging/Test Process.....	81
6.2	— The Bare Die Problem.....	83
6.3	— Addressing the Bare Die Problem—Wafer Lot Acceptance Testing	86
6.4	— Known Good Die (KGD).....	86
6.5	— Wafer Level Burn-in and Test (WLBT).....	90
6.6	— Industry Responsiveness	92
7	Packaging Options—Chip on Board.....	93
7	— DIRECT CHIP ATTACH (DCA) AND CHIP ON BOARD (COB).....	93
7.1	— The COB Process	94
7.2	— Flip Chip On Board (FCOB).....	98
7.3	— Summary	101
8	Chip & Wire Assembly.....	103
8	— CHIP & WIRE ASSEMBLY	103
8.1	— Die/Wire Bonding and Bonder Equipment Development.....	103
8.2	— Impact of the IC on Bonding and Bonder Development	105
8.3	— The Chip and Wire Assembly Process	105

8.4 — Bonding Wire: Au, Al, and Cu.....106
 8.5 — Bonding Methods.....108
 8.6 — Types of Bonds110
 8.7 — The Ball Bonding Process.....110
 8.8 — Wedge Bonding.....111
 8.9 — Obstacles to Quality and Reliable Wire Bonding.....112
 8.10 — Metallurgical Concerns and Surface Finishes.....114
 8.11 — Handling and Storage.....118
 8.12 — Verifying Wire Bonding Quality.....118
 8.13 — Responding to the IC and End Product.....120
 8.14 — Wire Bonding on Organic Substrates, The PBGA and PWB.....125
 8.15 — Summary.....127

9 Tape Automated Bonding—TAB..... 129

9 — BACKGROUND—MINIMOD.....129
 9.1 —Tape Automated Bonding129
 9.2 — The TAB Tape129
 9.3 — TAB Assembly.....134
 9.4 — Reliability Concerns.....138
 9.5 — Areas of Applications.....139
 9.6 — Summary.....140

10 Flip Chip—The Bumping Processes..... 143

10 — BACKGROUND143
 10.1 — IBM’s Flip Chip Transistor.....143
 10.2 — Wafer Bumping.....147
 10.3 — Bump Deposition Processes.....150
 10.4 — Comparing Flip Chip Solder Bumping Processes.....160
 10.5 — Polymer/Bumps.....161
 10.6 — Stud/Ball Bumping.....163
 10.7 — Trends in Bumping Technology.....165

11 Flip Chip Assembly..... 169

11 — BASIC FLIP CHIP ASSEMBLY169
 11.1 — Flip Chip Bonding Processes170
 11.2 — The Solder Reflow Process171
 11.3 — Flip Chip Solder Joint Reliability.....173
 11.4 — Reliability and Lead-Free Solders.....182
 11.5 — Solder Reflow Attach: Comments, Concerns.....183
 11.6 — Alternative Flip Chip Bonding Methods.....183
 11.7 — Adhesive Flip Chip Attachment.....184

11.8 — Adhesive Bumps	188
11.9 — Summary: Advantages of Flip Chip as a First Level Interconnect....	189
12 HDI Substrate Manufacturing Technologies: Thin Film Technology.....	193
12 — HIGH DENSITY PACKAGE/SUBSTRATE MANUFACTURING TECHNOLOGIES.....	193
12.1 — Thin Film Technology.....	193
12.2 — The Patterning Process.....	195
12.3 — Processing an HDI Substrate Interconnect	200
12.4 — Thin Film Materials.....	202
12.5 — Alternative Thin Film Processes for MCP Applications	212
12.6 — High Density Interconnects—Cost and Yield Considerations	218
13 HDI Substrate Manufacturing Technologies: Thick Film Technology.....	221
13 — THICK FILM TECHNOLOGY.....	221
13.1 — The Thick Film Process	221
13.2 — The Patterning Process.....	222
13.3 — Thick Film Screen Printing and MCM-C/HDI.....	227
13.4 — Advanced Thick Film Patterning Processes	229
14 HDI Substrate Manufacturing Technologies: Cofired Ceramic.....	233
14 — THE COFIRED CERAMIC TAPE TECHNOLOGY.....	233
14.1 — IBM's Multilayer Interconnect (MLI) Packaging Program	234
14.2 — The Co-fired Ceramic Technology	236
14.3 — The Cofired Ceramic Tape Process.....	237
14.4 — High Temperature Cofired Ceramic HTCC	237
14.5 — Low Temperature Co-fired Ceramic LTCC	238
14.6 — Comparing Thick Film, HTCC and LTCC	239
14.7 — Advanced LTCC Processes.....	241
14.8 — Summary Co-fired Ceramic Process Technologies.....	243
15 Substrate Manufacturing Technologies: Organic Packages and Interconnect Substrate.....	245
15 — THE LEVEL 2.0 PRINTED WIRING BOARD.....	245
15.1 — Overview of Conventional MLB Processing	247
15.2 —The PBGA and the MCM-L.....	248

15.3 — Impact of the IC on Packaging and Interconnect Technology	249
15.4 — Vias and HDI	251
15.5 — IBM’s SLC and HDI PWB Build Up Technology (BUT)	253
15.6 — Current Status Microvia HDI PWBs.....	256
15.7 — Enhancing HDI PWBs—Embedded Passives	257
15.8 —Technology Status.....	259
Acronymns and Definitions	261
Microelectronics Glossary.....	265
Index	289

List of Figures

Figure 1-1. Moore’s Law	2
Figure 1-2. The Electronic Manufacturing Process	4
Figure 1-3(a). Single Chip Packaging	5
Figure 1-3(b). Multichip Packaging	5
Figure 1-3(c). Chip On Board.....	6
Figure 1-4(a). Chip & Wire	6
Figure 1-4(b). TAB.....	6
Figure 1-4(c). Flip Chip.....	7
Figure 1-5. Printed Circuit Board (PCB) or Printed Wiring Board Assembly (PWBA).....	7
Figure 1-6. IC circa 1970, Single Level Al Metallization \approx 20 Micrometers Minimum Line Width.....	8
Figure 1-7(a). IC circa 2000, Multilevel Metallization.....	9
Figure 1-7(b). SEM Photomicrograph Multilevel Copper Interconnect, Minimum Line Width \approx 2 micrometers.....	9
Figure 1-8(a). Peripheral and Area Array I/O formats	12
Figure 1-8(b). I/O Capabilities: Peripheral Format vs. Area Array	13
Figure 1-9. Area Array Packages—BGAs	14
Figure 2-1. A 300 mm (12") and 200 mm (8") Diameter Silicon Wafer	16
Figure 2-2. Schematic Cross-Section of a Si Integrated Circuit	17
Figure 2-3. A Class 1 Cluster Cell within a Class 10 Cleanroom.....	19
Figure 2-4. Robotic Wafer Handling	19
Figure 2-5. Si Wafer Fab, The Front End Processes.....	20
Figure 2-6. The Basic Pattern Transfer Process.....	21
Figure 2-7(a). An Array Photomask	22
Figure 2-7(b). A Reticle.....	23
Figure 2-8. Deposition of Liquid Photoresist by Spinning	24
Figure 2-9. Positive and Negative Acting Photoresist	25
Figure 2-10. The Basic Exposure System.....	26
Figure 2-11. (a) Contact Printer; (b) Proximity Printer.....	26
Figure 2-12. Projection Printer	27
Figure 2-13. The Wafer Stepper Projection System	28
Figure 2-14. The Step and Scan Projection System.....	28
Figure 3-1. Transistor and an Early IC Package (TO-5 Outline)	31
Figure 3-2. IC Package History and Trends.....	32
Figure 3-3(a). Ceramic and Plastic Dual Inline Packages	33
Figure 3-3(b). PCB with Through-Hole Solder Attached DIPs.....	33
Figure 3-4(a). Small Outline IC Packages (SOIC)	34
Figure 3-4(b). PCB with Surface Mounted Components.....	35

Figure 3-5. Plastic Quad Flat Pack, PQFP	35
Figure 3-6. Peripheral leaded Package vs. Area Array Package	36
Figure 3-7. The Pin Grid Array Package (PGA)	36
Figure 3-8(a). BGA Package	37
Figure 3-8(b). BGA—Typical Bump Diameters And Pitch	37
Figure 3-9. Ceramic BGA Configurations	38
Figure 3-10. Ceramic BGA, Ceramic Column BGA, Pad BGA	38
Figure 3-11. Intel’s Pentium 4 in Plastic BGA	39
Figure 3-12. PBGA Configurations with Rigid Laminate	39
Figure 3-13. Schematic Flip Chip in Package (FCIP) PBGA	40
Figure 3-14. Tape BGA Configurations	41
Figure 3-15. CBGA, PBGA, TBGA	41
Figure 4-1. BGA vs. CSP	47
Figure 4-2. CSP Packages	48
Figure 4-3(a). Lead Frame Based CSP (Small Outline No-Leads, SON)	49
Figure 4-3(b). Laminate-Based CSP	49
Figure 4-3(c). Tape Based CSP	50
Figure 4-4. The CSP Loop	50
Figure 4-5. Schematic of CSP on Rigid Organic Substrate	51
Figure 4-6(a). Embedded CSP	51
Figure 4-6(b). Metallurgical Cross-Section Embedded CSP	52
Figure 4-7(a). Chip & Wire Bonded μ BGA™ (Face-Up)	52
Figure 4-7(b). The μ BGA™ Tape Lead Bonded Face-Down	53
Figure 4-8. μ BGA™ “Interposer” Tape Format and a Singulated CSP	53
Figure 4-9. μ BGA™ Lead Bonding Assembly Process	54
Figure 4-10. μ BGA™ Lead Bonding Die Attach	54
Figure 4-11. μ BGA™ Structured Compliancy	55
Figure 4-12. The UltraCSP® Process	56
Figure 4-13. WL-CSP	56
Figure 4-14. The ShellCase CSP	57
Figure 4-15. Flip Chip International’s <i>UltraCSP</i> ® with Polymer Collar	58
Figure 5-1. Multichip vs. Single Chip Packaging	61
Figure 5-2. Hybrid Circuit with Transistors and Diodes (Circa 1960s)	63
Figure 5-3. Multiple ICs on Multilevel Thick Film Conductor Pattern (Circa early 1980s)	64
Figure 5-4. RF/Microwave Hybrid Circuit	64
Figure 5-5(a). MCM-D (mounted on PWB)	65
Figure 5-5(b). MCM-C Coffered Ceramic Package	66
Figure 5-5(c). Laminate MCM-L in Molded BGA Package. Top—Molded Package; Left—Wire Bonded ICs; Right—Bottom of Package	66
Figure 5-6. Earliest 3-D Packaging: The RCA Micromodule	67
Figure 5-7. 3-D IC Stacking Options	68
Figure 5-8. Stacked TSOPs	68
Figure 5-9. (a) Schematic 3-D Memory Cube; (b) TI’s 3-D Memory Cube	69
Figure 5-10(a). Wire Bonded Stacked Die	69

Figure 5-10(b). 2 Die Stack Flip Chip/Wire Bonded.....	70
Figure 5-11. A 2 Die Stacking/Package Process Flow	70
Figure 5-12. 3 Die Stack.....	71
Figure 5-13. SEM of a 4 Stacked Die Assembly with 2 Spacers.....	71
Figure 5-14. Various Stacked Die Configurations.....	72
Figure 5-15. Folded Flex: Hearing Aid Application.....	72
Figure 5-16. Folded Flex Stacked Packages.....	73
Figure 5-17(a). Flex inner layers with Packaged and Unpackaged Components	73
Figure 5-17(b). Finished Cube Showing Inner Layer Interconnections	73
Figure 5-18. (a) Single Chip Neo-Stack™ inner layer; (b) Multichip Inner Layer.....	74
Figure 5-18(c). 19-Layer Smart Flash Stack including Two Neo-Stack™ Layers	74
Figure 5-19(a). Vertical Integration Silicon Through-Via Die-to-Die Stacking Process.....	76
Figure 5-19(b). Cu filled Silicon Through Vias	76
Figure 5-20. Schematic Cross-Section of Vertically Interconnected Stacked Die	77
Figure 5-21. MCM vs. SiP vs. SoP.....	78
Figure 5-22. Cost/Benefits SiP/SoP vs. SoC.....	79
Figure 6-1. (a) IC Wafer on Film Frame; (b) Wafer Sawing.....	82
Figure 6-2. Waffle Pack, Gel-Pak®, Tape, Film Frame	82
Figure 6-3. IC Plastic Encapsulated Package Process	83
Figure 6-4. MCP Assembly/Test Process Flow	84
Figure 6-5. Multichip Assembly/Electrical Yield vs. Electrical Yield of Die	85
Figure 6-6. The DiePak Die Carrier.....	87
Figure 6-7. Die Flow for Package Device and KGD Die in Temporary Carrier.....	88
Figure 6-8. KGD Testing—Options 2, 3, 4.....	89
Figure 6-9. Cost/Reliability Tradeoffs.....	90
Figure 6-10. Wafer Level Burn-in and Test.....	91
Figure 7-1. (left) Chip on Board Assembly; (right) MCM-L.....	93
Figure 7-2. SMT/COB Assembly	94
Figure 7-3(a). COB Assembly: Die Attach, Wire Bonding, Encapsulation (Glob Top).....	95
Figure 7-3. (b) Wedge Bonding on PWB; (c) Ball Bonding on PWB.....	95
Figure 7-4. Assemblies Before and After Glob Top Encapsulation.....	96
Figure 7-5. SMT/COB Process Flow.....	98
Figure 7-6. Flip Chip/SMT Assembly Process	99
Figure 7-7. SMT/Flip Chip On Board, FCOB	99
Figure 7-8. Comparing QFP, TAB, COB, Flip Chip Footprint on PWB.....	100
Figure 8-1. Classic Wedge Wire Bond	103
Figure 8-2. Classic Wire Ball Bond.....	105
Figure 8-3. IC Assembly Process for PEMs	106
Figure 8-4. Al Wire Bonding on Power Hybrid.....	108

Figure 8-5. Metallurgical Cross Sections of Au and Cu Ball Bonds on Al with Data on Growth Rates at Elevated Temperatures	109
Figure 8-6. Bonding Tools—Capillary and Wedge Bonding Tools	110
Figure 8-7. SEM Au Ball Bond and Al Wedge Bond	111
Figure 8-8. The Ball Bonding Process	112
Figure 8-9. The Wedge Bonding Process	113
Figure 8-10. SEM—Thick Film and EDAX Analysis	116
Figure 8-11. Wire Bonding on Screen Printed Thick Film	116
Figure 8-12. Schematic Ball Shear (left) and Wire Pull Testing (right)	118
Figure 8-13. Wire Bonding Failure Modes/Sites	120
Figure 8-14(a). Two and Three Staggered Row I/O Pad Configurations	121
Figure 8-14(b). 3 Staggered Rows of Bond Pads	122
Figure 8-15. Capillary Re-Design for Fine Pitch Applications	122
Figure 8-16. Fine Pitch Ball Bonding	123
Figure 8-17. PBGA Showing Fan Out of Package Pads and Long Loop Wire Bonds	123
Figure 8-18. No Sweep Encapsulant	124
Figure 8-19. High Density Fine Pitch Wire Bonding with Insulated Wires	124
Figure 8-20. Wire Bonding Responding to Changing Packaging Technologies	125
Figure 8-21. Bond Pad “Cupping” on “Soft” Substrate	127
Figure 9-1. Schematic of a Single Frame TAB Assembly	130
Figure 9-2. Microprocessor IC TAB Tape—35mm Tape	131
Figure 9-3. Close-up of TAB Tape (70 mm) for Very High I/O Count IC	131
Figure 9-4. Types of TAB Tapes	132
Figure 9-5. Tape Layout with Annular Ring	133
Figure 9-6. Excised TAB Assembly in Carrier for Testing	133
Figure 9-7(a). Schematic Bumped Die TAB	134
Figure 9-7(b). Bumped Tape TAB	135
Figure 9-7(c). TAB Lead on Al Pad	135
Figure 9-8. TAB Inner Lead Bonding Process	136
Figure 9-9. TAB Package/Substrate Attachment Options	137
Figure 9-10. Face Up and Flip TAB Bonding	137
Figure 9-11. TAB Failure Sites	138
Figure 9-12. Microprocessor Module (~5"x5") with all TAB Device Assembly ...	140
Figure 10-1. (a) IBM’s Flip Chip Transistor; (b) Multichip Transistor Assembly	144
Figure 10-2. IC with Bumps Directly on Bond Pads	144
Figure 10-3. IC I/O Pad Formats: (L to R) Dual Row Peripheral, Peripheral + Partial, Area Array	145
Figure 10-4(a). Direct Bump on Pad	145
Figure 10-4(b). Schematic Redistribution Layer (RDL)	146
Figure 10-4(c). Schematic of Relocated Pad and Bump	146
Figure 10-4(d). SDRAM Flip Chip with Redistributed Bond Pads	146
Figure 10-5(a). Al Pad as Received	150

Figure 10-5(b). Al Pad after Electroless Ni/Immersion Au Plating (5 microns thick).....	150
Figure 10-6. Ball Placement by Vacuum Process.....	151
Figure 10-7(a). The Evaporation Bumping Process (C-4).....	152
Figure 10-7(b). Schematic of C-4 Evaporated Bump Before and After Reflow.....	153
Figure 10-7(c). Solder Dammed Substrate Pad (C-4).....	153
Figure 10-8. The Electroplated Solder Bumping Process.....	154
Figure 10-9. Schematic Cross-section of Bump Site Pre-Plating and AS-Plated Bump.....	155
Figure 10-10. SEM Electroplated Cu Bumps.....	155
Figure 10-11. Electroplated Au Bumps.....	156
Figure 10-12(a). Wafer Bumping Process Using Stencil Printing.....	157
Figure 10-12(b). Bumping by Stencil Printing.....	157
Figure 10-13(a). C4NP Mold with Cavities Corresponding to Bump Locations....	158
Figure 10-13(b). Molten Solder Filling of Mold Cavities.....	158
Figure 10-13(c). Molten Solder Bump Transfer to Wafer.....	158
Figure 10-14. Continuous Mode Solder Jet Technology.....	159
Figure 10-15. (a) Schematic Cross-section of NiAu Bump; (b) 20 μ m Ni-Au Bump.....	160
Figure 10-16. Stencil Printed Conductive Epoxy Bump (75 μ m).....	162
Figure 10-17. Elastomeric Bumps.....	163
Figure 10-18. Au Stud Bumps as Bonded and After Coining.....	164
Figure 10-19. Coined Stud Bumps As Bonded.....	164
Figure 10-20. Stacked and Area Array Stud Bumps.....	165
Figure 11-1. (right) Manual Flip Chip Aligner Bonder; (left) Schematic of Bi-directional Viewing of Die and Package/Substrate Footprint.....	169
Figure 11-2. Solder Reflow Options.....	171
Figure 11-3. Flip Chip Solder Reflow Process.....	172
Figure 11-4. Solder Reflow and Self-Alignment.....	172
Figure 11-5. SMT/Flip Chip Assembly.....	173
Figure 11-6(a). Schematic of a FCOB Solder Joint Fatigue Failure.....	174
Figure 11-6(b). Metallurgical Cross-Section of Solder Fatigue Cracking in Eutectic SnPb.....	175
Figure 11-7. CTE Values for Various Microelectronic Packaging Materials.....	175
Figure 11-8. Flip Chip Assembly on Organic Substrate (FCOB).....	176
Figure 11-9. Fatigue Life vs. Substrate CTE; TC/ 0–100°C.....	177
Figure 11-10. Flip Chip with Underfill.....	178
Figure 11-11. (a) Distance From Neutral Point (DNP); (b) Von-Mises Strain at Each Bump Location with/without Underfill (IBM).....	178
Figure 11-12. Micro Moire Pattern Analysis of FCOB With/Without Underfill....	179
Figure 11-13. (a) Underfill Dispensing and Capillary Flow; (b) No Flow Underfill; (c) Wafer Level Underfill Process.....	180
Figure 11-14. Flip Chip Isotropic Adhesive Attachment.....	185
Figure 11-15. (a) Stencil Printed Epoxy; (b) Epoxy Dipped Stud Bump; (c) Cross-section Isotropic Epoxy Attached.....	186
Figure 11-16. Anisotropic Conductive Adhesive Attach.....	186

Figure 11-17. Non-conductive Adhesive FC Bonding Contact Resistance vs. Applied Force	187
Figure 11-18. Conductive Polymer Bumps and Attachment	189
Figure 12-1. Thin Film Cleanroom.....	194
Figure 12-2. Subtractive Etch and Selective Plate Up Patterning Processes	195
Figure 12-3. Thin Film Process for WL-CSP (Ultra CSP®)	196
Figure 12-4. Dry Film Lamination and Patterning.....	198
Figure 12-5. (Left) Dry Film Applied Over Previously Patterned Structure; (Right) Substrate Vias or Holes.....	198
Figure 12-6. Electrodeposited Resist: Patterned for Selective Plate-up of 25um Lines Over Previously Patterned 45um Thick 100um Wide Feature	199
Figure 12-7. Subtractive Etch Process; The “Etch Factor”	202
Figure 12-8. Planarization of a Deposited Dielectric	205
Figure 12-9. Photodefiable vs. Photosensitive (+/-) Via Patterning	206
Figure 12-10. Achievable Via Diameters Using Laser and Photo-Patterning	207
Figure 12-11. Metallurgical Cross-Section Thin Film Multilayer Interconnect on Ceramic Substrate.....	208
Figure 12-12. Thin Film Interconnects on Co-fired Ceramic Substrate.....	209
Figure 12-13. Thin Film Multilayer Interconnect on PWB (MCM-L/D)	209
Figure 12-14. Si Substrate Supporting Multilevel Thin Film Interconnect for MCM	210
Figure 12-15. Schematic Cross-Section of a Si Substrate with Embedded Active and Passive Devices.....	211
Figure 12-16. DRAM Chips Flip Chip Assembled on Electrically Tested ASICs	211
Figure 12-17. GE HDI “Chips First” MCM	212
Figure 12-18. The “Chips First” (GE HDI) MCM Process Flow	213
Figure 12-19. GE HDI MCM and SMT Printed Circuit Board Assembly.....	213
Figure 12-20. The Low Cost GE HDI or Embedded Chip Build Up (ECBU) Process.....	214
Figure 12-21(a). An ECBU MCM with Embedded Active and Passives.....	215
Figure 12-21(b). An ECBU MCM with Embedded Actives and Passives and Package Devices and Discrete Passives Mounted on Top Layer.....	215
Figure 12-22. The Intel BBUL Process for Microprocessors	216
Figure 12-23. Intel’s Current Microprocessor Package and the BBUL	217
Figure 12-24. Intel’s Multichip BBUL	217
Figure 12-25. Substrate Size/Yield and Defect Density	219
Figure 13-1. The Multilayer Thick Film Process Sequence.....	222
Figure 13-2(a). Photo-Patterned Emulsion (2 mils l/s) on 360 SS Mesh.....	224
Figure 13-2(b). Fully Patterned Screen	225
Figure 13-3. Screen Printing Process.....	225
Figure 13-4. Manual Screen Printer.....	226
Figure 13-5. Thick Film Printing Variables Requiring Monitoring.....	226
Figure 13-6. Automatic Thick Film Screen Printer	227
Figure 13-7. Screen Printed Thick Film Au Conductor trace	228

Figure 13-8(a). Thick Film Multilayer Interconnect Board (MIB).....	228
Figure 13-8(b). Cofired Ceramic MIBs Populated with Ceramic Chip Carrier Packages	229
Figure 13-9. Diffusion Patterning™ Process	230
Figure 13-10. Dupont Fodel® Photosensitive Thick Film Paste Processing	231
Figure 13-11(a). Photo-Patterned 50 um Via in Thick Film Dielectric	231
Figure 13-11(b). Photo-Patterned Thick Film Au Conductor Traces; Left: 28 um lines, 22 um spaces; Right: 50 um lines, 4.5 um thick	232
Figure 14-1. Patent on Cofired Ceramic Manufacture Issued to Harold W. Stetson, RCA	233
Figure 14-2(a). IBM Thermal Conduction Module (TCM).....	234
Figure 14-2(b). Cross-Section of TCM Ceramic Substrate Interconnect	235
Figure 14-3(a). Next Generation TCM	235
Figure 14-3(b). A Cofired Ceramic Package with Thin Film Signal Layers and Top Layer Metallization	236
Figure 14-4. Unfired (“Green”) Ceramic Tape	236
Figure 14-5. Cofired Ceramic Optional Instruction Features (LTCC).....	237
Figure 14-6. The Cofired Ceramic Tape Process.....	238
Figure 14-7(a). HTCC Hermetic Single and Multichip Packages	239
Figure 14-7(b). HTCC Multilayer Interconnect Board with Select Areas for Hermetic Sealing	239
Figure 14-8. LTCC Multichip Packages	240
Figure 14-9. LTCC-M, A Constrained Cofired Ceramic Tape Process.....	242
Figure 14-10. Large Area Panel (7"x 11") Using Heralock™ Self-Constrained LTCC Tape.....	243
Figure 15-1(a). Multilayer PWB with Plated-Through Holes	246
Figure 15-1(b). Plated Through-Hole Via	246
Figure 15-2. Inner Layer Patterning Process Sequence	248
Figure 15-3(a). Schematic Plastic BGA	249
Figure 15-3(b). PBGAs in Strip Format and After Epoxy Molding/Singulation... ..	249
Figure 15-4(a). Unpopulated MCM-L Substrate	250
Figure 15-4(b). MCM-L—Multichip Module with Laminate Substrate	250
Figure 15-5. Through-Hole, Blind, and Buried Vias	252
Figure 15-6. Effect of Via Type on Board Size	252
Figure 15-7. Methods of Via Generation	253
Figure 15-8(a). Schematic IBM’s Surface Laminar Circuit-SLC BGA	254
Figure 15-8(b). Cross-section SLC Flip Chip Package	254
Figure 15-9. Single Chip SLC/BUT PBGA.....	254
Figure 15-10. Key Feature Dimensions for the HDI PWB.....	255
Figure 15-11. The HDBU and Super HDBU	256
Figure 15-12. Cross-section Super-HDBU 2–3–2 PWB.....	256
Figure 15-13. Multilayer and Microvia PWB Projections	257
Figure 15-14. Cell Phone Key Features and Component Count	257
Figure 15-15. Embedded Discrete Capacitor	258
Figure 15-16. Discrete vs. Embedded Planar Decoupling Capacitor.....	259

List of Tables

Table 1-1. Overall IC Characteristics (ITRS Technology Roadmap (ITRS 2005))	11
Table 1-2. Single Chip Pin Count (ITRS 2005)	11
Table 2-1. Cleanroom Classifications [US FED STD 209E Cleanroom Standards]	18
Table 2-2. Comparison of Positive and Negative Resists	25
Table 5-1. Comparing DIP, SMT, MCP at System Level (<i>Courtesy Hughes Aircraft</i>)	62
Table 5-2. Advantages of System on Package vs. System On Chip	78
Table 7-1. Encapsulants for COB	97
Table 7-2. COB vs. FCOB/WLP	100
Table 8-1. Eutectic vs. Adhesive Bonding	107
Table 8-2. Material Properties of Al, Cu, and Au Wire	107
Table 8-3(a). Advantages/Disadvantages of Thermocompression Bonding	109
Table 8-3(b). Advantages/Disadvantages of Ultrasonic Bonding	109
Table 8-3(c). Advantages/Disadvantages of Thermosonic Bonding	110
Table 8-4. Sources of Contamination that Lead to Poor Quality Bonds	114
Table 8-5. Metallurgical Compatibility of Wire bonding Materials	115
Table 8-6(a). Au Wire Destructive Pull Test Criteria	119
Table 8-6(b). Al Wire Destructive Pull Test Criteria	119
Table 9-1. Key Elements of a TAB Assembly	130
Table 9-2. Comparing Tape Options	133
Table 9-3. Comparison TAB Inner Lead Bonding Techniques	138
Table 10-1. Reflow Temperatures for Common Solder Bump Materials	147
Table 10-2. Typical Bump Materials and Favored UBM	149
Table 10-3. Comparing Wafer Bumping Processes	161
Table 11-1. Materials Properties of Some Organic Substrates	176
Table 11-2. Lead and Lead-Free Solders Performance on HTS and HTOL Reliability Screening	183
Table 11-3. Reliability Screening Tests for Solder Bumped FC/WLP	184
Table 12-1. Thin Film Process Capability	194
Table 12-2. Typical Properties of Spin on Liquid Resist	197
Table 12-3. Dry Film Photoresist Properties	197

Table 12-4. Electrodeposited Photoresist Properties.....	199
Table 12-5. Mask Aligner vs. 1X Stepper.....	200
Table 12-6. Conductor Metals	203
Table 12-7. Metals and Their Function (<i>Courtesy Advanced Technical Ceramics</i>)	204
Table 12-8. Material Properties for Polyimide and BCB	205
Table 12-9. Thermal Properties of Select Inorganic Materials	208
Table 12-10. Patterning Requirements for Various Package/Substrate Interconnects	219
Table 13-1. Most Common Thick Film Formulations	223
Table 14-1. Cofired Ceramic Materials and Properties.....	240
Table 14-2. Advantages/Disadvantages Thick Film, HTCC, LTCC.....	241
Table 15-1. Typical Electrical Properties of Some Laminate Materials	247
Table 15-2. Typical Thermal Properties of Some Laminate Materials	247

Preface

The integrated circuit with each new generation has been characterized by increasing functionality. In the 1980's Very Large Scale Integrated Circuits (VLSIC) began to emerge with transistor counts approaching one million plus per chip! The IC package quickly became more than a "chip carrier". Now the packaging had to address the electrical, mechanical and thermal requirements of the IC, and had to do so cost-effectively. A package costing more than the chip was not an option. In addition, the demands of the marketplace for product that was "smaller, better and cheaper" came into play.

As a result the late '80s saw paradigm shifts in IC packages and packaging options. Area array packages, in particular, the Ball Grid Array (BGA) began to emerge that more effectively addressed increasing chip I/O count. Ceramic packaging for high performance circuits (microprocessors digital signal processors) gave way to organic based packages, the plastic BGA (PBGA), offering a more favorable solution to package cost. And the hybrid circuit suddenly became a multichip module!

Over the past 15 years the author has developed and presented professional development courses at various technical symposia as well as on-site at semiconductor, component and equipment manufacturers and materials suppliers facilities. The courses have covered topics that make up the electronic manufacturing arena focusing on packaging and assembly of the integrated circuit.

This book evolved from these courses and discusses the many changes that have taken place not only with the physical package itself but also the currently available packaging options and assembly technologies. It is intended to serve as an *introduction* to IC packaging and assembly providing sufficient coverage to afford a working knowledge of the basic concepts and technologies. The book is intended for personnel new to the industry and, those indirectly involved in electronics manufacturing such as upper management, quality assurance, procurement, marketing and sales, and equipment manufacturers and material suppliers. For those directly involved the book can serve as a useful *overview* of new and emerging technologies.

The First Chapter is discussion of electronic manufacturing that basically describes the packaging and assembly of the integrated circuit. It identifies the various levels of microelectronic assembly, i.e., Level 1.0 interconnects – chip to package and Level 2.0 – chip or package to a substrate board and the packaging options, – single chip, multichip and chip on board.

The Second Chapter briefly reviews the integrated circuit manufacturing process and the *applicability* of much of the procedures and practices to IC packaging and assembly. It highlights the significance of a cleanroom operating environment and the photolithographic process in particular, as a model for implementing a proven high yield cost effective manufacturing technology.

Subsequent Chapters 3 and 4, discuss the trends in the IC package, the Chip Scale Package, and Wafer Level Packaging. Chapter 5 covers Multichip Packaging and the various sub-classifications – the hybrid circuit, the multichip module, System

in Package, System on Packaging and the rapidly developing 3-D Packaging that includes stacking of both multiple die and packages.

Working with bare die as opposed to package devices is discussed in Chapter 6 and covers the subject of Known Good Die or KGD. It presents the concerns associated with bare die and multichip applications and the problem related to the lack of sufficient electrical testing of unpackaged die to insure the device meeting full electrical specifications. Various approaches to resolving this problem and providing for Known Good Die are discussed.

The assembly of a bare die onto an organic board, Chip on Board (COB) is covered in Chapter 7. Implementation and incorporation into Surface Mount Assembly lines and concerns are included. A “packageless packaging” approach makes it a viable packaging option offering both increased component density and an enhanced reliability at the Level 2.0 printed circuit board (PCB) assembly.

The Level 1.0 interconnect technologies are covered in subsequent chapters, C&W Assembly in Chapter 8, TAB in Chapter 9, and Flip Chip Bumping and Assembly, Chapter 10 and 11 respectively.

The last four chapters, 12 through 15, cover the manufacturing technologies, namely Thin Film, Thick Film, Cofired Ceramic and the Organic Laminate Technology, for packages – SCP and MCP, and High Density Interconnect (HDI) substrates. The Thin Film process technology is highlighted as the leading technology in meeting the challenges that arise with the packaging and assembly of current and future integrated circuits. It basically emulates the IC manufacturing and therefore has the inherent capability for achieving very fine line conductor circuitry and the high wiring density required for high density interconnects supporting Levels 1.0 and 2.0. The application of the Thin Film Technology to Thick Film, Cofired and Laminate, to further enhance the overall advantages of each is also discussed. Chapter 15 presents a discussion of a combined Thin Film and Laminate process (Build Up Technology, BUT) as a key enabler for Level 2.0 interconnect substrates that adequately accommodates all current and future IC packaging and assembly technologies.

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I was fortunate in having spent my early years in the electronics industry at RCA working on materials and process development supporting the early manufacture of both the transistor and the integrated circuit that followed. I am indebted to my mentor during those early years, the late Arnold Rose, who guided me and provided me the opportunity to become deeply involved in the many process technologies that are still part of IC manufacturing.

Over the years that followed there were many individuals who help expand my areas of expertise and made it possible for me to write this book. There were and are many and to attempt to recognize everyone would be nearly impossible and would add many pages to this book. And I am certain I would be missing many as well. They come from all areas of industry and include: component manufacturers, equipment manufacturers and material suppliers, manufacturer reps and of course, my colleagues in consulting.

There are several however that I must acknowledge since they were particularly helpful in bring this book to fruition. In particular I am extremely thankful to Richard Brown, an industry consultant, author, instructor of professional development courses who provided invaluable insight. I am most grateful for the many discussions, his suggestions and critiques he provided that were so helpful.

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About the Author

A graduate of Fordham University with a BS in Physics Bill has had extensive experience in Microelectronics covering semiconductor processing and assembly, hybrid circuits, and PWB fabrication and assembly. He began his career with RCA Semiconductor Division and subsequently worked for General Electric and Lockheed Electronics. While at RCA he was awarded six U.S. patents covering wafer processing and semiconductor assembly. At General Electric he was a staff engineer and consultant for hybrid circuits and PWB manufacturing.

As Manager of Advanced Development at Lockheed, he was directly responsible for the design, construction, and operation of a state of the art Microelectronic Packaging facility supporting research, development, and manufacture of advanced hybrid circuits and multichip modules.

He became an independent consultant in 1988. His clients have included material suppliers, assembly equipment manufacturers, and component manufacturers.

His consulting activities has included work at NASA Headquarters in Washington D.C. where he provided technical expertise and assistance in developing an Advanced Integrated Circuit Packaging and Assembly Program.

Bill specializes in packaging and assembly, focusing on high density substrate manufacturing, and chip assembly including flip chip and chip scale packaging.

His company offers assistance in technology assessment and implementation, and specializes in technical audits of manufacturing operations directed towards yield improvement and reliability enhancement.

He has developed several educational and training courses which are offered at various national and international symposia and on-site presentations.

He is an active member of IMAPS where he is a Fellow of the Society and Past President of the Garden State Chapter.