

# OVERSAMPLED DELTA-SIGMA MODULATORS

# Oversampled Delta-Sigma Modulators

**Analysis, Applications and Novel Topologies**

by

**Mücahit Kozak**

*University of Rochester, U.S.A.*

and

**İzzet Kale**

*University of Westminster, U.K.*

**KLUWER ACADEMIC PUBLISHERS**

NEW YORK, BOSTON, DORDRECHT, LONDON, MOSCOW

eBook ISBN: 0-306-48728-4  
Print ISBN: 1-4020-7420-4

©2004 Springer Science + Business Media, Inc.

Print ©2003 Kluwer Academic Publishers  
Dordrecht

All rights reserved

No part of this eBook may be reproduced or transmitted in any form or by any means, electronic, mechanical, recording, or otherwise, without written consent from the Publisher

Created in the United States of America

Visit Springer's eBookstore at:  
and the Springer Global Website Online at:

<http://www.ebooks.kluweronline.com>  
<http://www.springeronline.com>

*This book is dedicated to  
Gülnur Kozak, and Sevilay and  
Ismail Kale*

# Contents

Preface	xi
1. INTRODUCTION	1
1.1 AIMS AND MOTIVATIONS	1
1.2 ORIGINAL CONTRIBUTIONS	4
1.3 OUTLINE OF THE RESEARCH MONOGRAPH	5
2. BASIC PRINCIPLES OF DELTA-SIGMA MODULATION	7
2.1 NYQUIST RATE CONVERTERS	8
2.2 QUANTIZATION NOISE	10
2.3 OVERSAMPLING ADVANTAGE	13
2.4 $\Delta\Sigma$ MODULATION	15
2.5 LIMIT CYCLE OSCILLATIONS AND TONES	21
2.5.1 Dithering	21
2.5.2 Chaotic $\Delta\Sigma$ Modulators	23
2.6 HIGHER-ORDER $\Delta\Sigma$ MODULATORS	23
2.6.1 Single-stage Architectures	24
2.6.2 Multi-stage Architectures	25
2.7 MULTI-BIT $\Delta\Sigma$ CONVERTERS	27
2.8 STATE-OF-THE-ART ANALYSIS	28
3. ANALYSIS OF MASH DELTA-SIGMA MODULATORS WITH DC INPUTS	31
3.1 INTRODUCTION	32

3.2	NON-LINEAR DIFFERENCE EQUATIONS	35
3.2.1	First-order $\Delta\Sigma$ Modulator	35
3.2.2	Higher-order MASH $\Delta\Sigma$ Modulator	40
3.3	STATISTICS OF THE QUANTIZER ERROR SEQUENCE	43
3.3.1	Preliminaries	43
3.3.2	First-order $\Delta\Sigma$ Modulator	45
3.3.3	Higher-order MASH $\Delta\Sigma$ Modulator	52
3.4	SIMULATION RESULTS	62
3.5	OUTPUT SPECTRUM	70
3.6	DIGITAL REALIZATION OF IRRATIONAL INITIAL CONDITION	71
3.7	CONCLUSION	74
4.	ANALYSIS OF SINGLE-STAGE DELTA-SIGMA MODULATORS WITH DC INPUTS	79
4.1	MOTIVATION BEHIND THE WORK	79
4.2	UNIFORM QUANTIZER IN THE NO-OVERLOAD REGION	80
4.3	NON-LINEAR DIFFERENCE EQUATIONS	83
4.3.1	Second-order $\Delta\Sigma$ Modulator	83
4.3.2	Higher-order $\Delta\Sigma$ Modulator	86
4.4	NO-OVERLOAD STABILITY CRITERION	95
4.5	SOLUTION TO THE NON-LINEAR DIFFERENCE EQUATION	99
4.6	STATISTICS OF THE QUANTIZER ERROR SEQUENCE	106
4.6.1	Second-order $\Delta\Sigma$ Modulator	107
4.6.2	Higher-order $\Delta\Sigma$ Modulator	108
4.7	FUNDAMENTAL RESULT	109
4.8	SIMULATION RESULTS	109
4.9	OUTPUT SPECTRUM	112
4.10	ERROR-FEEDBACK TOPOLOGY	116
4.11	CONCLUSION	118
5.	FRACTIONAL-N PLL FREQUENCY SYNTHESIZERS	119
5.1	INTRODUCTION	120
5.2	ANALYSIS OF PLLS	121
5.2.1	Small-signal Model	122
5.2.2	Second-order Systems	124
5.2.3	Charge-pump PLL	128
5.3	THE FRACTIONAL-N CONCEPT	131
5.3.1	First Generation Fractional-N PLL Synthesizers	132
5.3.2	Higher-order $\Delta\Sigma$ Modulation for Modulus Control	134
5.4	DESIGN AND SIMULATION OF FRACTIONAL-N PLL FREQUENCY SYNTHESIZERS	138
5.4.1	Linear Model of the Charge-Pump PLL	138
5.4.2	Design Issues	141

5.4.3	Computer Simulation Model	145
5.4.4	Overall Fractional-N PLL Simulation Results	152
5.5	PIPELINED IMPLEMENTATION OF MASH $\Delta\Sigma$ MODULATORS	157
5.6	CONCLUSION	165
6.	TIME-INTERLEAVED DELTA-SIGMA MODULATORS	167
6.1	INTRODUCTION	168
6.2	BLOCK DIGITAL FILTERING APPROACH	170
6.3	TIME-INTERLEAVED $\Delta\Sigma$ MODULATORS WITH REDUCED COMPLEXITY	175
6.4	SIMULATIONS	182
6.5	IMPLEMENTATION ISSUES	184
6.5.1	Finite Op-amp Gain	184
6.5.2	Op-amp dc Offset	185
6.5.3	Mismatch Effects	187
6.5.4	Sampling Clock Jitter	190
6.5.5	Critical Delay Problem	190
6.6	HARDWARE COMPARISON	192
6.7	HIGHER-ORDER TIME-INTERLEAVED $\Delta\Sigma$ MODULATORS	194
6.7.1	Cascaded Integrators with Feed-Forward Summation Topology	195
6.7.2	Cascaded Integrators with Distributed Feedback as well as Feed-forward Branch Topology	199
6.7.3	Simulations	201
6.7.4	Coefficient Mismatches	203
6.8	ZERO-INSERTION INTERPOLATION TIME-INTERLEAVING	206
6.9	FURTHER PRACTICAL ISSUES	215
6.9.1	Sampling Clock Jitter Effects	215
6.9.2	Branch Mismatch Effects	217
6.10	CONCLUSION	218
	References	221

## Preface

The constant scaling of CMOS VLSI technologies has produced orders of magnitude of increase in packing density and operation frequency of the circuits, moving more of the signal processing in to the digital domain. This put increasingly difficult demands on the design of analog-to-digital/digital-to-analog converters, as the partition between analog and digital sub-circuits change. The robustness against circuit non-idealities has made Delta-Sigma modulators one of the best choices for high-resolution data conversion. Despite the fact that Delta-Sigma modulation is a mature subject, there are still many unanswered questions. While a detailed coverage for all these questions in a single text is impossible, an honest effort has been made in this research monograph to address the exact analysis and speed limitations of Delta-Sigma modulators.

Due to the incorporation of a highly non-linear element (the quantizer) in the feedback loop, the exact analysis of Delta-Sigma modulators is a very challenging task. In this text, rigorous analysis of Delta-Sigma modulators (both multi-stage and single-stage) with rational dc inputs and non-zero initial conditions are presented. It is concluded that for a first-order modulator the binary quantizer error exhibits a purely discrete power spectrum and the conventional white noise assumption is strictly violated. Second-order modulators produce the same first-order statistics as those of the white noise, but they still fail to generate an uncorrelated quantizer error sequence. Third-order modulators are capable of complying with the signal-independent white noise assumption provided that an irrational initial condition is invoked on the first accumulator.

It has been well known that Delta-Sigma modulators are non-linear chaotic systems, and two infinitesimally small different initial conditions may result in completely different and divergent outputs. This book presents



the first exact analysis results (to the best knowledge of the authors) that rigorously prove the effectiveness of the initial condition in terms of the modulator tonality performance. The irrational initial condition principle rigorously analyzed here eliminates the need for dithering or chaotic operation in which reduction in the limit cycle oscillations and tones comes with some performance penalties and hardware overhead.

During the development of this research, it has become clear that the elimination of limit cycle oscillations and tones in some applications are of paramount importance. Such a need, for instance, occurs in Fractional-N PLL frequency synthesis applications, which may be used to implement a local oscillator in a wireless transceiver. In Fractional-N PLL applications, the dc input to the modulator poses a significant problem and is responsible for the generation of significant amount of spur signals. In this book, an important application of our novel mathematical analysis in a Fractional-N synthesizer is presented as a solution to cancel spurious signals. The solution is simply to set “1” LSB initial condition on the first accumulator, so that the initial condition resembles an irrational number eliminating unwanted spurious components.

Increased integration capabilities provided by current-state-of-the-art CMOS technologies as well as constant scaling trends encourage analog designers to employ more parallelism in Delta-Sigma based A/D converter designs. In the architecture domain, the research monograph introduces a new method to obtain efficient architectures for time-interleaved Delta-Sigma modulators. Additionally, a novel parallel conversion technique, which we have dubbed as the “Zero-Insertion Time-Interleaving” concept is also proposed. In this approach, the input only needs to be sampled at the operating frequency of the parallel channels. Thus, the high sampling rate input multiplexer involved in the regular Time-Interleaved approach is completely eliminated resulting in further significant reductions in the hardware complexity. Such a multiple channel Delta-Sigma modulator may be very useful for implementing high-resolution converters for wide bandwidth input signals, at the expense of moderate increase in the hardware cost.

This research monograph resulted from a doctoral study completed by the first author at the University of Westminster, London, UK, while working under the supervision of Prof. İzzet Kale.

Mücahit Kozak, İzzet Kale