OVERSAMPLED DELTA-SIGMA MODULATORS

Oversampled Delta-Sigma Modulators

Analysis, Applications and Novel Topologies

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This book is dedicated to
Gülnur Kozak, and Sevilay and
Ismail Kale

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Preface

The constant scaling of CMOS VLSI technologies has produced orders of magnitude of increase in packing density and operation frequency of the circuits, moving more of the signal processing in to the digital domain. This put increasingly difficult demands on the design of analog-to-digital/digital-to-analog converters, as the partition between analog and digital sub-circuits change. The robustness against circuit non-idealities has made Delta-Sigma modulators one of the best choices for high-resolution data conversion. Despite the fact that Delta-Sigma modulation is a mature subject, there are still many unanswered questions. While a detailed coverage for all these questions in a single text is impossible, an honest effort has been made in this research monograph to address the exact analysis and speed limitations of Delta-Sigma modulators.

Due to the incorporation of a highly non-linear element (the quantizer) in the feedback loop, the exact analysis of Delta-Sigma modulators is a very challenging task. In this text, rigorous analysis of Delta-Sigma modulators (both multi-stage and single-stage) with rational dc inputs and non-zero initial conditions are presented. It is concluded that for a first-order modulator the binary quantizer error exhibits a purely discrete power spectrum and the conventional white noise assumption is strictly violated. Second-order modulators produce the same first-order statistics as those of the white noise, but they still fail to generate an uncorrelated quantizer error sequence. Third-order modulators are capable of complying with the signal-independent white noise assumption provided that an irrational initial condition is invoked on the first accumulator.

It has been well known that Delta-Sigma modulators are non-linear chaotic systems, and two infinitesimally small different initial conditions may result in completely different and divergent outputs. This book presents

the first exact analysis results (to the best knowledge of the authors) that rigorously prove the effectiveness of the initial condition in terms of the modulator tonality performance. The irrational initial condition principle rigorously analyzed here eliminates the need for dithering or chaotic operation in which reduction in the limit cycle oscillations and tones comes with some performance penalties and hardware overhead.

During the development of this research, it has become clear that the elimination of limit cycle oscillations and tones in some applications are of paramount importance. Such a need, for instance, occurs in Fractional-N PLL frequency synthesis applications, which may be used to implement a local oscillator in a wireless transceiver. In Fractional-N PLL applications, the dc input to the modulator poses a significant problem and is responsible for the generation of significant amount of spur signals. In this book, an important application of our novel mathematical analysis in a Fractional-N synthesizer is presented as a solution to cancel spurious signals. The solution is simply to set "1" LSB initial condition on the first accumulator, so that the initial condition resembles an irrational number eliminating unwanted spurious components.

Increased integration capabilities provided by current-state-of-the-art CMOS technologies as well as constant scaling trends encourage analog designers to employ more parallelism in Delta-Sigma based A/D converter designs. In the architecture domain, the research monograph introduces a new method to obtain efficient architectures for time-interleaved Delta-Sigma modulators. Additionally, a novel parallel conversion technique, which we have dubbed as the "Zero-Insertion Time-Interleaving" concept is also proposed. In this approach, the input only needs to be sampled at the operating frequency of the parallel channels. Thus, the high sampling rate input multiplexer involved in the regular Time-Interleaved approach is completely eliminated resulting in further significant reductions in the hardware complexity. Such a multiple channel Delta-Sigma modulator may be very useful for implementing high-resolution converters for wide bandwidth input signals, at the expense of moderate increase in the hardware cost.

This research monograph resulted from a doctoral study completed by the first author at the University of Westminster, London, UK, while working under the supervision of Prof. İzzet Kale.

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