DESIGN FOR AT-SPEED TEST, DIAGNOSIS AND MEASUREMENT

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**DESIGN FOR AT-SPEED TEST,
DIAGNOSIS AND MEASUREMENT**

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Foreword

System-on-a-chip (SOC) technology has come to represent various aspects of integrating more and more functionality in a single integrated circuit (IC) and delivering it to the market in the shortest possible time. This ranges from ICs with user-defined logic and embedded memories on one extreme end of an SOC, to a complex graphics controller SOC with an embedded microprocessor, several embedded memories, phase-locked-loops, analog-to-digital converters, digital-to-analog converters, user-defined logic, and other predesigned cores. Despite disagreements on a commonly accepted definition of an SOC, there is a widespread agreement that SOC's represent a major discontinuity with incredible design and test challenges. Now imagine a product built with several such SOC's. Most data communication products are perfect examples of such complex systems.

Many of these design challenges are being met by new hierarchical, block-based design methodologies and corresponding automation tools that include higher-level floorplanners, verification environments, static-timing signoffs, and block-based synthesis. Nonetheless, one of the key problems faced by designers is the manufacturing test, diagnosis and measurement. This continues to be perceived as a back-end problem and is ignored by most electronic design automation (EDA) tool providers. In this age of SOC, the test problem impacts time to market, quality, and overall cost.

What is needed is a total design for testability solution that can provide at-speed test of all embedded blocks and of the chip as a whole. This solution should be able to handle diversity of embedded cores from logic to memory to mixed-signal and their associated fault models. At the chip level, the solution should be able to reduce the test time, provide higher fault coverage, better diagnostics, and reduce the time to market. At the system level, fast time to market requires better tools to perform board-level prototyping and system-level integration. Reliability at a lower cost is also a prime objective for many applications.

It is well known that some of these problems are fundamentally impossible to solve with external testers. It is also generally accepted that a more economical approach to solving these problems is to provide a proper balance between external test and embedded test. Incorporating some of the test functions right on the very chip that is being tested makes an SOC include the tester as a part of that system. Embedded test—if done properly—offers a whole range of advantages for solving test, diagnosis, and debug problems.

This is the first book of its kind to offer practical and proven solutions to product managers, designers, and test engineers for test and diagnosis problems at the silicon level as well as the board and system levels. The basic theme of this book is that embedded test offers significant reductions in design and test engineering efforts, in time to market, and in cost of design and test of chips, boards, and systems.

LogicVision has been at the forefront of the embedded test technology with its continued innovations, automation, and customer successes. This book is an admirable effort by Dr. Benoît Nadeau-Dostie and his colleagues to share the fruits of their success with the design and test community at large. The practical aspects of design for testability explored in this book bring immediate value to its readers. System designers will find the material extremely useful in defining requirements for their chips that can speed up board-level prototyping, and system-level integration and bring up. Embedded test has the added benefit of reducing the extent of diagnostic software that must go on every complex system.

For chip designers, the use of embedded test significantly helps them meet their 99 percent plus fault coverage requirements with small test time and at-speed tests. In addition, designers benefit from help of embedded test in performing silicon debug of their first samples. Finally, the product engineers and test engineers can take full advantage of embedded test by reducing their efforts in the preparation of complex test programs and diagnostics.

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Acknowledgments

Many people contributed to the writing of this book, which required a considerable team effort. I thank all the contributors for their sustained enthusiasm and diligence.

A large team of highly competent engineers was involved in the development and application of the products and capabilities referred to in this book. I gratefully acknowledge all of them for making the embedded test technology robust and easy to use.

We are deeply indebted to all our loyal customers, who have given us the chance to prove and improve the technology. In particular, some companies made special contributions. Nortel provided access to their memory and logic BIST technologies, which constituted the first generation of LogicVision products. Stratus Computers helped us specify and use the first controllers to support multi-cycle paths—a significant milestone in at-speed logic testing—as well as the first controllers to support at-speed interconnect testing. Fujitsu was the main driver and first user of embedded core test technology. Lockheed-Martin contributed to the development of off-the-shelf memory test technology in the context of the US Air Force Rapid Prototyping Program (RASSP). Mitel was the first user of the new embedded test technology developed for analog-to-digital converters. Ericsson provided the motivation for developing the fault insertion feature.

Dr. Vishawani D. Agrawal, Series Editor of Kluwer Academic Publishers, was very helpful in promoting the concept of this book, and I wish to thank him for his support. Carl Harris at Kluwer Academic Publishers also deserves our gratitude. Finally, special thanks to Susan Borton and Diane Lynch for converting the manuscript into a truly professional publication.

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Preface

This book addresses designers, test engineers, and product managers, for whom success depends upon the fast deployment in the market of electronic systems based on complex ICs. The *system* can be the integrated circuit itself (system on a chip) or an arrangement of multiple boards. The complexity of today's chips is not only a function of the number of transistors but also the diversity of embedded functions such as logic, memory, processors, and mixed-signal components.

Product managers will read how the time, resources, and costs associated with test development, manufacture, and life-cycle maintenance of their products can be significantly reduced by designing test, diagnosis, and measurement features in the product. This book provides a complete design flow and analysis of the impact on the design to enable designers to learn how to implement these features in systems. Test engineers will learn how embedded test circuitry can provide superior quality without exceeding the capabilities of their equipment. The book also provides procedures for diagnosing failures and measuring circuit parameters.

The book places special emphasis on at-speed testing. Being able to perform tests, diagnose failures, and make measurements using system clocks offers several benefits. The main benefit is the ability to test the circuit—or subcircuit—under conditions that are as close as possible to normal circuit operation. This factor has a direct impact on the number of chips that are found defective during system operation but still pass all manufacturing and functional tests. At-speed testing can be used for characterization and can also expedite test application time.

Finally, the book addresses the concerns associated with embedded test. One such concern is the perceived inability of embedded test to perform proper diagnosis and the assertion that the technology can be used only to determine whether circuits pass or fail a test. Not only do the technologies described in this book have several levels of diagnostic features, but they can also perform accurate measurements of circuit parameters. Other concern about embedded test relates to the size of the test circuitry and its power consumption. It will be seen that both of these concerns are not significant with the solution described in this book.

The type of information in this book is significantly different from the information provided in other books on Design for Test (DFT) and Built-in Self-Test (BIST), which are fundamental components of embedded test. These books typically present the basic concepts of several potential solutions to the same test problem without providing all the information required to determine the application context and implementation issues. This book emphasizes the issues that the practitioner, designer, or test engineer must understand in order to implement embedded test for a single chip or an entire system. For example, the book addresses the following questions: What are the restrictions put on the design style of the chip and the system? Is there any impact on circuit performance? How are clock skew and other timing issues addressed? How are the tests verified and debugged?

All the technology described in this book has been proven in silicon, is automated, and is integrated with all the other components described. This technology has been used by hundreds of designers and test engineers in major companies, including Cabletron, Cisco Systems, Ericsson, Fujitsu, Hughes, Lockheed-Martin, LSI Logic, National Semiconductor, Nortel Networks, Stratus, and Sun Microsystems. All this is to underscore that everything you read in this book is practically sound and verifiable on real-world chips.

Overview of the Chapters

This book is organized as follows:

Chapter 1, “Technology Overview,” has three main sections. The first section discusses the motivation behind, need for, and advantages of designed-in, or embedded, test. The second section introduces basic concepts of LogicVision’s embedded test solution. The third section provides an overview of all embedded test capabilities.

Chapter 2, “Memory Test and Diagnosis,” describes embedded test technology for memories. Memory BIST is a well-known application and is used to illustrate many of the features common to all LogicVision technologies. For example, all controllers use a common protocol for initialization and results collection. Diagnosis and integration with scan design and logic BIST are other features shared by all embedded test controllers. The BIST described in this chapter facilitates sharing test resources among several memories of the same or different types.

Chapter 3, “Logic Test and Diagnosis,” explains the circuit preparation required to perform an at-speed test of digital logic. Very few design rules other than the conventional scan design rules apply. The second section of this chapter introduces the hardware building blocks that are provided by the automation tools. The various test configurations and diagnostic procedures supported by the test circuitry are described. The last section describes automated solutions for addressing potential timing issues.

Chapter 4, “Embedded Test Design Flow,” describes the three phases of the process of adding embedded test: test insertion in subblocks, preparation of logic blocks, top-level test insertion and integration. In each phase, the flow consists of four steps: Generate, Assemble, Analyze, and Verify. In some cases, a Prep (prepare) step is also needed.

Chapter 5, “Hierarchical Core Test,” is devoted to the handling of embedded cores which are becoming prevalent in the design of large integrated circuits. The embedded test solution described in this book naturally fits the needs of a core-based design methodology. Two situations can arise. In the first situation, the core itself makes use of embedded test. A hierarchy of embedded test controllers can be implemented to test the entire integrated circuit. The second situation concerns legacy cores which are assumed to come with a predetermined test set and require access from the periphery of the integrated circuit. In both situations, great care is taken to ensure that the core and surrounding logic are completely tested.

Chapter 6, “Test and Measurement for PLLs and ADCs,” introduces completely new capabilities that allow designers to accurately measure circuit parameters. The first section explains how the lock range, lock time, loop gain, and jitter of PLLs are measured using embedded test. The second section describes how to test analog-to-digital converters (ADCs) to measure their offset, gain, second and third harmonic distortion, differential non-linearity, and idle channel noise. The benefits of these solutions are explained as well as the design requirements for applying the measurement methods.

Chapter 7, “System Test and Diagnosis,” presents technologies that are used for board and system tests but that are designed in the integrated circuits populating the electronic system. The first section shows how an at-speed test of board interconnect is implemented to detect and diagnose defects escaping conventional low-speed tests. The capability is compatible with existing IEEE 1149.1 standard infrastructure. Another capability built around the standard is fault insertion. This capability is extremely useful for verifying the correct implementation of the system hardware and software components dealing with online error detection, diagnosis, and recovery. A last section covers the test and diagnosis of off-the-shelf memories and their interconnections.

Chapter 8, “System Reuse of Embedded Test,” describes how to use embedded test technology in a board/system manufacturing environment, or even in the field, to provide a completely self-testing, self-diagnosing system. Several architectures are reviewed and commentary on the implications for system design is included. Examples are provided of embedded test access using third-party tools.

A **Glossary** at the end of this book defines terms and acronyms pertaining to embedded test technology.