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Created in the United States of America

To the late Vanja Gustavsson
Mikael Gustavsson

To Ulrica and my family
J Jacob Wikner

To Regina and Diana
N. Nick Tan

CONTENTS

PREFACE

"In the telecommunication era, analog design is not just a matter of isolated self-satisfying circuit tweaking, it is above all a system planning."

Digital radio and high-speed internet access have created a great demand on high-performance data converters. The conventional view of data converters as numerical conversion blocks does not suffice for this kind of communication applications. From a communication system's perspective, the bit error rate (BER) requirement determines the signal-to-noise ratio (SNR) requirement for a given modulation and duplexing scheme. Therefore, when we design data converters for a communication system, frequency-domain measures such as the SNR are of great importance. In theory, any known distortion components in a transmit channel of a communication system can be corrected by measuring it through the use of a pilot signal or during the initialization phase. But in practice, it is difficult to predict the distortions due to the time-varying interference of adjacent channels in most communication systems. Therefore, the distortion and inter-modulation of data converters are of great importance as well. The use of discrete multi-tone (DMT) modulation for digital subscriber line (DSL) and the use of orthogonal frequency division multiplexing (OFDM) for wideband radio further complicate the data converter design in that even the single-tone frequency-domain measures do not suffice.

Most universities teach analog courses as circuit design courses with little interaction with communication or signal processing systems. Most analog designers can only design circuits specified by system engineers without much understanding of the system, and most system engineers have not much knowledge about analog imperfections. This combination usually results in non-optimal system solutions. If analog designers with the system knowledge participate in the system specification and system partitioning, we can really design the optimal system with judicious trade-offs between analog and digital, software and hardware. By realizing the industrial and educational need of analog designers with system knowledge, the Microelectronics Research Center of Ericsson started analog activities with close cooperations with Linköping University in 1995. One of the results is this book.

CMOS data converters for communications addresses analog design for communication systems. It distinguishes itself from other data converter books by emphasizing system-related aspects of data converter designs and frequency-domain performance of data converters. However, this is not a book written by system designers rather than by circuit designers. It therefore also covers circuit designs and implementations of

CMOS data converters, based on measured chips.

CMOS data converters for communications bridges the gap between the communication system requirements and the mixed signal design. It derives data converter requirements from the communication system specifications such as line codes, modulation schemes, and duplexing methods, etc. It also gives examples of relating asymmetrical DSL (ADSL) and wideband ratio systems to the data converter requirements.

CMOS data converters for communications can be used as a reference book by analog circuit designers to understand the data converter requirements for communications. It can also be used by communication system designers to understand the difficulties of certain performance requirements on data converters. This book reflects the authors many year philosophy in both industrial practice and academic education. In the telecommunication era, analog design is not just a matter of isolated self-satisfying circuit tweaking, it is above all a system planning. To prepare analog students for the new challenge, this book can be an excellent resort.

This book consists of 13 chapters.

In chapter 1, we discuss the characterization of data converters with emphasis on frequency-domain measures. It also discusses the multi-tone power ratio (MTPR) measure for DMT or OFDM applications. It is shown that multi-carrier modulations usually have a higher dynamic range requirement on data converters due to the instantaneous summation of many carriers resulting in a large peak to average ratio (PAR).

In chapter 2, we first briefly discuss the fundamentals of digital communication systems and introduce the relevant terminologies such as bit error rate (BER), line codes, modulation schemes, and duplexing methods, etc. Then we derive the minimum data converter requirements as a function of the bit error rate, the line code, and the modulation. The influence of duplexing methods is discussed as well. By considering the transmit and receive power and the background noise/interference power, we also derive the optimum data converter requirements for ADSL and wideband radio systems.

Chapters 3 and 4 are devoted to the overview of data converter architectures. These two chapters cover the most data converter architectures and discuss their suitabilities for communications. Chapter 3 presents an overview of high-performance analog-to-digital converters (ADCs) while chapter 4 presents an overview of high-performance digital-to-analog converters (DACs).

Chapters 5~8 are devoted to analog circuits and circuit techniques before we discuss data converter designs and implementations.

Chapter 5 briefly compares the two existing circuit techniques, the switched-capacitor (SC) and switched-current (SI) technique. Although the SI technique offers the simplicity advantages among others, it is advised to use the SC technique for high-performance ADCs due to the higher dynamic range and lower distortion of SC circuits.

For most ADCs, sample-and-hold (S/H) amplifiers have a great impact on the frequency-domain performance such as the SNR and distortion, especially for sub-sampled

ADC systems where the signal frequency is beyond the Nyquist bandwidth determined by the sampling rate. S/H amplifiers are a special case of multiplying DACs used in pipelined ADCs and a special case of integrators used in oversampling ADCs. Chapter 6 discusses the design and characterization of these functional blocks such as multiplying DACs and integrators.

Chapter 7 discusses the circuit building blocks needed for data converters including operational amplifiers (opamps), comparators, and references, etc. It highlights how to design high-gain high-speed opamps and fast low-power comparators. It also covers common-mode feedback (CMFB) techniques and practical issues such as bandgap reference generation and reference buffering.

Chapter 8 is an extension of chapter 7, focusing on low-voltage building blocks in order to operate analog circuits at a supply voltage of 2.5 V or even lower. It includes low voltage (2.5 V) high-speed opamps, voltage doublers, and high-voltage generators, etc.

Chapters 9~11 deal with ADC designs and implementations.

Chapter 9 is devoted to pipelined ADCs, from architecture to design and implementation. It discusses different pipelining techniques, different coding techniques, digital correction techniques, and digital calibration techniques.

Chapter 10 is about how to increase the speed of ADCs by time-interleaving or parallelism. The major limitation of time-interleaved ADCs is the phase skews in the different channels which introduces distortion. A global S/H circuit at the input would eliminate this limitation but the speed and accuracy would be limited by the opamp used in the S/H circuit. Besides discussions on the conventional methods, it also presents a passive global sampling technique to increase the speed beyond the opamp limitation and reduce the phase skew distortion by 8~10 dB.

Chapter 11 covers oversampling ADCs. It discusses different trade-offs between single-stage and multi-stage architectures, between single-bit and multi-bit quantizers. A design example of a fourth-order oversampling ADC is also presented. It highlights the architecture selection as well as the SC design and implementation.

Chapter 12 discusses the modeling of Nyquist DACs for communications. Through this modeling, it is possible to relate the frequency-domain requirements to actual design parameters and therefore provide a guideline for circuit designers.

Chapter 13 presents the actual design and implementation of a current-steering DAC chipset, including high-speed (> 50 MHz) and ultra-low voltage (1.5 V) chips. Based on the discussed architecture and improved current source matching, it is demonstrated possible to deliver a spurious dynamic range (SFDR) over 75 dBc in standard digital CMOS process and achieve an SFDR over 65 dBc with a single 1.5-V supply.

This book is based on the analog research conducted at the Microelectronics Research Center of Ericsson and at the Linköping University. First we would like to thank Dr. Gunnar Björklund, director of the Microelectronics Research Center for initializing and supporting the analog activities at the research center. We would also like to thank

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Last but not the least, we would like to thank our families for their love, patience, and support.

ABBREVIATIONS AND ACRONYMS

2B1Q	Two Binary 1 Quaternary
ΣΔ	Sigma-Delta
A/D	Analog to Digital
ADC	Analog-to-Digital Converter
ADSL	Asymmetrical digitial subscriber line
AGC	Automatic Gain Control
ASK	Amplitude-Shift Keying
AWGN	Additive White Gaussian Noise
BER	Bit Error Rate
BP	Band pass
BPSK	Binary Phase-Shift Keying
CAP	Carrierless Amplitude Phase (modulation)
CFT	Clock Feedthrough
CNR	Carrier-to-Noise Ratio
CMFB	Common-Mode Feedback
D/A	Digital to Analog
DAC	Digital-to-Analog Converter
DEM	Dynamic Element Matching
DMT	Discrete Multi-Tone
DNL	Differential Non-Linearity
DR	Dynamic Range
DSL	Digital Subscriber Line
EC	Echo Cancellation
ENOB	Effective Number Of Bits
ERB	Effective Resolution Bandwidth
FDD	Frequency-Division Duplexing
FDM	Frequency-Division Multiplexing
FIR	Finite-length Impulse Response
FM	Frequency Modulation
FSK	Freqeuncy-Shift Keying
GMSK	Gaussian Minimum-Shift Keying

GSM	Global System for Mobile Communication
HDSL	High data-rate Digital Subscriber Line
HDTV	High-Definition Television
HP	High Pass
IF	Intermediate Frequency
IIR	Infinite-length Impulse Response
IMD	Inter-Modulation Distortion
INL	Integral Non-Linearity
ISDN	Integrated Service Digital Network
LP	Low Pass
LSB	Least Significant Bit
MDAC	Multiplying Digital-to-Analog Converter
MSB	Most Significant Bit
MTPR	Multi-Tone Power Ratio
OFDM	Orthogonal Frequency Division Multiplexing
Opamp	Operational Amplifier
OSADC	Oversampling Analog-to-Digital Converter
OSDAC	Oversampling Digital-to-Analog Converter
PAM	Phase Amplitude Modulation
PAR	Peak-to-Average Ratio
PCM	Pulse Code Modulation
PGA	Programmable Gain Amplifier
PSD	Power Spectral Density
PSK	Phase-Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase-Shift Keying
RF	Radio Frequency
RSD	Redundant Signed Digit
S/H	Sample-and-Hold
SC	Switched Capacitor
SDD	Space-Division Duplexing
SFDR	Spurious-Free Dynamic Range
SFG	Signal Flow Graph
SI	Switched Current
SNR	Signal-to-Noise Ratio
SNDR	Signal-to-Noise-and-Distortion Ratio
SR	Slew Rate
TDD	Time-Division Duplexing

TDM Time-Division Multplexing
THD Total Harmonic Distortion

VDSL Very high data-rate Digital Subscriber Line

XDSL all/any digital subscriber line