Appendix A
Capacitance–Voltage Measurements

C–V measurements are a powerful tool for the characterisation of thin-film dielectrics and their interfaces with semiconductors. Extensive use of such measurements is made in this work. This appendix describes the principles underlying C–V measurements, and details the analysis used to extract material parameters of interest. For a more thorough discussion of the theoretical basis, the interested reader is referred to the definitive work of Nicollian and Brews [1].

A.1 Principles

A.1.1 The MIS Capacitor

The sample structure used for C–V measurements is the MIS capacitor, shown in Fig. A.1. This structure typically consists of a semiconductor wafer substrate covered on one side with a thin-film dielectric layer, over which is deposited a metal gate contact which defines the device area. The structure is contacted ohmically at the semiconductor rear and at the gate, which form the two electrodes of the capacitor.

C–V measurements of MIS structures probe the variation of the spatially extended charge distribution in the semiconductor (the space-charge region) in response to a time-varying voltage applied to the metal gate. This charge mirrors charges present at the semiconductor–insulator interface and in the insulator itself, as well as in the gate contact, and C–V measurements therefore contain information about the charge centres that give rise to each of these contributions.

The capacitive response of each of these charge components—the free charge in the semiconductor, interface-trapped charge, and insulator charge—possesses a characteristic dependence on the semiconductor surface potential and on the frequency of potential variations. Thus, by measuring the C–V characteristics of a given device across a range of gate bias voltages at both high and low frequencies, the various charge contributions may be distinguished.

L.E. Black, *New Perspectives on Surface Passivation: Understanding the Si–Al_2O_3 Interface*, Springer Theses, DOI 10.1007/978-3-319-32521-7

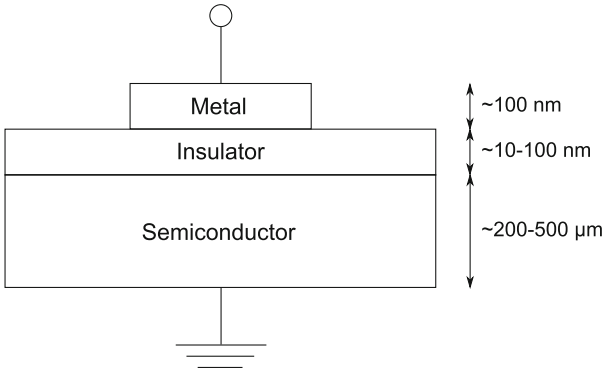

Fig. A.1 Schematic of the MIS structure used in C–V measurements. Typical dimensions are indicated

Furthermore, since the relationship between the semiconductor charge distribution and the gate bias is influenced by the ionised dopant concentration in the semiconductor, as well as the dielectric properties of the insulator layer, C–V measurements also contain information about these device properties. In the following sections we describe how these various parameters influence the measured C–V characteristics, and how they may be systematically extracted from experimental C–V data.

A.1.2 Basic Equations

Figure A.2 shows schematically the energy band diagram of the MIS capacitor under bias, along with the corresponding distribution of the various charges. The semiconductor potential $\phi(x)$ is defined by $q\phi(x) \equiv E_F - E_i(x)$, while the value of $\phi(x)$ in the semiconductor bulk ($x \to \infty$) is called the bulk potential ϕ_b. The gate voltage V_g designates the potential applied to the gate contact with respect to the grounded semiconductor substrate, while ψ_s is the induced potential at the semiconductor surface relative to ϕ_b.

The charge Q_g induced at the metal gate by the applied V_g is balanced by the insulator fixed charge Q_f, interface trapped charge Q_{it}, and semiconductor charge Q_s. Charge neutrality dictates that

$$Q_g(\psi_s) + Q_s(\psi_s) + Q_f + Q_{it}(\psi_s) = 0, \tag{A.1}$$

where the dependence of the various charges on ψ_s has been indicated.

V_g is related to ψ_s and to the charge by

$$V_g = -\frac{Q_s + (1 + x_c/t_i)Q_f + Q_{it}}{C_i/A} + \psi_s + W_{ms}, \tag{A.2}$$

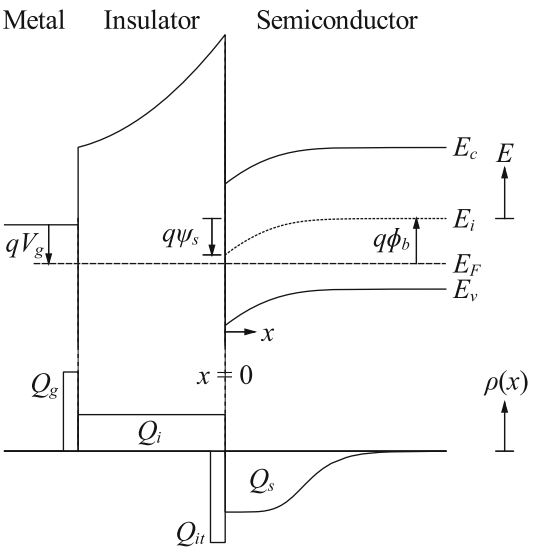

Fig. A.2 Energy band diagram and associated charge distribution ($\rho(x)$) diagram of the (p-type) MIS capacitor under bias (depletion), showing the relationship between the various potentials and charges described in the text. *Arrows* pointing down (*up*) denote positive (*negative*) potentials

where x_c is the location of the insulator charge centroid relative to the semiconductor–insulator interface, C_i is the insulator capacitance, A is the area of the metal gate, and W_{ms} is the work-function difference between the metal gate and the semiconductor bulk. It will be convenient to define a flatband voltage V_{fb}, as the gate voltage corresponding to $\psi_s = 0$. In this case we also have $Q_s = 0$, so that

$$V_{fb} = \frac{(1 + x_c/t_i)Q_f + Q_{it}}{C_i/A} + W_{ms}. \tag{A.3}$$

The small-signal differential capacitance C of the MIS capacitor is defined by

$$C(V_g) \equiv \frac{dQ_g}{dV_g}A. \tag{A.4}$$

Similarly the semiconductor capacitance C_s and interface state capacitance C_{it} are defined by

$$C_s(\psi_s) \equiv -\frac{dQ_s}{d\psi_s}A, \tag{A.5}$$

$$C_{it}(\psi_s) \equiv -\frac{dQ_{it}}{d\psi_s}A. \tag{A.6}$$

The insulator fixed charge is assumed to be independent of ψ_s ($dQ_f/d\psi_s = 0$), so that no capacitive component is associated with this charge.

Combining (A.4)–(A.6) with (A.1) and (A.2), and using $dQ_f/d\psi_s = 0$, the total low-frequency capacitance C_{lf} of the MIS capacitor is related to its components by

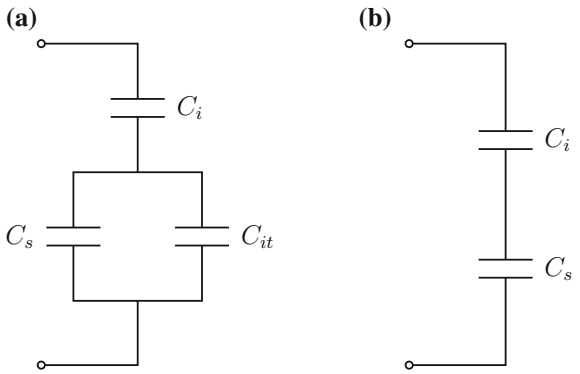

Fig. A.3 **a** Low frequency, and **b** high frequency equivalent circuits of the MIS capacitor

$$C_{lf}^{-1} = C_i^{-1} + (C_s + C_{it})^{-1}. \tag{A.7}$$

The corresponding low-frequency equivalent circuit of the MIS capacitor is shown in Fig. A.3a. The insulator capacitance C_i is connected in series with the parallel combination of the semiconductor capacitance C_s and the interface state capacitance C_{it}. At high frequencies, interface states are unable to follow variations in the Fermi level, and (A.7) is reduced to

$$C_{hf}^{-1} = C_i^{-1} + C_s^{-1}, \tag{A.8}$$

with the corresponding equivalent circuit shown in Fig. A.3b.

The insulator capacitance C_i is given by

$$C_i = \epsilon_i A / t_i, \tag{A.9}$$

where ϵ_i is the insulator permittivity, and t_i is the insulator thickness. It is common to refer to an equivalent oxide thickness (EOT), given by calculating t_i from (A.9) with ϵ_i equal to the value for thermal SiO_2 ($3.9 \times \epsilon_0$) [2]

Assuming that D_{it} is a slowly varying function of energy, C_{it} is simply related to D_{it} by

$$C_{it}(\psi_s) = q A D_{it}(\psi_s). \tag{A.10}$$

Finally, assuming Fermi–Dirac statistics apply, Q_s is given by

$$\begin{aligned} Q_s = (2kT\epsilon_s)^{1/2} \Bigg\{ & N_c \left[F_{3/2}\left(\frac{E_F - E_c + q\psi_s}{kT} \right) - F_{3/2}\left(\frac{E_F - E_c}{kT} \right) \right] + \\ & N_v \left[F_{3/2}\left(\frac{E_v - E_F - q\psi_s}{kT} \right) - F_{3/2}\left(\frac{E_v - E_F}{kT} \right) \right] + \\ & (N_A - N_D)\left(\frac{q}{kT}\psi_s \right) \Bigg\}^{1/2}. \end{aligned} \tag{A.11}$$

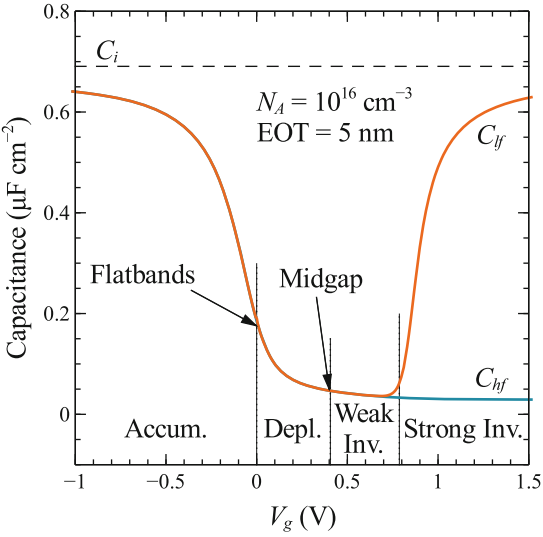

Fig. A.4 Modelled ideal C–V curve (no interface states, $V_{fb} = 0\,\text{V}$) of a silicon MIS capacitor at low and high frequencies. The voltage ranges corresponding to accumulation, depletion, weak inversion, and strong inversion are indicated

In the low-frequency case, C_s is then found by substituting Q_s from (A.11) in (A.5):

$$C_s(\psi_s) = \frac{q\epsilon_s A}{Q_s}\left[N_c F_{1/2}\left(\frac{E_F - E_c + q\psi_s}{kT}\right) - N_v F_{1/2}\left(\frac{E_v - E_F - q\psi_s}{kT}\right) + N_A - N_D\right]. \tag{A.12}$$

For Boltzmann (non-degenerate) statistics, the Fermi integrals in (A.11) and (A.12) may be replaced with exponential functions.

Figure A.4 shows low-frequency capacitance C_{lf} versus gate voltage V_g, calculated from (A.2), (A.7), (A.9), (A.11), and (A.12), with D_{it}, Q_f, and $W_{ms} = 0$. In accumulation and strong inversion, C_s is large, and C_{lf} approaches C_i, while in depletion and weak inversion C_{lf} is limited by the much smaller value of C_s.

At high frequencies both the inversion layer charge and the interface state charge are unable to follow the AC voltage signal, but do follow changes in the gate bias (although spatial redistribution of the inversion layer charge in response to the AC signal does occur). As a result the high-frequency capacitance C_{hf} saturates at a low value in strong inversion rather than increasing as for low frequencies, as shown in Fig. A.4. The resulting expression for C_s is somewhat more complex than for the low-frequency case, and we do not attempt to provide a derivation here. Exact expressions for the non-degenerate case are given by Nicollian and Brews [1].

Thus, to the first approximation, C_i is independent of the applied bias and frequency (though see the following section on the frequency dispersion of the permittivity), while C_s and C_{it} are strong functions of both. These different dependencies may be exploited in order to determine the value of each component.

A.2 Measurement Corrections

Measured C–V data is subject to systematic errors and non-idealities that must be taken into account to allow an accurate analysis. This section details the correction procedure applied to measured C–V data in this work.

A.2.1 Parallel and Series Representations

The complex admittance measured by the LCR meter is a vector quantity with real and imaginary components that can be described using a number of equivalent representations. In general for C–V analysis it is most conveniently described as the parallel combination of one capacitive and one conductive component. We shall refer to the measured values of these components as C_{mp} and G_{mp} respectively. The corresponding equivalent circuit is shown in Fig. A.5a.

In some situations, however, it is useful to convert this representation into an equivalent series form, with capacitive and resistive components C_{ms} and R_{ms}, as shown in Fig. A.5b. The following set of relationships may be used to convert between the two equivalent forms.

$$C_{ms} = \frac{G_{mp}^2 + \omega^2 C_{mp}^2}{\omega^2 C_{mp}}, \tag{A.13}$$

$$R_{ms} = \frac{G_{mp}}{G_{mp}^2 + \omega^2 C_{mp}^2}, \tag{A.14}$$

$$C_{mp} = \frac{C_{ms}}{1 + (\omega R_{ms} C_{ms})^2}, \tag{A.15}$$

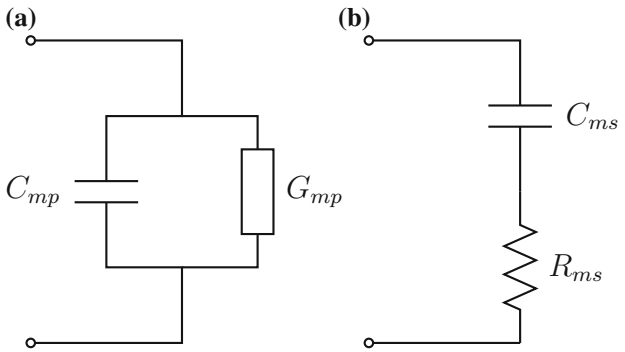

Fig. A.5 **a** Parallel and **b** series equivalent circuits

$$G_{mp} = \frac{1}{R_{ms} + (\omega^2 R_{ms} C_{ms}^2)^{-1}}. \tag{A.16}$$

A.2.2 Parasitic Circuit Elements

A real C–V measurement contains contributions from parasitic elements external to the MIS sample, arising from non-idealities in the measurement system, wires, probes, rear contact, and chuck. These may be described by additional elements in the equivalent circuit of the measurement, as shown in Fig. A.6. Parasitic elements which may be present include parallel capacitance and conductance due to the measurement setup (C_{pp} and G_{pp}), contact capacitance and resistance (C_c and R_c), and equivalent series resistance and inductance (R_s and L). C_{pp} and G_{pp} are corrected for by calibration of the capacitance meter, while C_c and R_c can be made negligible with proper ohmic contacting. This leaves R_s and L as generally non-negligible parasitic elements that must be evaluated and corrected for in careful measurements.

The equivalent series resistance R_s is usually due largely to the resistance of the semiconductor bulk between the rear contact and the edge of the space-charge region. The effect of R_s is to decrease C_{mp} and increase G_{mp} at high frequencies. R_s is most straightforwardly determined from the admittance in accumulation. In strong accumulation, the resistance contribution of interface states is shunted by the large semiconductor capacitance, and $R_s = R_{ms}$, where R_{ms} may be determined from (A.14) [1].

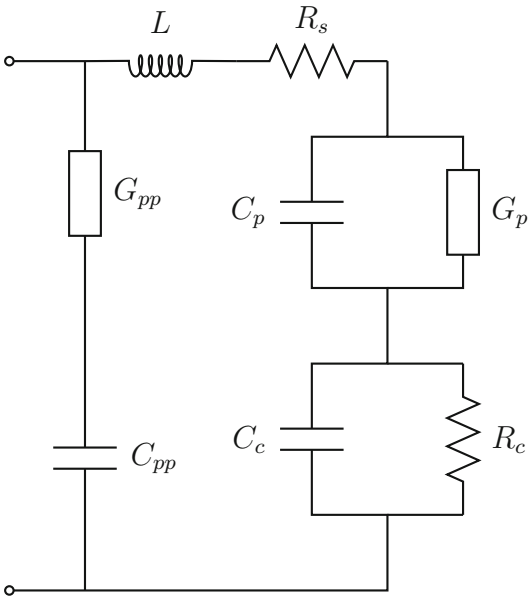

Fig. A.6 **a** Full equivalent circuit corresponding to the C–V measurement, including parasitic elements of the measurement system

In addition to series resistance, series inductance L within the measurement circuit is often a significant source of error, acting to increase the measured capacitance at high frequencies. Like R_s, L is most easily determined in accumulation, where the impedance of the device itself is minimised. Unlike R_s however, L cannot be determined from measurements at a single frequency, since L appears in series with the device capacitance. Instead, measurements at two or more frequencies must be used to distinguish the inductive and capacitive components through their different frequency dependence.

Figure A.7 shows an example of the determination of L by this method. C_{ms} is measured as a function of frequency in accumulation, and L is determined by fitting the measured capacitance with an equivalent circuit model including a frequency-dependent capacitance (see the later part of this section on the frequency dispersion of the permittivity) in series with an inductance. For the measurement system used in this work, L was found to be a function of the capacitance of the device under test. This dependence was assessed by evaluating L for capacitor test structures with nominal capacitances ranging from 47 to 1000 pF, in the same way as shown in Fig. A.7. The results are plotted in Fig. A.8 as a function of C_{ms}^{-1}. It was found that L possessed a linear dependence on C_{ms}^{-1}, given by

$$L = a + bC_{ms}^{-1}, \tag{A.17}$$

where $a = 1.46\,\mu\text{H}$ and $b = 1.65 \times 10^{-16}\,\text{FH}$.[1] Rather than assess L in each individual case, this empirical relationship was subsequently used to determine L for samples measured with this system.

The measured admittance is most straightforwardly corrected for equivalent series resistance and inductance by first converting to its series form via (A.13) and (A.14). Corrected series resistance and capacitance R'_{ms} and C'_{ms} may then be calculated from

$$R'_{ms} = R_{ms} - R_s, \tag{A.18}$$

and

$$\frac{1}{C'_{ms}} = \frac{1}{C_{ms}} + \omega^2 L. \tag{A.19}$$

Corrected parallel capacitance C'_{mp}, and conductance G'_{mp}, may subsequently be calculated from C'_{ms} and R'_{ms} via (A.15) and (A.16). These values are those used in subsequent analysis.

[1] We note that the values of a and b are likely to depend on the details of the measurement setup, and would therefore need to be newly determined if significant changes were made to this setup.

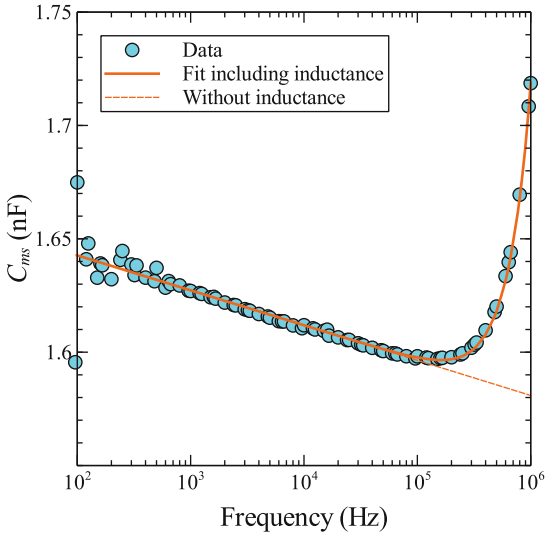

Fig. A.7 Experimental C_{ms} versus frequency f for an n-type Al_2O_3 MIS sample in accumulation. Fits using an equivalent circuit model with and without the inclusion of series inductance are also shown. The linear slope of C_{ms} with log f at lower frequencies is due to frequency dispersion of the insulator permittivity. At higher frequencies, C_{ms} increases sharply due to inductance

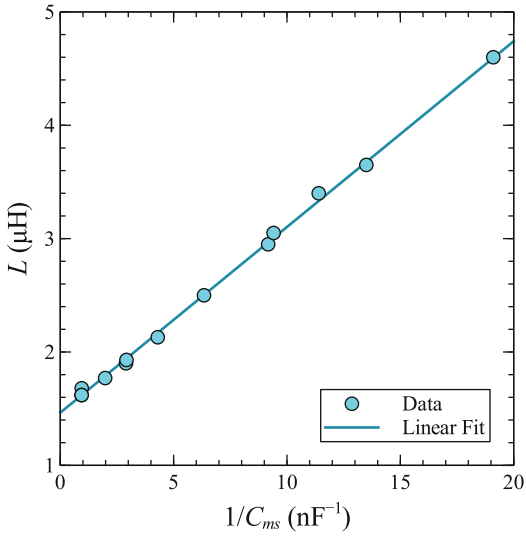

Fig. A.8 Equivalent series inductance L versus $1/C_{ms}$ for capacitor test structures with a range of nominal capacitances, measured by the system used in this work

A.2.3 Quasi-Static Capacitance Correction

While the low-frequency capacitance is not subject to the same parasitic effects as the high-frequency measurement, it can suffer from other sources of error. Because of the practical difficulties in performing true low-frequency AC capacitance measurements,[2] the "low-frequency" capacitance is instead commonly measured using

[2]It should be noted that "low-frequency" is defined relative to the response of the interface states and the semiconductor minority carriers. At low-frequency these should be in thermal equilibrium

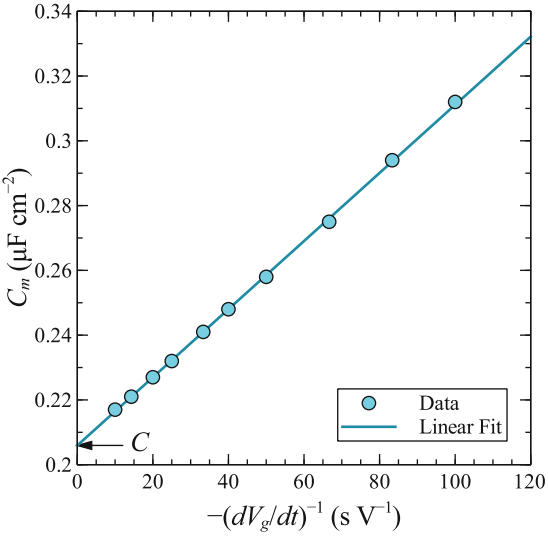

Fig. A.9 Quasi-static capacitance measured for an Al_2O_3 MIS capacitor in accumulation, as a function of the inverse voltage sweep rate. The corrected device capacitance is found from the intercept of the linear fit at $(dV_g/dt)^{-1} = 0$

the linear voltage-ramp method (a so-called "quasi-static" capacitance[3]) [3]. In this method, the capacitance is calculated from the displacement current I_d that flows in response to a linear voltage sweep with sweep rate dV_g/dt, using the relationship $C = I_d(dV_g/dt)^{-1}$. However, besides the displacement current, additional contributions to the measured current may be present due either to leakage current between the semiconductor and the gate, or to uncompensated background current within the measurement system. These currents may be distinguished from the displacement current by the fact that they are independent of the sweep rate, and thus constitute a static current I_s. In the presence of such currents the measured capacitance C_m may be expressed as [4, 5]

$$C_m = C + I_s(dV_g/dt)^{-1}. \tag{A.20}$$

Equation (A.20) implies that the corrected capacitance C may be determined from measurements at two or more different sweep rates. Figure A.9 shows this graphically by plotting experimentally determined C_m as a function of inverse sweep rate for a p-type Al_2O_3 MIS capacitor in accumulation. As expected from (A.20), C_m shows a linear dependence on $(dV_g/dt)^{-1}$, with a slope equal to I_s (in this particular case I_s can be shown to be due to the measurement system rather than to leakage current). The corrected device capacitance C is given by the intercept at $(dV_g/dt)^{-1} = 0$.

(Footnote 2 continued)
with the surface potential over the full C–V curve. This condition is usually not achieved at the low-frequency limit of typical AC capacitance meters at room temperature.

[3]The term "quasi-static" is generally used elsewhere in this work when referring to low-frequency C–V measurements performed by the voltage-ramp method.

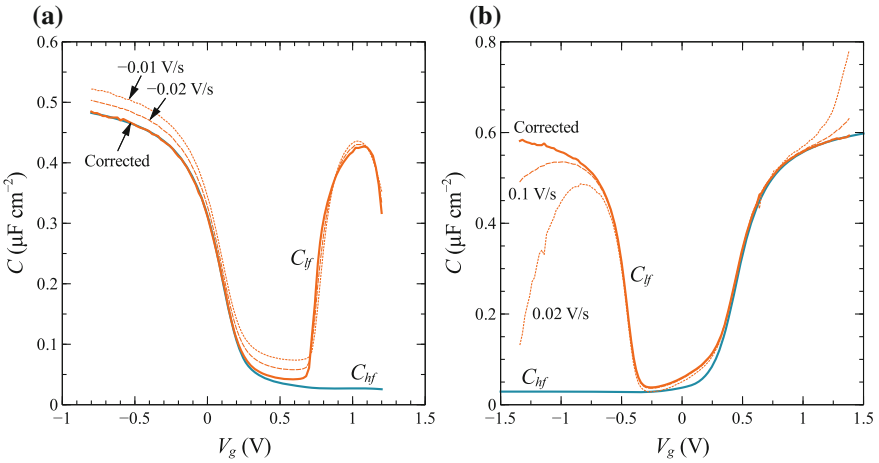

Fig. A.10 Experimental examples of the use of quasi-static C–V measurements at different sweep rates to correct for the effects of **a** non-zeroed background current within the measurement system, and **b** leakage current through the dielectric

In general, measurements at two different sweep rates are sufficient to correct the quasi-static capacitance for static current contributions via (A.20).[4] Figure A.10 shows examples of such a correction applied to experimental quasi-static C–V data. This procedure is routinely applied to C–V measurements presented in this work.

A.2.4 Permittivity Frequency Dispersion

In conventional C–V analysis it is implicitly assumed that C_i is independent of the measurement frequency, so that high- and low-frequency (or quasi-static) C–V measurements may be directly compared. In fact, the insulator permittivity is usually significantly frequency-dependent in the frequency range of the measurement, due to broad frequency dispersion of the (dipolar) dielectric response. This may readily be observed by measuring the accumulation capacitance as a function of frequency, as shown in Fig. A.7. Such frequency dispersion of the permittivity is a general feature of dielectric materials [6], and is well-attested for Al_2O_3 [7–9]. As a consequence, the accumulation capacitance measured at low frequencies or under quasi-static conditions is expected to be greater than that measured at high frequencies.[5]

Therefore, in comparing measurements made at high and low frequencies, we need to take into account that C_i is frequency-dependent. The simplest way of doing

[4] Alternatively, I_s may also be determined by separate current–voltage measurements.

[5] While this is indeed commonly observed in experimental data within the literature, it is typically attributed to measurement error when it is noted at all.

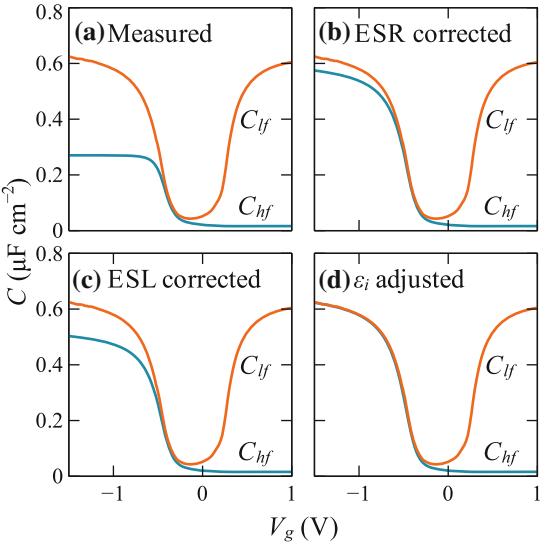

Fig. A.11 Example of correction procedure applied to experimental high-frequency (1 MHz) capacitance. The measured parallel capacitance is shown **a** without corrections, **b** after correction for equivalent series resistance and **c** inductance, and **d** after adjusting for the frequency dispersion of the insulator permittivity via (A.21)

this is to adjust one or other measurement for the difference in C_i. For C–V analysis, we are primarily interested in the static (zero frequency) permittivity, since this is the value which is relevant for the determination of the insulator fixed charge Q_f from the flatband voltage shift. This value is most closely approached under the conditions of the low-frequency or quasi-static capacitance measurement. Therefore we choose to calculate an adjusted high-frequency capacitance C'_{hf} according to

$$C'_{hf} = \left(C_{hf}^{-1} + C_{i,lf}^{-1} - C_{i,hf}^{-1}\right)^{-1}, \tag{A.21}$$

where $C_{i,hf}$ and $C_{i,lf}$ are the insulator capacitances at high and low frequencies respectively. The value of $C_{i,lf}^{-1} - C_{i,hf}^{-1}$ in (A.21) is chosen such that $C'_{hf} = C_{lf}$ in strong accumulation. Figure A.11 shows an example of such an adjustment applied to experimental data.

A.3 Parameter Extraction

Having corrected the experimental data for measurement errors and inconsistencies, we next wish to analyse it in order to extract various physical parameters of interest. These include the insulator capacitance, dopant concentration, flatband voltage (and by extension, the insulator charge), and the interface state density. This section describes the procedure used to extract these parameters in this work.

A.3.1 Insulator Capacitance

In the expression for the high-frequency MIS capacitance (Eq. (A.8)), the insulator capacitance C_i appears in series with the semiconductor capacitance C_s. In order to extract C_i it is therefore necessary to make some assumption about C_s. Most commonly, it is assumed that $C_s \gg C_i$ in strong accumulation, so that C_i is simply given by the maximum measured capacitance in accumulation. This approximation is commonly used because of its simplicity, and is reasonable for thicker dielectrics ($\gtrapprox$100 nm), for which C_i is small. However, it becomes an increasingly poor approximation as insulator thickness is decreased, especially for high-κ materials.

A number of more sophisticated approximations have been proposed for extraction of C_i [10–15]. In this work we use that of McNutt and Sah [11], as extended by Walstra and Sah [13]. These authors derived the following expression for C_i based on the Boltzmann approximation for the carrier statistics in strong accumulation:

$$C_i = C\left[1 - \left(-2\frac{kT}{q}C^{-1}\frac{dC}{dV_g}\right)^{1/2}\right]^{-1}. \tag{A.22}$$

Equation (A.22) implies that a plot of $(-2kT/qC^{-1}(dC/dV_g))^{1/2}$ versus C in non-degenerate strong accumulation will have a slope of $-C_i^{-1}$ and an intercept of C_i at $dC/dV_g = 0$. In practice, the value derived from the intercept is significantly less sensitive to the assumed carrier statistics, and is therefore preferred. Figure A.12 shows an experimental example of such a plot, together with the fit used to extract C_i. For this sample, use of (A.22) to determine C_i results in a value 8 % higher

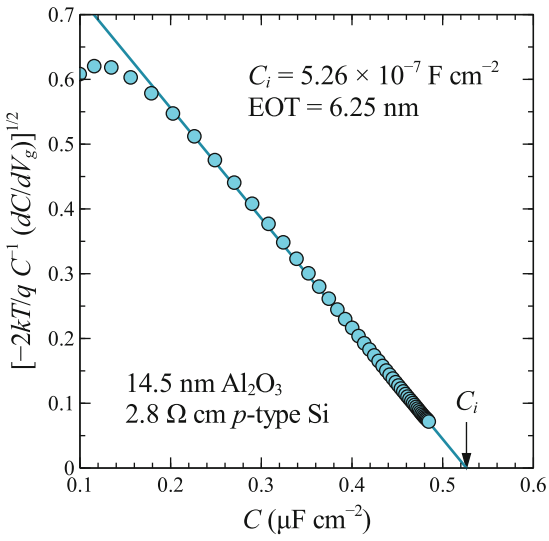

Fig. A.12 Example of C_i extraction from experimental C–V data via Eq. (A.22)

than the maximum measured capacitance. The relative difference increases as film thickness is reduced. Equation (A.22) is still an approximation, because it is based on Boltzmann statistics, and hence neglects degeneracy and surface quantisation effects. Because of this, it is still expected to underestimate C_i, though to a significantly lesser extent than when C_i is taken as equal to the maximum measured capacitance.

A.3.2 Dopant Concentration

The dopant concentration N_{dop} is most accurately determined from the slope of the capacitance in depletion, according to [1]

$$N_{dop} = 2\left[q\epsilon_s A^2 \frac{d}{dV_g}\left(\frac{1}{C_{hf}^2}\right)\right]^{-1}\left(\frac{1 - C_{lf}/C_i}{1 - C_{hf}/C_i}\right), \tag{A.23}$$

where the latter term accounts for voltage stretch-out due to interface states. The corresponding depletion layer width w_D is given by

$$w_D = \epsilon_s A(C_{hf}^{-1} - C_i^{-1}). \tag{A.24}$$

Using (A.23) and (A.24), N_{dop} may be plotted as a function of distance from the semiconductor surface.

Figure A.13 shows N_{dop} versus w_D calculated in this way for samples with two different Al_2O_3 films fabricated on the same 8.2 Ω cm *p*-type substrate. The apparent

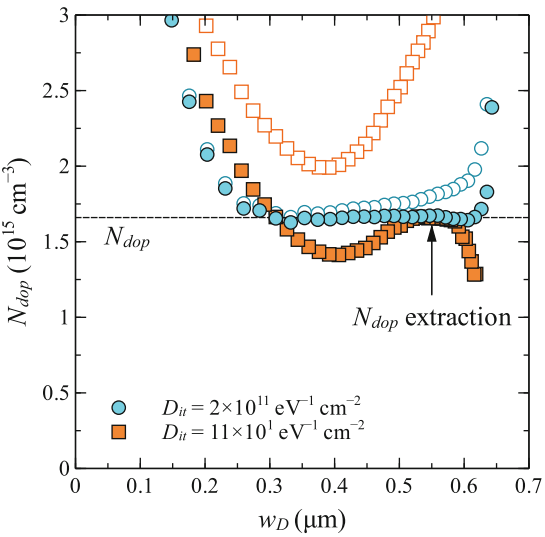

Fig. A.13 Experimental N_{dop} profiles calculated using Eqs. (A.23) and (A.24). Data are shown for two samples processed on the same *p*-type substrate with different Al_2O_3 films, distinguished by the value of D_{it} at midgap. Closed (open) symbols show N_{dop} with (without) correction for stretch-out due to interface states

rise of N_{dop} near the surface is due to the failure of the depletion approximation—which underlies Eqs. (A.23) and (A.24)—for small departures from flatbands [1]. The subsequent dip in N_{dop}, visible most prominently for the sample with higher D_{it}, is due to the distortion of the 1 MHz high-frequency capacitance by interface state response near flatbands [1]. Its magnitude thus depends on D_{it}. N_{dop} should be extracted from the flat part of the profile following the dip. Figure A.13 also shows that neglecting the interface state correction term in (A.23) results in significant error in the apparent N_{dop}, especially as D_{it} increases.

A.3.3 Flatband Voltage and Charge

A widely used method of determining V_{fb} is to calculate the theoretical capacitance at flatbands from C_i and N_{dop} using (A.8) and (A.12), and then to find the voltage corresponding to this capacitance on the experimental high-frequency C–V curve. This method is commonly used because of its simplicity. However, it is subject to systematic error due to the failure of the high-frequency assumption at flatbands for typical measurement frequencies. That is, interface state response at flatbands is non-zero, and $C_{it} > 0$. This results in systematic over(under)estimation of V_{fb} for p-type (n-type) substrates. This error increases with increasing D_{it}.

As proposed by [1], a better point of comparison is the capacitance in depletion, where interface state response is slower, and the assumption of high-frequency conditions is more usually valid. The most straightforward way to make this comparison is to calculate a gate voltage V_{g0} corrected for stretch-out due to interface states

$$V_{g0} = \int_{V_{fb}}^{V_g} \frac{C_i + C_s}{C_i + C_s + C_{it}}\, dV. \tag{A.25}$$

We begin by calculating V_{g0} from (A.25) making an arbitrary initial guess for V_{fb}. By plotting $1/C^2$ versus V_{g0} calculated in this way, and an ideal $1/C^2$ versus V_{g0} calculated from (A.2), (A.8), and (A.12), with D_{it}, Q_f, and $W_{ms} = 0$, we should obtain two parallel linear curves in depletion, with a slope given by $2(q\epsilon_s N_{dop})^{-1}$. We label the voltage shift of the measured plot relative to the ideal plot ΔV_{g0}. V_{fb} is then found as the value of V_g for which V_{g0} calculated from (A.25) is equal to ΔV_{g0}. Figure A.14 shows an experimental example of the determination of ΔV_{g0} in this manner.

To make use of (A.25) to determine V_{fb}, we must know C_{it} as a function of gate voltage. The formulation given by [1] for V_{g0} uses C_{it} derived from the combined high–low frequency capacitance method [16]. This has the advantage of allowing an explicit determination of V_{g0}, since D_{it} determined by this method is independent of V_{fb}. However, it results in systematic error in V_{fb}, due to the fact that D_{it} near flatbands is systematically underestimated by this method. In this work, we instead use D_{it} calculated from (A.29) for the purpose of determining (A.25). Since D_{it}

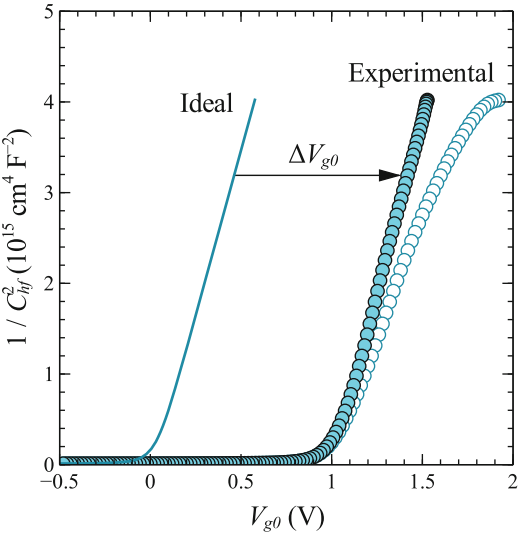

Fig. A.14 Example of experimental determination of ΔV_{g0} using (A.25). Closed (open) symbols show experimental data plotted against V_{g0} (V_g), where the latter is uncorrected for stretch-out due to interface states

from (A.29) depends on V_{fb}, this approach requires an iterative solution, but it avoids systematic error in V_{fb}.

From (A.3), V_{fb} is related to the insulator fixed charge Q_f and interface state trapped charge Q_{it} by

$$V_{fb} = \frac{(1 + x_c/t_i)Q_f + Q_{it}}{C_i/A} + W_{ms}. \tag{A.26}$$

Assuming $x_c = 0$ (i.e. Q_f is located at the semiconductor–dielectric interface), we may write

$$Q_{tot} = Q_f + Q_{it} = \frac{C_i}{A}(V_{fb} - W_{ms}). \tag{A.27}$$

Given V_{fb}, Eq. (A.27) may thus be used to assess the sum of Q_f and Q_{it}, designated Q_{tot}. When Q_{it} is negligible (e.g. for samples with low D_{it}), $Q_{tot} \approx Q_f$.

The metal–semiconductor work-function difference W_{ms} is given by

$$W_{ms} = \phi_m - (\phi_s - \phi_b), \tag{A.28}$$

where ϕ_m and ϕ_s are the metal and semiconductor work-functions (the latter defined with respect to E_i), and ϕ_b is the semiconductor bulk potential which is determined by the dopant concentration. The values of ϕ_m and ϕ_s used in this work are those recommended by Kawano [17] of 4.23 V for Al, 4.71 V for intrinsic ⟨100⟩ Si, and 4.79 V for intrinsic ⟨111⟩ Si.

A.3.4 Interface State Density

From (A.7) and (A.10), D_{it} may be related to the low-frequency (quasi-static) capacitance C_{lf} by [18]

$$qAD_{it}(\psi_s) = C_{it} = (C_{lf}^{-1} - C_i^{-1})^{-1} - C_s(\psi_s). \tag{A.29}$$

C_s in (A.29) may be calculated using (A.12), following determination of $\psi_s(V_g)$. The latter may be calculated from the low-frequency C–V curve via [18]

$$\psi_s(V_g) = \int_{V_{fb}}^{V_g} \left(1 - \frac{C_{lf}}{C_i}\right) dV. \tag{A.30}$$

Alternatively, C_s may be determined directly from the difference between C_{lf} and C_{hf}. Combining (A.8) with (A.29) leads to [16]

$$qAD_{it}(\psi_s) = C_{it} = (C_{lf}^{-1} - C_i^{-1})^{-1} - (C_{hf}^{-1} - C_i^{-1})^{-1}. \tag{A.31}$$

This has the advantage of avoiding the need to calculate C_s theoretically. However the use of (A.31) results in systematic underestimation of D_{it} near flatbands due to non-zero interface state response at practical measurement frequencies [1]. D_{it} determined by (A.29) is more accurate in this range.

D_{it} can also be calculated from the voltage stretch-out of the high-frequency C–V curve as described by Terman [19]. However, this method is also subject to significant error near flatbands due to non-zero interface state response, and additionally requires accurate knowledge of the dopant concentration, which cannot be determined reliably from C_{hf} alone when interface states are present [1]. Consequently, the use of (A.29) or even (A.31) to determine D_{it} is preferable. The former is used in this thesis.

A.3.5 General Procedure

The general procedure followed in this work for parameter extraction from corrected C–V data is as follows:

1. C_i is determined from (A.22).
2. N_{dop} is determined from (A.23).
3. An initial guess value for V_{fb} is determined using the theoretical flatband capacitance calculated from (A.8) and (A.12).
4. $\psi_s(V_g)$ is determined from (A.30).
5. $D_{it}(\psi_s)$ is determined from (A.29).
6. V_{fb} is determined from (A.25).
7. Steps 4–6 are iterated to determine V_{fb} and $D_{it}(\psi_s)$ self-consistently.
8. Q_{tot} is evaluated from V_{fb} and C_i via (A.27).

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Appendix B
The Conductance Method

The C–V method (Appendix A) may be used to evaluate the energetic distribution of interface states, but provides only limited information concerning their capture cross-sections, which determine their effectiveness as recombination centres. For this purpose, other, related techniques must be employed, such as DLTS (which examines the temperature dependence of time-domain capacitance transients), or measurements of the MIS parallel conductance as a function of frequency. The latter technique, generally referred to as the conductance method, is the subject of this appendix.

The use of the conductance method to determine interface state properties was pioneered by Nicollian and Goetzberger [1, 2], and subsequently employed by numerous authors, particularly for the characterisation of the Si–SiO_2 interface. A detailed exposition of the method, together with a comprehensive survey of work up to that date, was given by [3].

We first briefly describe the principles of the method, before presenting the relevant theory and equations. Following Cooper and Schwartz [4], we include minority carrier effects in our treatment of the equivalent circuit of the interface states. These are usually neglected, which unnecessarily limits the range of validity of the method. The derivation of the equations closely follows that of [4], except that here full expressions for all of the elements of the equivalent circuit are given explicitly rather than simply implied.

B.1 Principles

The principle of the conductance method is based on the energy loss that occurs when interface state capture and emission occurs out of phase with an AC variation of the surface Fermi level. At low frequencies, the interface states are able to change their occupancy in response to Fermi-level variations in order to maintain equilibrium, and no energy loss occurs. At very high frequencies, Fermi-level variations occur too quickly for the interface states to follow at all, so that energy loss is again zero.

L.E. Black, *New Perspectives on Surface Passivation: Understanding the Si–Al_2O_3 Interface*, Springer Theses, DOI 10.1007/978-3-319-32521-7

However, at intermediate frequencies, interface state response occurs out of phase with the applied signal, leading to energy loss as electrons transition from higher to lower energy states.

This energy loss manifests as an increase of the small-signal parallel conductance G_p of the MIS capacitor. The component of G_p due to the interface state branch of the MIS equivalent circuit, designated $\langle G_p \rangle$, is given by

$$\frac{\langle G_p \rangle}{\omega} = \frac{\omega C_i^2 G_p}{G_p^2 + \omega^2 (C_i - C_p)^2}. \tag{B.1}$$

When plotted as $\langle G_p \rangle / \omega$ versus frequency on a log scale, this contribution forms a peaked function with a peak frequency corresponding to the time constant for majority carrier capture, and an integrated area proportional to the interface state density. The peak width is broadened relative to that expected from single-time-constant behaviour due to short-range statistical fluctuations of the surface potential, described by the standard deviation of surface potential σ_s. Minority carrier contributions alter the shape of the peak at lower frequencies.

Parameter extraction requires fitting such experimental $\langle G_p \rangle / \omega$ data over a range of frequencies with a numerical model. The following section describes the equivalent circuit model used for this purpose.

B.2 Equivalent Circuit

The small-signal equivalent circuit of the MIS capacitor including an energetic distribution of interface states is shown in Fig. B.1. Each state may exchange charge with the valence and conduction bands via capture resistances R_{ps} and R_{ns} for holes and electrons, and may store charge on a capacitance C_{it} connected to the displacement current line of the semiconductor. C_I and C_D are the capacitances of the inversion layer and depletion region respectively. The values of R_{ps}, R_{ns}, and C_{it} are given by

$$R_{ps} = \left(\frac{q}{kT} q A D_{it} f_t \sigma_p v_{th} p_s \right)^{-1}, \tag{B.2}$$

$$R_{ns} = \left(\frac{q}{kT} q A D_{it} (1 - f_t) \sigma_n v_{th} n_s \right)^{-1}, \tag{B.3}$$

$$C_{it} = \frac{q}{kT} q A D_{it} f_t (1 - f_t), \tag{B.4}$$

where

$$f_t = \left(1 + \exp\left(\frac{E_t - E_F}{kT} \right) \right)^{-1} \tag{B.5}$$

is the Fermi occupation function for interface states of energy E_t.

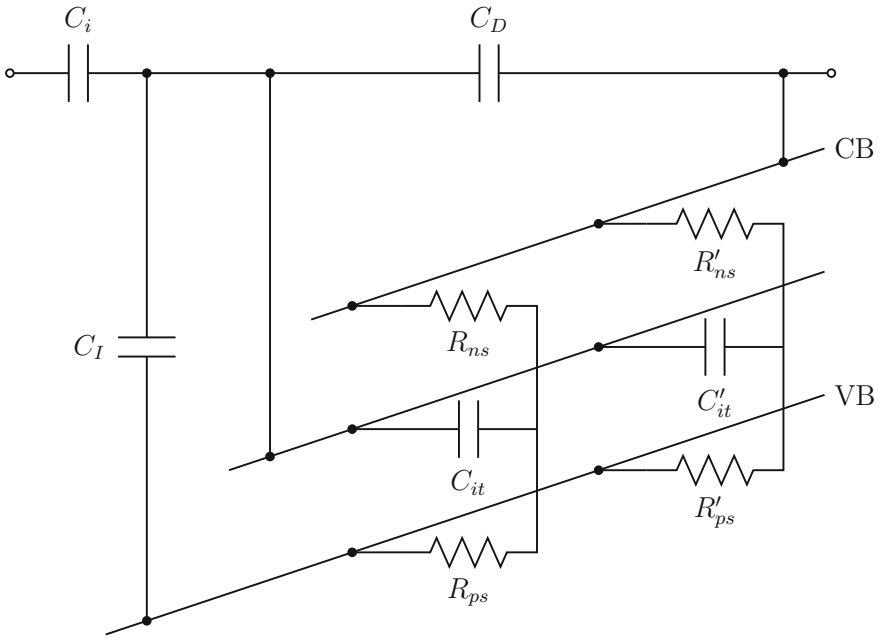

Fig. B.1 Equivalent circuit of the (n-type) MIS capacitor with a distribution of interface states throughout the semiconductor bandgap (in this case two states are shown, but an arbitrary number may be present)

By performing a Y-Δ transformation, the equivalent circuit of Fig. B.1 becomes a parallel network of lumped admittance elements Y_{dp}, Y_{dn}, and Y_{pn} as shown in Fig. B.2. These elements are given by

$$Y_{dp} = \frac{j\omega R_{ns} C_{it}}{R_{ns} + R_{ps} + j\omega R_{ns} R_{ps} C_{it}}, \tag{B.6}$$

$$Y_{dn} = \frac{j\omega R_{ps} C_{it}}{R_{ns} + R_{ps} + j\omega R_{ns} R_{ps} C_{it}}, \tag{B.7}$$

$$Y_{pn} = \frac{1}{R_{ns} + R_{ps} + j\omega R_{ns} R_{ps} C_{it}}. \tag{B.8}$$

The total lumped admittance between each node may then simply be calculated as the sum of the individual Y_{dp}, Y_{dn}, and Y_{pn} elements (i.e. $Y_{dp} + Y'_{dp} + Y''_{dp} + \ldots$). Because each admittance depends both on the interface state energy and on the surface carrier concentration (which varies locally due to surface potential fluctuations), this involves a double integration over both bandgap energy and surface potential, where the latter integral is weighted by the surface potential probability density function

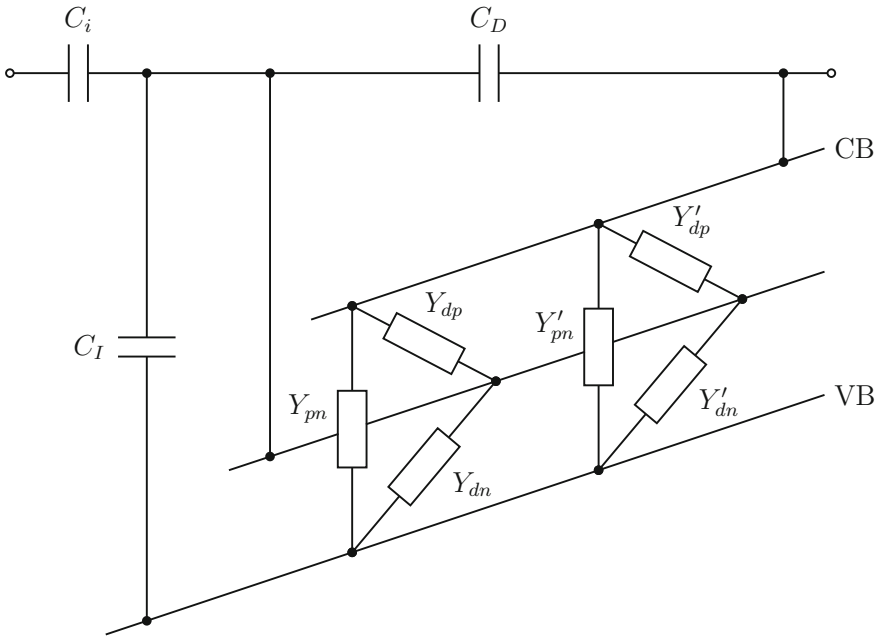

Fig. B.2 Parallel equivalent circuit of the (n-type) MIS capacitor following a Y-Δ transformation

$P(\psi_s)$, where

$$P(\psi_s) = (2\pi\sigma_s^2)^{-1/2} \exp\left[-(kT/q)^{-2}\frac{(\psi_s - \bar{\psi}_s)^2}{2\sigma_s^2}\right], \tag{B.9}$$

$\bar{\psi}_s$ is the mean surface potential, and σ_s^2 is the variance of band bending in units of kT/q. Writing the real and imaginary parts of these admittances separately, we have

$$\frac{G_{dp}}{\omega} = \int_{-\infty}^{\infty}\int_{E_v}^{E_c} \frac{\omega R_{ps} C_{it}}{(1 + R_{ps}/R_{ns})^2 + (\omega R_{ps} C_{it})^2} C_{it} P(\psi_s)\, dE_t\, d\psi_s, \tag{B.10}$$

$$C_{dp} = \int_{-\infty}^{\infty}\int_{E_v}^{E_c} \frac{1 + R_{ps}/R_{ns}}{(1 + R_{ps}/R_{ns})^2 + (\omega R_{ps} C_{it})^2} C_{it} P(\psi_s)\, dE_t\, d\psi_s, \tag{B.11}$$

$$\frac{G_{dn}}{\omega} = \int_{-\infty}^{\infty}\int_{E_v}^{E_c} \frac{\omega R_{ns} C_{it}}{(1 + R_{ns}/R_{ps})^2 + (\omega R_{ns} C_{it})^2} C_{it} P(\psi_s)\, dE_t\, d\psi_s, \tag{B.12}$$

$$C_{dn} = \int_{-\infty}^{\infty}\int_{E_v}^{E_c} \frac{1 + R_{ns}/R_{ps}}{(1 + R_{ns}/R_{ps})^2 + (\omega R_{ns} C_{it})^2} C_{it} P(\psi_s)\, dE_t\, d\psi_s, \tag{B.13}$$

$$G_{pn} = \int_{-\infty}^{\infty} \int_{E_v}^{E_c} \frac{R_{ns} + R_{ps}}{(R_{ns} + R_{ps})^2 + (\omega R_{ns} R_{ps} C_{it})^2} P(\psi_s)\, dE_t\, d\psi_s, \tag{B.14}$$

$$C_{pn} = \int_{-\infty}^{\infty} \int_{E_v}^{E_c} \frac{R_{ns} R_{ps} C_{it}}{(R_{ns} + R_{ps})^2 + (\omega R_{ns} R_{ps} C_{it})^2} P(\psi_s)\, dE_t\, d\psi_s. \tag{B.15}$$

Finally, the total semiconductor admittance including the interface states is given (for n-type doping) by

$$Y_s = j\omega C_D + Y_{dn} + \left[(j\omega C_I + Y_{dp})^{-1} + Y_{pn}^{-1} \right]^{-1}. \tag{B.16}$$

Solving for the real and imaginary components gives

$$\langle G_p \rangle = G_{dn} + \frac{\begin{array}{c}(G_{dp} + G_{pn})\left[G_{dp} G_{pn} - \omega^2 C_{pn}(C_I + C_{dp})\right] \\ + \omega^2 (C_I + C_{dp} + C_{pn})\left[G_{dp} C_{pn} + G_{pn}(C_I + C_{dp})\right]\end{array}}{(G_{dp} + G_{pn})^2 + \omega^2 (C_I + C_{dp} + C_{pn})^2}, \tag{B.17}$$

and

$$\langle C_p \rangle = C_D + C_{dn} + \frac{\begin{array}{c}(G_{dp} + G_{pn})\left[G_{dp} C_{pn} + G_{pn}(C_I + C_{dp})\right] \\ - (C_I + C_{dp} + C_{pn})\left[G_{dp} G_{pn} - \omega^2 C_{pn}(C_I + C_{dp})\right]\end{array}}{(G_{dp} + G_{pn})^2 + \omega^2 (C_I + C_{dp} + C_{pn})^2}. \tag{B.18}$$

Analogous expressions apply for the case of p-type doping.

In order to determine D_{it}, σ_p, σ_n, and σ_s, by the conductance method, these parameters must be adjusted to provide a good fit between $\langle G_p \rangle / \omega$ calculated from Eq. (B.17), and experimental data measured over a range of frequencies. In this work, automated least-squares fitting of $\langle G_p \rangle / \omega$ data was performed using the Levenberg–Marquardt algorithm. Interface states at different energies are probed by performing measurements over a range of gate biases in depletion and weak inversion. C_I is generally negligible at these biases and thus may be neglected when calculating $\langle G_p \rangle / \omega$ from (B.17). The surface potential ψ_s must be determined independently as a function of gate bias using C–V measurements, as described in Appendix A. This may then be used to calculate p_s and n_s in (B.2) and (B.3).

B.3 General Procedure

The general procedure followed in this work for parameter extraction from conductance measurements is as follows:

1. High- and low-frequency C–V curves are measured, and C_i, N_{dop}, and $\psi_s(V_g)$ are determined as described in Appendix A.

2. G_p and C_p are measured as a function of frequency at a bias in depletion or weak inversion (correcting for parasitic effects as described in Appendix A).
3. $\langle G_p \rangle / \omega$ versus ω is determined from (B.1).
4. A theoretical $\langle G_p \rangle / \omega$ versus ω curve is calculated from (B.17), using initial guess values for D_{it}, σ_p, σ_n, and σ_s.
5. D_{it}, σ_p, σ_n, and σ_s are determined by varying their values using a non-linear least-squares solver (Levenberg–Marquardt) in order to minimise the mean squared error between the measured and modelled $\langle G_p \rangle / \omega$ versus ω.
6. Steps 2–5 are repeated to determine D_{it}, σ_p, σ_n, and σ_s for a range of energies in the bandgap.

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