Appendix A
Third Quadrant DC Output Characteristics of Low Voltage Trench MOSFETs

The advantages of higher switching frequencies in SMPS cannot often be realized due to switching losses. Thus, a fundamental understanding of switching transients has become a key goal to future optimal high frequency SMPS designs.

Today, device modeling and circuit simulators are fundamental tools to carry out transient analysis and power loss calculations of rather complex nonlinear networks. For the synchronous buck converter used in VR applications, major concerns are the power losses generated in the SyncFET, particularly, reverse recovery and conduction losses in the body diode. Several studies on these loss contributions have been published, stating the importance of reducing them and proposing techniques to achieve it. However, in order to come up with effective measures to mitigate SyncFET losses, further insights of the third quadrant operation are required.

This section deals with large die size trench MOSFETs for high current, high frequency applications, aiming at a comprehensive study of the device static behavior in the third quadrant. The investigations demonstrate that body diode conduction is strongly influenced by significant sub-threshold reverse channel conduction. This intrinsic effect is fundamental and allows explaining some switching transient behavior, as it shall be seen in Appendix B. Therefore, the inclusion of the third quadrant output characteristics in any circuital MOSFET model leads to a more accurate device description and improved power loss predictions.

A.1 DC Output Characteristics

Semiconductor manufacturers typically specify the DC output characteristics of power MOSFETs in datasheets, i.e., drain current i_D vs. voltage v_{DS} at different v_{GS} voltages. Yet, such specification only refers to the operation in the first quadrant, i.e., positive v_{DS} voltage. Regarding the third quadrant, i.e., voltage v_{DS} is negative, only the body diode forward characteristic is usually specified for zero volts v_{GS}. No further information about the channel current in the third quadrant and its v_{GS} dependence is provided.

T. López et al., *Voltage Regulators for Next Generation Microprocessors,*
DOI 10.1007/978-1-4419-7560-7, © Springer Science+Business Media, LLC 2011

In circuit simulations where this information may be relevant, it is usually assumed that the first and third quadrants are symmetric and that the body diode forward characteristic is independent on v_{GS} [1, 2]. As shown in Fig. A.1, such assumption is not always valid. The plot depicts experimental results corresponding to the output characteristics of an N-channel power trench MOSFET (PHB96NQ03LT) for VR applications. The main characteristics of the measured device are:

- Maximum drain current $i_D = 75$ A.
- Maximum drain-to-source voltage $v_{DS} = 25$ V.
- 5 mΩ R_{DSon} at gate-to-source voltage $v_{GS} = 10$ V and junction temperature $T_j = 25°C$.
- Typical gate-to-source threshold voltage ($i_D = 1$ mA, $v_{DS} = v_{GS}$) $V_{GS(th)} = 1.5$ V at $T_j = 25°C$.

Note that the measurements are performed with a curve tracer featuring fast measurement acquisition times (<150 μs for each v_{GS} trace) and therefore self-heating effects in the device under test are minimized.

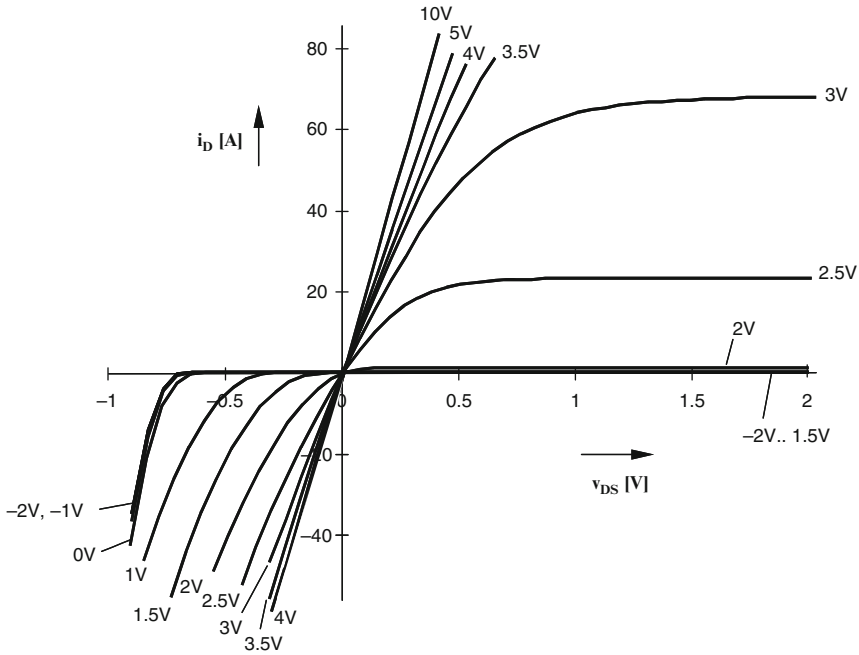

Fig. A.1 Measurement results of the output characteristics of a trench MOSFET device (PHB96NQ03LT from NXP Semiconductors). First and third quadrants are depicted for various v_{GS} at 25°C

From the measurement results it can be observed that:

- The body diode forward characteristic seems to be modulated by voltage v_{GS} in the sub-threshold region, even at negative v_{GS} values down to -1 V.
- At a given v_{GS} in the threshold region (i.e., voltage v_{GS} close to $V_{GS(th)}$), the drain current magnitude in the third quadrant is much larger than that in the first quadrant, also at low v_{DS}. For instance, at $v_{GS} = 2$ V and $v_{DS} = -0.5$ V the drain current reaches -40 A. In the first quadrant however, the maximum drain current at the same v_{GS} is about only a few amps.
- A symmetric characteristic between the first and third quadrant appears to be at high v_{GS}.

This characteristic behavior is not exclusive of trench MOS technologies as it may also occur in other types of vertical MOSFETs such as DMOS, CoolMOS^{TM}, and planar structures.

In the following subsections the third quadrant output characteristics is described in more detail by looking at the internal structure of the device and analyzing the origin of this significant reverse current conduction.

A.2 Device Physics Simulations vs. Measurement Results

MEDICI simulations are carried out to get further insights into the device's fundamental behavior in the third quadrant output characteristics. Current flow lines and carrier concentrations are analyzed under specific boundary conditions. MEDICI is based on a method approach to simulate complex semiconductor structures. A wide variety of device technologies like vertical MOSFETs can be analyzed. In this study, a trench MOS cell geometry corresponding to the PHB96NQ03LT device is modeled. Due to the symmetry of the structure, only half of the trench is modeled. The width of the channel (i.e., the third dimension) is supposed to be very large.

Figure A.2 compares measurement and simulation results of the DC output characteristics of the trench MOSFET. Note that the simulation data are scaled to the corresponding size of the MOSFET die. Package resistance is not included. The good matching between simulation and measurement demonstrates the high accuracy that the device physics simulator can offer with the simplified 2D geometrical representation.

A.3 Comparison of the First and 3Q DC Output Characteristics

Figures A.3 and A.4 represents 2D numerical simulated results in 3D graphs of the first and third quadrant DC output characteristics, respectively. The drain current difference between the first and third quadrant is depicted in Fig. A.5. For the

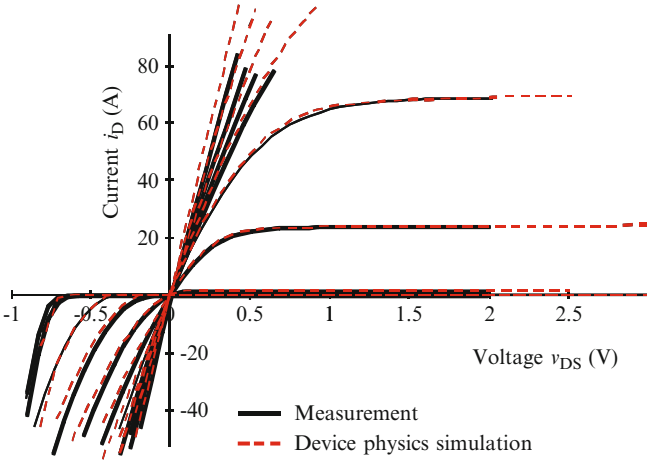

Fig. A.2 Comparison between the measurement and simulation of the output characteristics of a trench MOSFET device (PHB96NQ03L from NXP Semiconductors). First and third quadrants are depicted for various v_{GS}. Both measurement and simulation refer to 25°C

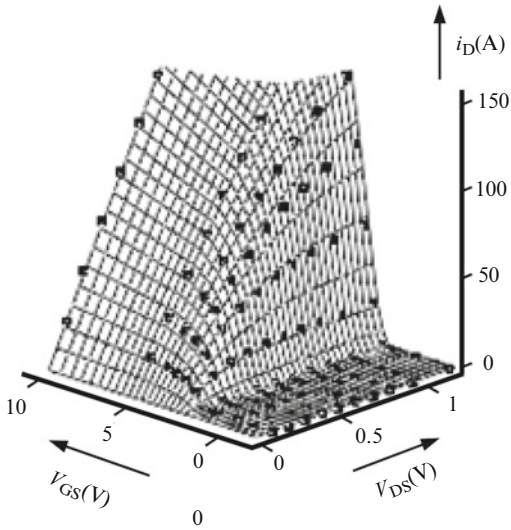

Fig. A.3 Simulated 3D representation of the first quadrant DC output characteristics of a trench MOSFET device (PHB96NQ03LT from NXP Semiconductors) at 25°C

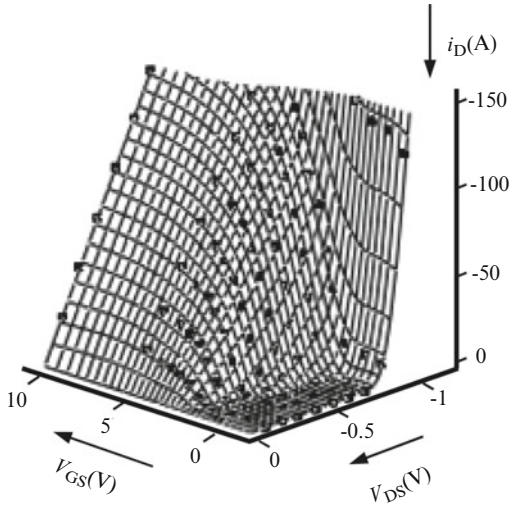

Fig. A.4 Simulated 3D representation of the third quadrant DC output characteristics of a trench MOSFET device (PHB96NQ03LT from NXP Semiconductors) at 25°C

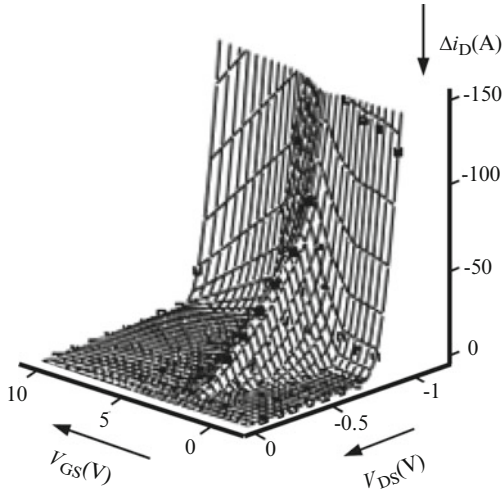

Fig. A.5 Simulated 3D representation of the current difference between third and first quadrant of the DC output characteristics of a trench MOSFET device (PHB96NQ03LT from NXP Semiconductors) at 25°C. Note that for the representation, the first quadrant is mirrored into the third quadrant

representation, the first quadrant current is mirrored onto the third one. Current difference Δi_D is therefore obtained by applying,

$$\Delta i_D = i_{D3Q} - i_{D1Q}|_{3Q}. \tag{A.1}$$

Current i_{D3Q} is the third quadrant drain current and $i_{D1Q}|_{3Q}$ the first quadrant drain current mirrored into the third quadrant.

Figure A.5 shows that the difference in current conduction between the first and third quadrants is not only caused by the body diode conduction above 0.7 V, but also due to a significant current modulated by v_{GS} in the threshold and subthreshold regions.

A further comparative study of the first and third quadrant can be made by representing the measurement results of Fig. A.1 in the way shown in Fig. A.6. Every curve in the graph corresponds to a specific drain current value and shows the required v_{GS} level to keep the drain current constant as function of v_{DS}. Therefore, the curves represent the switching trajectories of an inductive load application where the current is impressed into the devices rather than the voltage.

According to the trajectories, in the first quadrant every curve is expected to flatten out as the device enters the active region and v_{DS} rises. Each v_{GS} value where the curve saturates corresponds to a specific point in the MOSFETs transfer curve. Though, in the third quadrant, the curves do not flatten but continue to decrease even further. Thus, reverse current conduction occurs below the first quadrant threshold voltage and below the conventional body diode forward

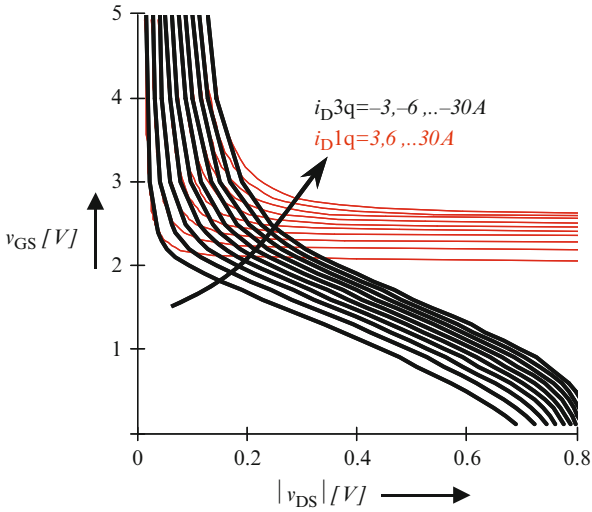

Fig. A.6 Representation of the gate-to-source voltage required to keep a certain drain current constant at different drain-to-source voltages. Comparison between the first (i_D1Q) and third quadrant (i_D3Q) operation. Measurement results at 30°C. MOSFET: PHB96NQ03LT from NXP Semiconductors

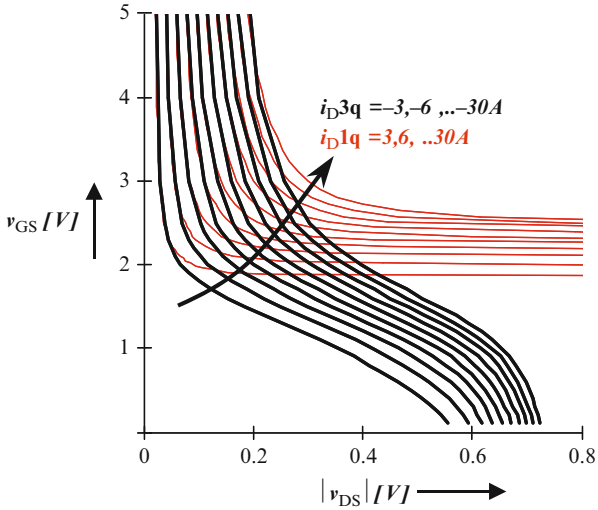

Fig. A.7 Representation of the gate-to-source voltage required to keep a certain drain current constant at different drain-to-source voltages. Comparison between the first (i_D1Q) and third quadrant (i_D3Q) operation. Measurement results at 125°C. MOSFET: PHB96NQ03LT from NXP Semiconductors

voltage conduction. A drain current value in the active region of the first quadrant at a given v_{GS} is therefore always lower than that in the third quadrant for the same v_{GS}.

At low v_{DS} the MOSFET enters the ohmic region, leading to a symmetric behavior between the first and the third quadrant.

Figure A.7 shows measurement results at 125°C. Temperature affects MOSFET parameters such as R_{DSon}, threshold voltage, and forward diode conduction. The positive thermal coefficient of the R_{DSon} makes the MOSFET to be in the ohmic region at higher v_{DS} with increased temperature. The threshold voltage reduction as temperature rises is reflected in the third quadrant curves by a reduction of v_{GS} in the active region. The negative thermal coefficient of the body diode forward voltage curve makes the diode current to be relevant at lower v_{DS} (absolute values) in the third quadrant.

A.4 3Q Current Flow Through a Trench Cell

The aim of the following simulations is to study the current flow in the third quadrant of the output characteristics. For this purpose, two important aspects are considered. First, the amount of electrons and holes that carry the current, and second the trench cell regions from which carriers flow. Figure A.8 depicts the ratio of electron to hole current at the drain ($q_{eh,\ drain}$) and source ($q_{eh,\ source}$) electrodes as function of $-v_{DS}$ (i.e., source-to-drain voltage) and for various v_{GS}. The results

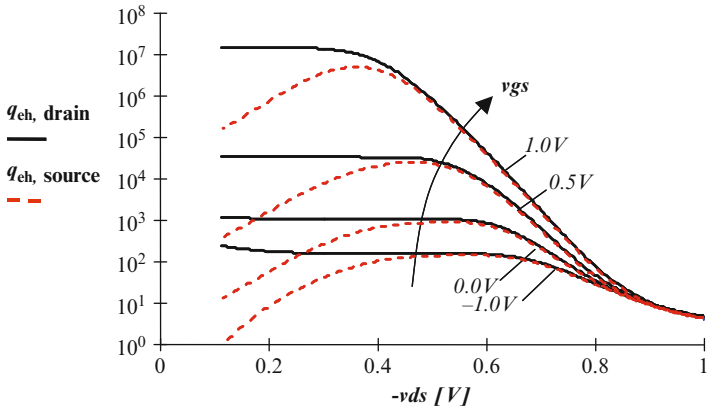

Fig. A.8 Ratio of electron to hole current at the drain and source contacts. Device: PHB96NQ03LT from NXP Semiconductors. Temperature: 25°C

Table A.1 Simulated electrical conditions for the current flow line graphs

Voltage v_{DS} (V)	Voltage v_{GS} (V)	Current i_D (A)
−0.1	0	-400×10^{-12}
	1	-32×10^{-6}
−0.4	0	-30×10^{-6}
	1	−1.2
−0.8	0	−13.8
	1	−42

demonstrate that the major contributors to current flow are electrons rather than holes, not only at the drain but also at the source electrode at moderated $-v_{DS}$ and with increasing v_{GS}. At high $-v_{DS}$, i.e., the body diode fully conducts, holes play an important role in current conduction, both at the drain (as minority carriers) and source electrodes. The electron to hole current ratio decreases at low $-v_{DS}$.

The current distribution through the trench cell is investigated under the six different electrical conditions of Table A.1. The drain current refers to Fig. A.2. The v_{GS} values are within the subthreshold region. Three different v_{DS} voltages are applied. Corresponding current flow lines and electron concentration are depicted in Figs. A.9–A.14.

Figure A.9 indicates the location of the gate, drain, and source electrodes as well as body region in the MOSFET cell. The *Y*-axis corresponds to the trench cell depth direction, whereas the *X*-axis refers to the cell length direction. The length of half trench cell is 2 μm. The trench cell depth including substrate and metallization is 6 μm. The trench depth is 1.5 μm. Source and body are shortened at the surface with a metal contact (i.e., source electrode).

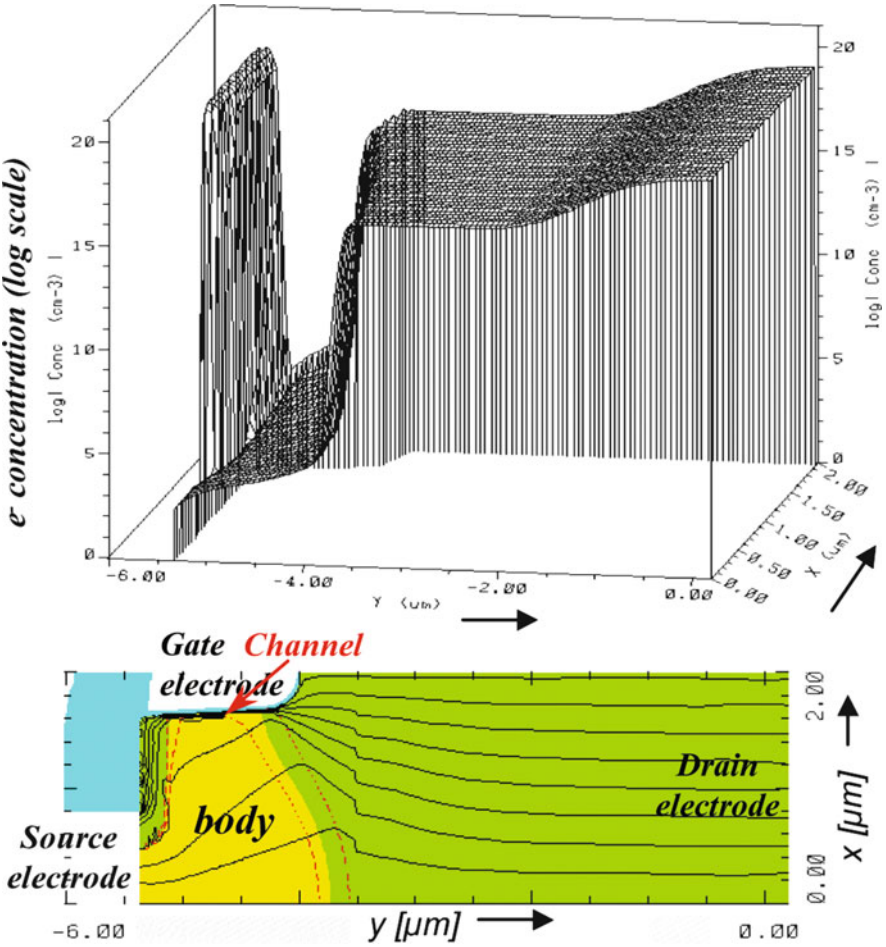

Fig. A.9 2D numerical simulation of a half trench MOSFET cell. Subthreshold electron concentration and current flow lines graphs at $v_{GS} = 0$ V and $v_{DS} = -0.1$ V. Note that simulated currents are specified in A/mm^2

The electron concentration and current flow lines graph show for every electrical condition how current distributes through the cell structure, i.e., the current distribution through body diode and channel regions.

In the simulation of Fig. A.9 ($v_{DS} = -0.1$ V, $v_{GS} = 0$ V), only a few hundred picoamps flow. Current flow lines indicate that this small amount of current is distributed through both body diode and channel regions even though the inversion channel layer is not yet formed. Although the channel region is much smaller than the body region, most of the flow lines are concentrated at the surface, showing that an important percentage of the total current is due to channel conduction. This is in agreement with the electron concentration graph showing

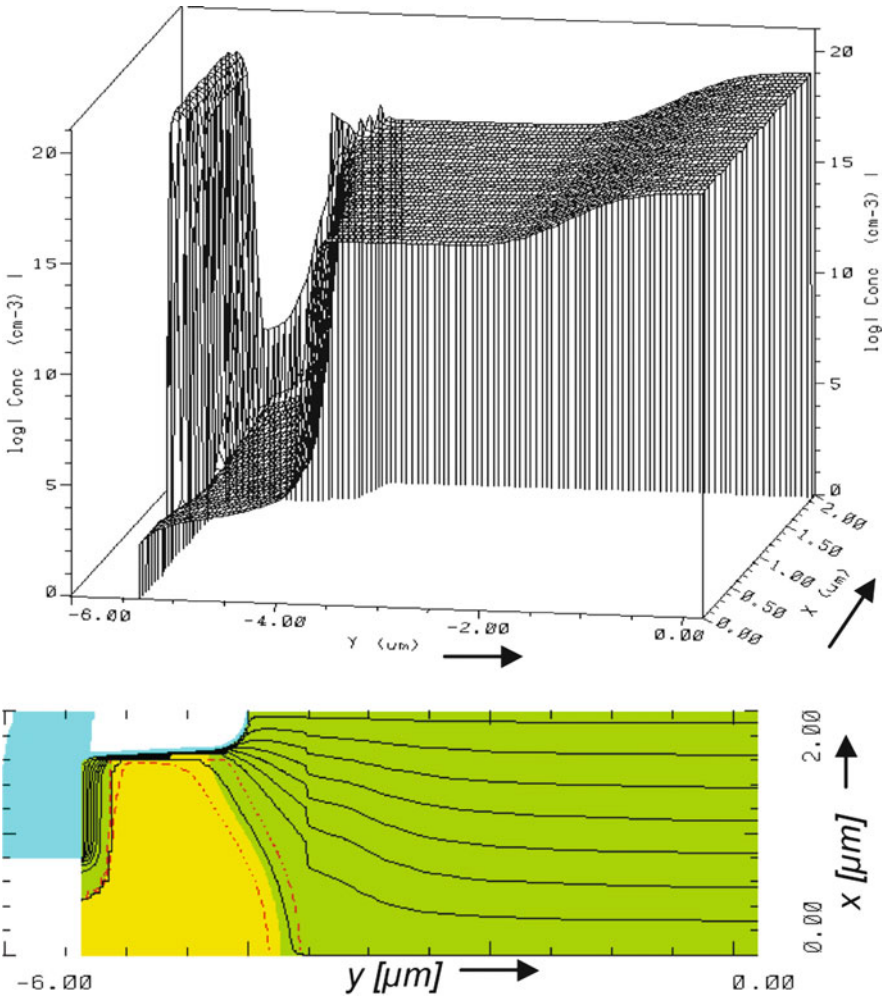

Fig. A.10 2D numerical simulation of a half trench MOSFET cell. Subthreshold electron concentration and current flow lines graphs at $v_{GS} = 1$ V and $v_{DS} = -0.1$ V

the presence of a higher electron concentration in the channel than in the body region.

Figure A.10 shows the result of increasing voltage v_{GS} from 0 to 1 V. The total current is still low but has increased to some tens of microamps. The electron concentration graph shows that there has been an increase of electrons in the channel region, whereas the electron concentration in the body region remains virtually constant. This indicates that the total current increase is caused by channel conduction. Since the positive v_{GS} depletes the channel of holes, the majority current carriers are conduction electrons in that region.

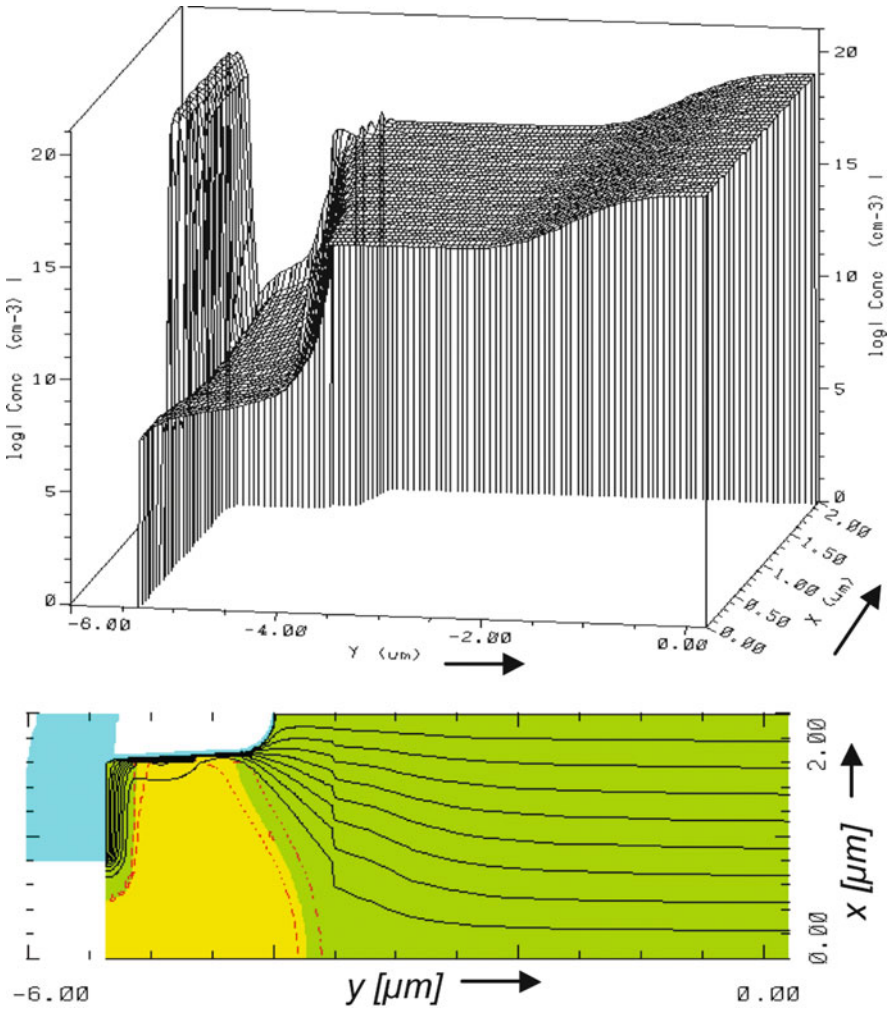

Fig. A.11 2D numerical simulation of a half trench MOSFET cell. Subthreshold electron concentration and current flow lines graphs at $v_{GS} = 0$ V and $v_{DS} = -0.4$ V

A similar behavior can also be observed at $v_{DS} = -0.4$ V from Figs. A.11 and A.12. A higher electron concentration in the channel than in the body region already occurs at $v_{GS} = 0$ V, indicating that the drain current mainly flows through the channel. The difference in work functions between the body and gate materials (semiconductor and metal, respectively) generates a partial depletion of holes in the channel. This is the reason why free electrons are likely concentrated in the channel region rather than in the body even without any external positive gate-to-source potential [3]. The drain current increases dramatically above 1 amp as soon as v_{GS} is increased from 0 to 1 V since a large number of free electrons from the drain are

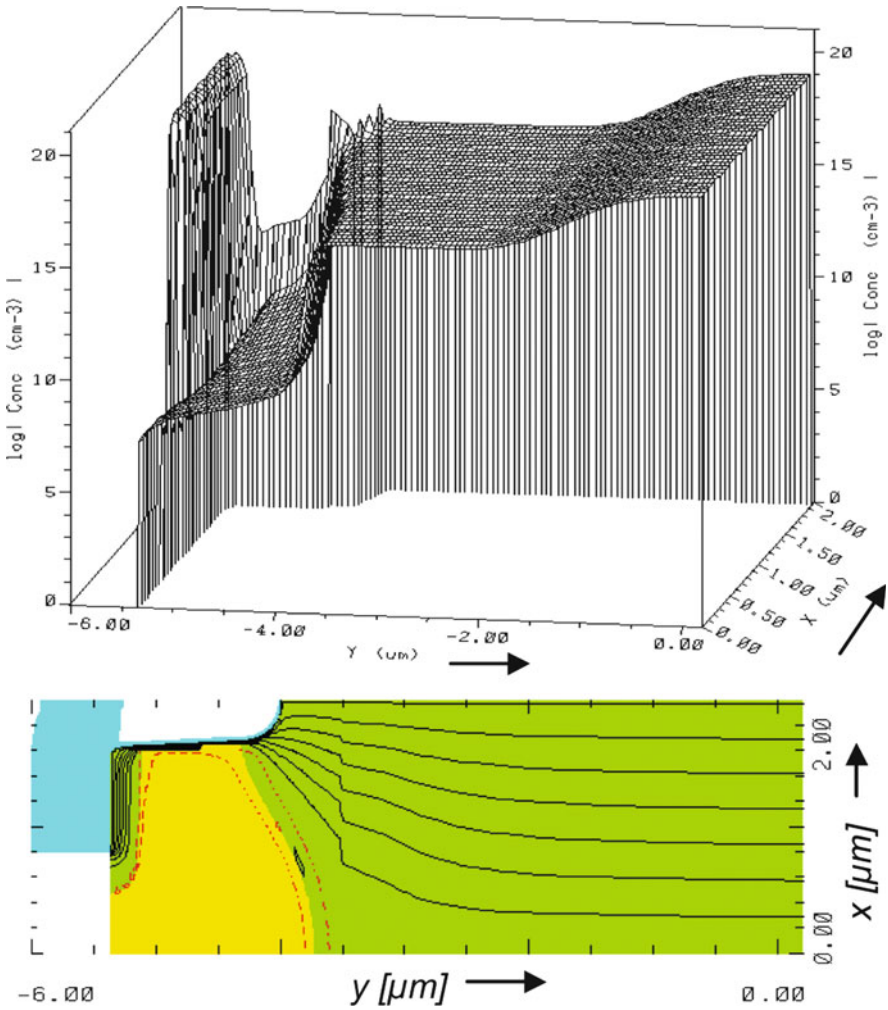

Fig. A.12 2D numerical simulation of a half trench MOSFET cell. Subthreshold electron concentration and current flow lines graphs at $v_{GS} = 1$ V and $v_{DS} = -0.4$ V

attracted to the channel. Again, the drain current rise is essentially caused by an increase of electron concentration in the channel.

High drain current results from applying a forward voltage of 0.8 V across the body diode. This is depicted in Fig. A.13. Voltage v_{GS} is kept at zero volts during the simulation. Figure A.14 shows the results of applying 1 V v_{GS}. The electron concentration in the body region is approximately equal to that for $v_{GS} = 0$ V, whereas the electron concentration in the channel region has increased. This results in a total current of 42 A (28.2 A higher than in case of $v_{GS} = 0$ V). The drain current has been amplified by 3 due to channel electron conduction.

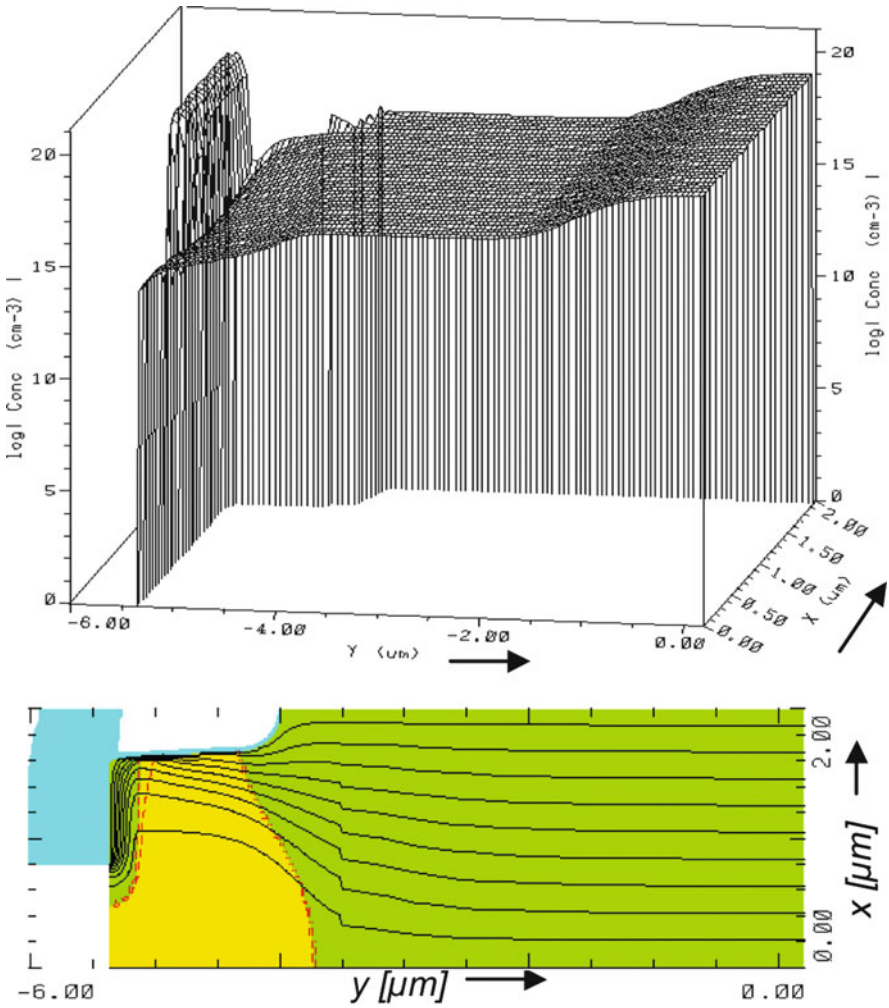

Fig. A.13 2D numerical simulation of a half trench MOSFET cell. Subthreshold electron concentration and current flow lines graphs at $v_{GS} = 0$ V and $v_{DS} = -0.8$ V

These simulation results demonstrate that the drain current in the third quadrant of the output characteristics is characterized by electron conduction in the channel region, which is modulated by the gate-to-source voltage at even values below threshold. This is in agreement with [4, 5]. The body diode current becomes important when it is forward biased with voltages above 0.7 V (at 25°C). Below this voltage value, the drain current is essentially caused by channel electron conduction.

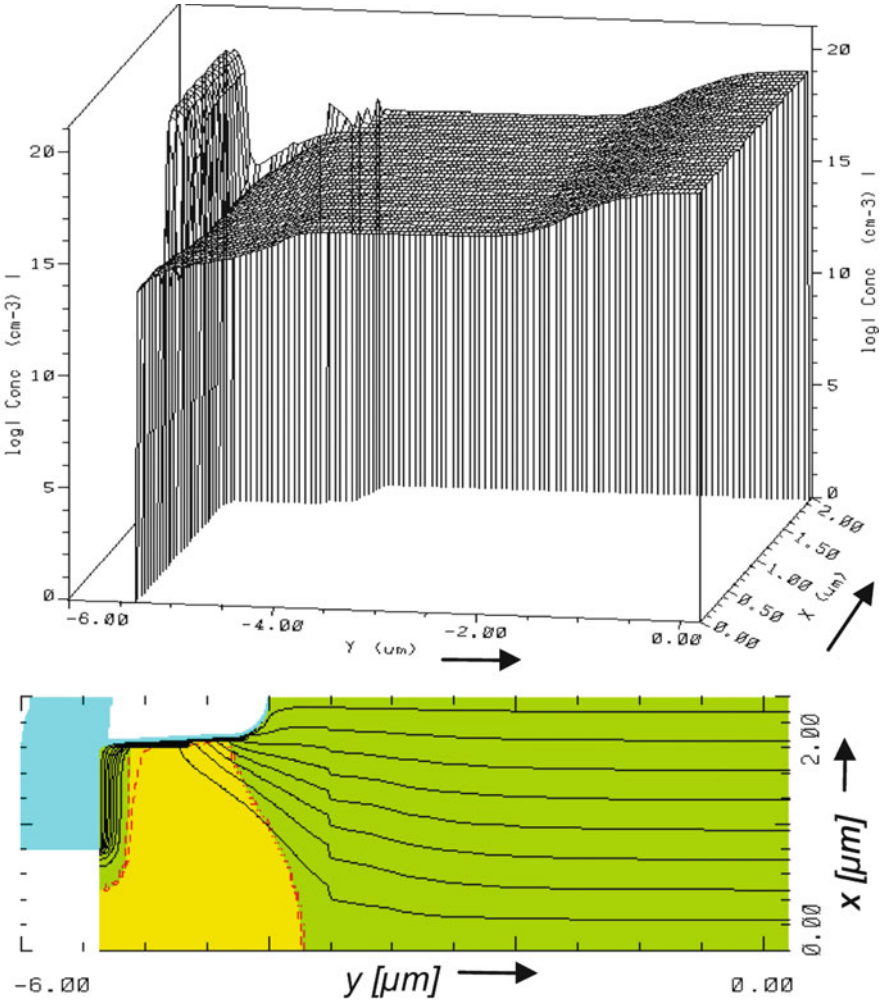

Fig. A.14 2D numerical simulation of a half trench MOSFET cell. Subthreshold electron concentration and current flow lines graphs at $v_{GS} = 1$ V and $v_{DS} = -0.8$ V

References

1. Ferreira A, Castro Simas MI (1991) Power MOSFETs reverse conduction revised. In: IEEE proceeding on power electronics specialists conference, PESC 1991, pp 416–422
2. Castro Simas MI, Costa Freire J (1994) CAD tools to optimise power MOSFET performance using channel reverse conduction. IEEE Trans Power Electron 9(5):522–531
3. Grant DA, Gowar J (1989) Power MOSFETs. Theory and applications. Wiley, New York
4. Dolny GM, Sapp S, Elbanhaway A, Wheatley CF (2004) The influence of body effect and threshold voltage reduction on Trench MOSFET body diode characteristics. In: IEEE

international symposium on power semiconductor devices and ICs, ISPSD 2004, pp 217–220
5. Sun NX, Huang AQ. The impact of sub-threshold current on ultra high density Trench MOSFET for synchronous rectifier application. In: IEEE international symposium on power semiconductor devices and ICs, ISPSD 200, pp 358–361
6. Maxim A (1998) The analog behavioural SPICE macro modelling – a novel method of power semiconductor devices modelling. IEEE Trans Power Electron
7. Lauritzen P, Ma C (1991) A simple diode model with reverse recovery. IEEE Trans Power Electron 6(2):188–191
8. Tolle T, Duerbaum T, Elferich R, López T (2003) Quantification of switching loss contributions in synchronous rectifier applications. In: European power electronics, EPE 2003
9. Djekic O, Brkovic M (1997) Synchronous rectifiers vs. Schottky diodes in a buck topology for low voltage applications. In: IEEE proceeding on power electronics specialists conference, PESC 1997, vol 2, pp 1374–1380
10. Bridge CD (2002) Control method to reduce body diode conduction and reverse recovery losses. Patent No. US 6396250 B1, 28 May 2002

Appendix B
Reverse Recovery in LV Trench MOSFETs

The optimization of power MOSFETs for high-frequency power converters needs a precise description of their dynamic behavior and the impact in the application. Circuit simulators are effective to analyze switching transients of power converters, yet they require accurate models to assess the device performance. This section presents a reverse recovery model for low voltage trench MOSFETs [1].

A simple lumped model approach is employed to represent the dynamics of diffusion and recombination processes of the MOSFETs intrinsic body diode. The parameters of the model are adjusted from reverse recovery waveforms resulting from rather accurate device physics simulations or, alternatively, from measurements. In either way, the required body diode diffusion current is extracted from the drain terminal current. This involves the identification of both channel current and MOSFET capacitance current, which are superimposed to the body diode diffusion current.

Channel conduction is manifested by the so-called "body effect" [2, 3] even though the gate voltage is well below the nominal threshold voltage of the device (see Appendix A). This channel current is proven to have a significant impact in the reverse recovery transient curves as it provides an alternative low ohmic path to the drain current. Device physics simulations reveal the existence of this channel conduction. Further, internal circulating currents between the body diode and channel regions exist that cannot be observed from the terminals. The de-embedding of the drain current forms the basis of a curve fitting procedure to derive the parameter values of the diode model. Device physics simulations validate the performance of the proposed reverse recovery representation.

B.1 Impact of the Body-Effect in Reverse Recovery Transients

According to the description of Appendix A, the effective threshold voltage reduction in the third quadrant conduction observed in the DC output characteristics of MOSFETs is consequence of the body-effect.

The DC current in the third quadrant may therefore result from two main carrier transport phenomena; namely, diffusion of minority carriers in the body diode, and

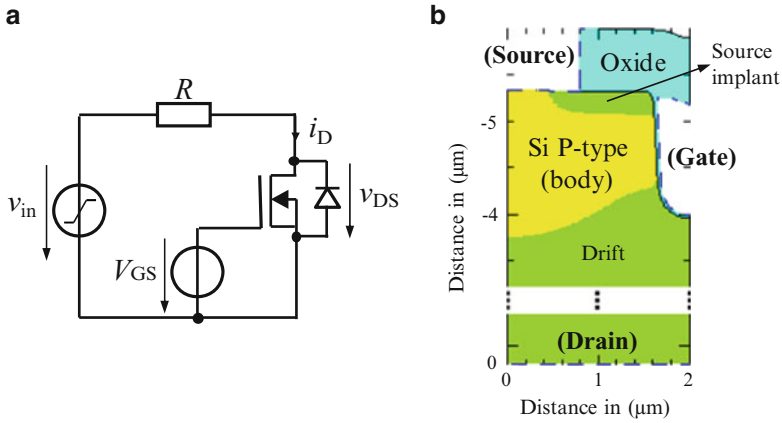

Fig. B.1 (**a**) Resistive load reverse recovery circuit diagram. (**b**) 2D representation of the simulated half-trench MOSFET cell

drift of majority carriers in the channel even though the gate voltage may be lower than the nominal threshold voltage (V_{TH0}).

This static characteristic behavior has a major impact on the dynamics of reverse recovery. First, the reverse recovery current is observed to be strongly dependent on the gate voltage in the subthreshold region because the stored charge is affected by a split of the drain current between the channel and body diode regions prior to switching. And second, since the diffusion current during reverse recovery may alternatively flow through the channel, an internal circulating current flow may arise that reduces the external drain current. Thus, the measured reverse current at the drain terminal may appear significantly lower than the actual internal body diode current.

Figure B.1 illustrates the impact of the body-effect in the reverse recovery curves. The data results from device physics simulations corresponding to the resistive reverse recovery setup and trench cell structure of Fig. B.2. Current and voltage waveforms are shown at three different gate voltage biases. Furthermore, current flow lines through the MOSFETs cell are depicted at various time instants for investigations on the current distribution.

As observed in the time dependent graphs, the reverse current conduction[1] in the three considered cases are significantly different, being the simulation at $V_{GS} = -5$ V the one with the longest reverse current time, and the simulation at $V_{GS} = 1$ V with the shortest. The current flow lines reveal that, in the latter case, the drain current flows almost entirely through the channel region prior to switching. Since no diffusion current is present, the reverse current during the transient is uniquely

[1]Reverse current conduction refers to the body diode. Thus, this happens when the drain current is positive.

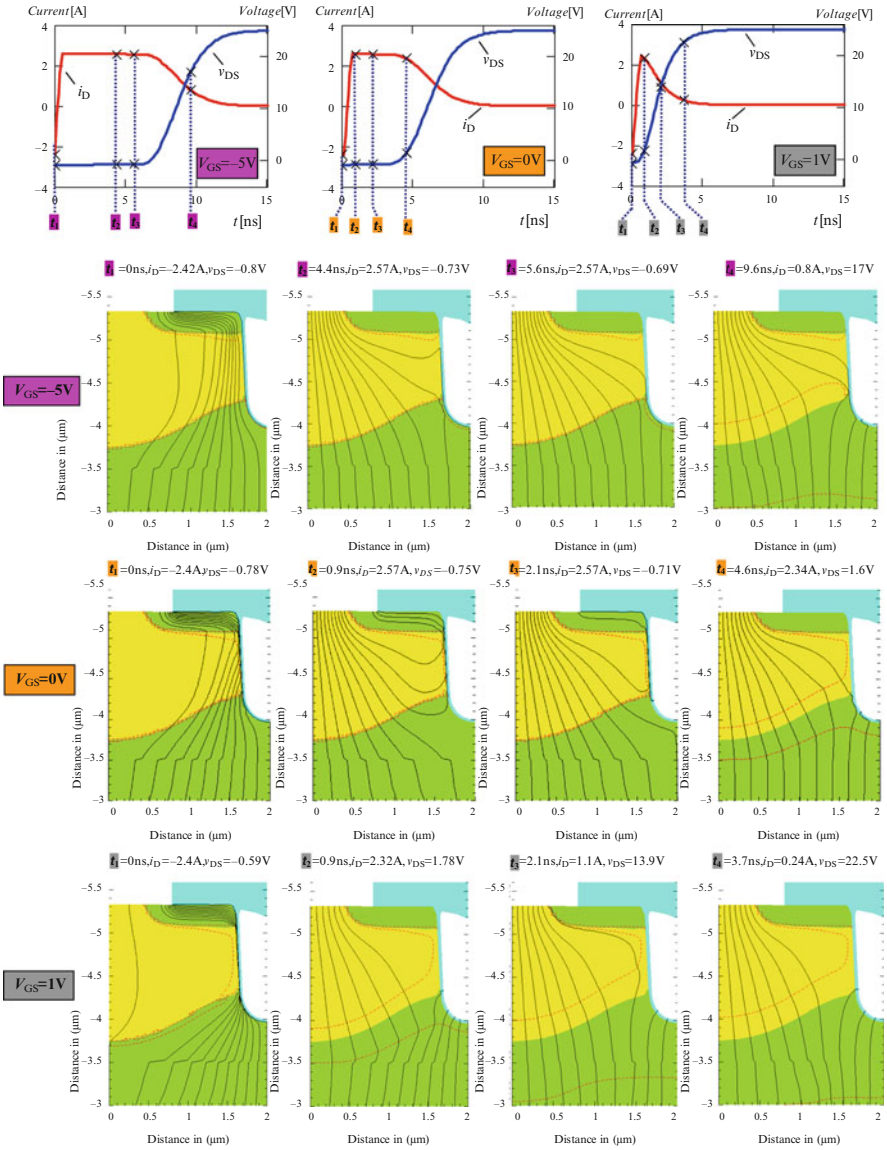

Fig. B.2 Resistive reverse recovery transient curves and current flow lines for various gate voltages. Data result from 2D device physics simulations of the trench cell of Fig. B.2b with a scale factor corresponding to a 1 mm^2 active area. Steady-state conditions prior to switching correspond to those at time t_1

caused by the output capacitance charge, i.e., the depletion capacitance of the body diode and the gate-to-drain oxide capacitance. Voltage V_{DS} rapidly rises when the current reverses, which causes the channel to block. Prior to switching at $V_{GS} = -5$ V, the drain current entirely flows through the body diode, i.e., the inversion layer is not formed. During reverse conduction, current flows from drain-to-source through the body region as the drain-to-source voltage remains virtually constant at -0.7 V, which is a clear indication of current flow due to diffusion of minority stored charges.

The current flow lines at $V_{GS} = 0$ V indicate that the drain current flows through both body diode and channel regions. Thus, the reverse current caused by charge diffusion is lower than in case of $V_{GS} = -5$ V, as the initial forward current through the body diode is lower. It is further observed that an internal circulating current flows between channel and body diode during reverse current conduction. Some of the flow lines cross the p–n junction from the body diode to the drift region and return to the source through the channel, which is conducting since V_{DS} remains negative. Other flow lines do not cross the p–n junction to get into the drift region, but trace a circulating path through the body region, channel, source implant, and source metallization. It is therefore expected that the internal diffusion current is higher than the current at the drain terminal. When the body diode blocks, V_{DS} rises and the drain current is predominantly capacitive.

B.2 Reverse Recovery Circuit Model

The main purpose of this section is to present a behavioral model that represents reverse recovery transients according to the description given in the previous section. The proposed model reproduces the MOSFET operation as the sum of the diffusion and drift carrier transport phenomena, as well as the capacitance current. The resulting circuit diagram is depicted in Fig. B.3. The three current contributors are independently modeled as described in [1].

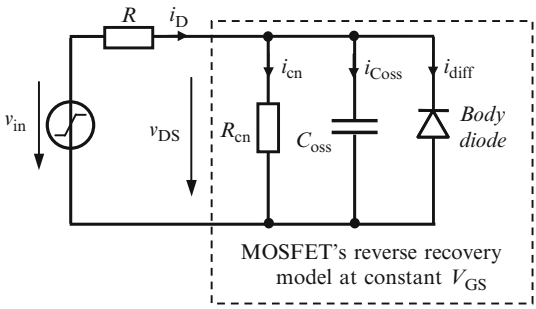

Fig. B.3 Circuit diagram of the resistive load reverse recovery and MOSFETs equivalent circuit

The output capacitance shown in Fig. B.4 is obtained from device physics simulations by means of voltage ramp transients. The resulting data are table-based represented in the circuit simulator.

For modeling the channel conduction in the third quadrant, the following assumption based on the body-effect is taken: the increase of drain current when the gate voltage rises is merely due to an increase of channel conduction. According to this, channel and body diode current can be distinguished from the output characteristics. That is, in the third quadrant there exists a gate voltage below which the drain current gets independent of. Such drain current curve corresponds to the diode current. The difference between the body diode current and the total drain current is thus the channel current. Figure B.5 shows the de-embedding of both channel and body diode currents for the present case study. As it is depicted, the channel current reaches maximum values at V_{DS} below −0.7 V, and tends to zero at strong body diode conduction. The resulting channel curve at a low current level is shown in the diagram of Fig. B.6 in comparison to the predicted curve resulting from applying the body-effect theory [4]. The theoretical curve is very

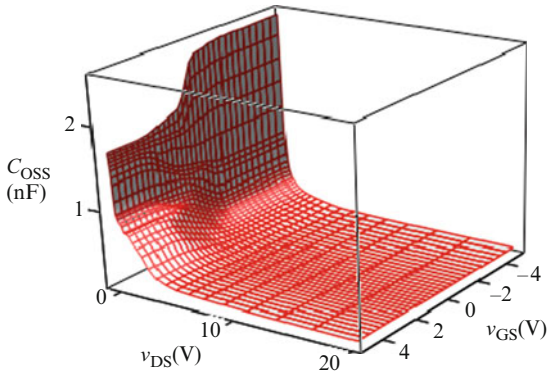

Fig. B.4 MOSFETs output capacitance. Data result from 2D device physics simulations of the trench cell of Fig. B.2b with a scale factor corresponding to a 1 mm^2 active area

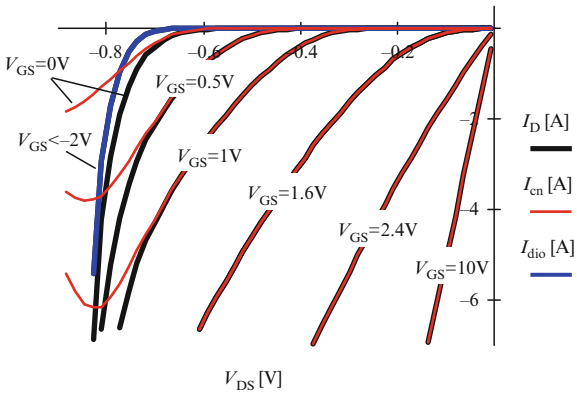

Fig. B.5 Third quadrant output characteristics. Drain current de-embedding. Data result from 2D device physics simulations of the trench cell of Fig. B.2b using a scale factor corresponding to a 1 mm^2 active area

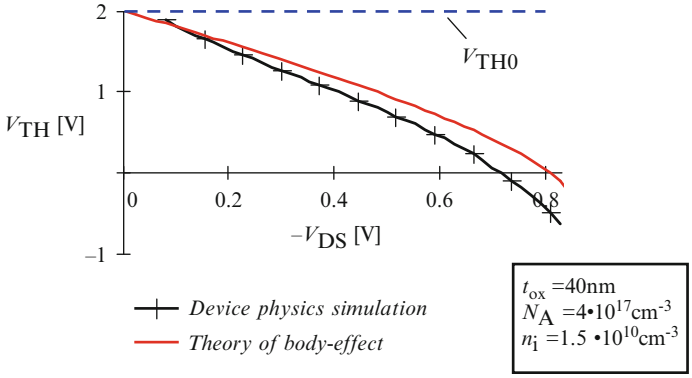

Fig. B.6 Effective third quadrant threshold voltage reduction. Comparison between device physics simulations and body-effect theory

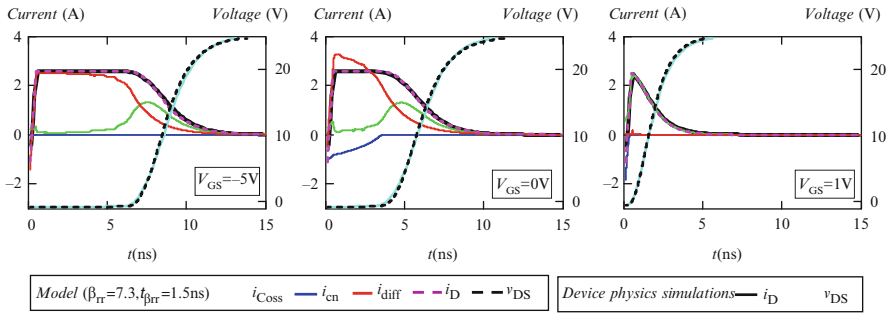

Fig. B.7 Comparison of resistive reverse recovery curves resulting from device physics simulations (Fig. B.1) and SPICE simulations of the proposed behavioral model

sensitive to the concentration of holes N_A in the body region. The high nonuniformity of this concentration in the simulated trench cell makes it difficult to assign a uniform equivalent value assumed in the theory. The channel behavior is modeled in a circuit simulator by means of a curve fitting function (Fig. B.7).

Finally, the body diode diffusion current is modeled employing the following empiric equation based on [5],

$$i_{\mathrm{diff}}(t) = \beta_{\mathrm{rr}} \cdot I_{\mathrm{dio}}(v_{\mathrm{DS}}(t)) + \frac{1}{t_{\beta\mathrm{rr}}} \int \left[I_{\mathrm{dio}}(v_{\mathrm{DS}}(t)) - i_{\mathrm{diff}}(t) \right] \mathrm{d}t + \cdots + I_{\mathrm{diff0}}, \qquad \text{(B.1)}$$

where I_{dio} is the body diode static characteristics (see Fig. B.5), I_{diff0} is the initial condition of the integral, and β_{rr} and $t_{\beta\mathrm{rr}}$ are fitting parameters. As done for the channel current, I_{dio} is modeled in the circuit simulator using a curve fitting function.

Figure B.6 shows reverse recovery transient curves resulting from both device physics- and circuit simulations. Parameters β_{rr} and $t_{\beta\mathrm{rr}}$ are adjusted to best match the device physics-simulated curves. Regarding voltage and current waveforms, the

simple body diode model together with the channel and capacitance data agree with the device physics simulation approach. For the case of $V_{GS} = 0$ V, circuit simulation predicts and quantifies the internal circulating current between channel and diode, which results in a body diode current peak higher than the drain current.

As described in [1], the reverse recovery model can also be applied for describing real devices by means of experimental characterization.

B.3 SPICE Simulations of a Synchronous Buck Converter

The effect of channel electron conduction as majority carriers in the third quadrant subthreshold region may impact on both switching and conduction losses in the application. First, because as channel conduction increases, the power loss due to the reverse recovery of the minority mobile stored charge reduces. And second, because v_{DS} voltage drop can be considerably lower than the conventional body diode forward voltage, with a consequent conduction power loss reduction.

The importance of this effect is illustrated by means of SPICE simulations of a synchronous buck converter. Figure B.8 shows the circuit diagram under consideration. For the sake of simplicity, the input and output of the converter is modeled as an ideal voltage and current source, respectively. Values are specified in Table B.1. Note that the parasitic impedance values *Lg*, *Rg*, *Ld*, *Rd*, *Ls*, and *Rs* do not correspond to any particular circuit arrangement (package device, PCB layout, etc.). A table based behavioral macro MOSFET model [1, 6] is applied for modeling in SPICE switches T1 and T2. The required data (i.e., capacitance, channel, and body diode characteristics) are gathered from MEDICI simulations corresponding to the PHB96NQ03LT device. The body diode reverse recovery effect is modeled as proposed in [5] and integrated as a part of the macro model.

The switching interval in which switch T2 turns off and switch T1 turns on is analyzed. In the usual operation, there exists a certain time delay between the T2 turn-off and the T1 turn-on that avoids cross conduction. The body diode of T2 takes over the output current during that delay time. Thus, reverse recovery occurs when T1 turns on and the diode blocks. SPICE simulation results from Figs. B.9 to B.11 illustrate this behavior in detail. In Fig. B.9 (case (a)), driving voltage v_{DRV2} of T2 switches from 10 to 0 V linearly. When v_{GS2} drops down to a sufficiently low value the body diode starts conducting and partially takes over the output current $i0$ (at v_{GS}= 0 V part of the total drain current still flows through the channel in the third quadrant). Voltage v_{GS2} may significantly bounce during current and/or voltage variation due to the gate parasitic impedance, which affects the body diode current. Meanwhile switch T1 is turned on. Driving signal[2] v_{DRV1} switches from 0 to 10 V

[2]The driver signals have not been optimized to reduce power losses in order to avoid effects that are out of the subject. The setup is arranged in a way to illustrate the impact of the third quadrant effect on the application.

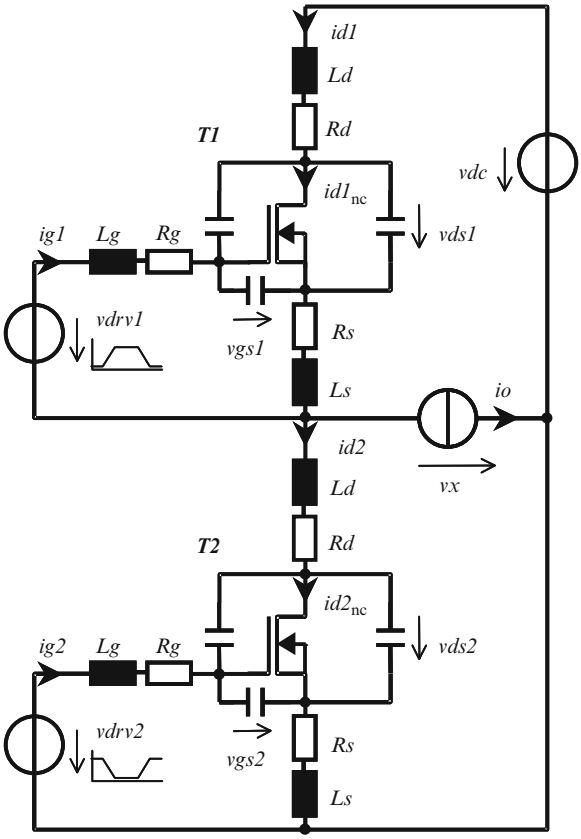

Fig. B.8 SPICE simulation circuit diagram of a synchronous buck converter

Table B.1 Specifications of the synchronous buck converter circuit of Fig. B.8

Operation DC-link voltage output current	DC-link voltage v_{DC}	10 V
	Output current I_o	10 A
Gate circuits (T1, T2)	Total gate inductance L_G	2 nH
	Total gate resistance R_G	1 Ω
Source, drain circuit (T1, T2)	Source inductance L_s	0.5 nH
	Drain inductance L_D	0.1 nH
	Source and drain resistance R_S, R_D	1 mΩ

MOSFETs T1, T2 Channel current and inter-electrode capacitances are functions of (v_{DS}, v_{GS}). The body diode current is a function of (v_{DS}, v_{GS}, t) and comprises reverse breakdown and reverse recovery

linearly in 20 ns. The feedback effect of the source inductance considerably delays the commutation, which is translated in a long quasi-plateau shape in the v_{GS1} waveform. During the Miller plateau voltage v_{DS1} rises and switch T1 conducts the output current. The oscillatory energy generated in the commutation is dissipated in

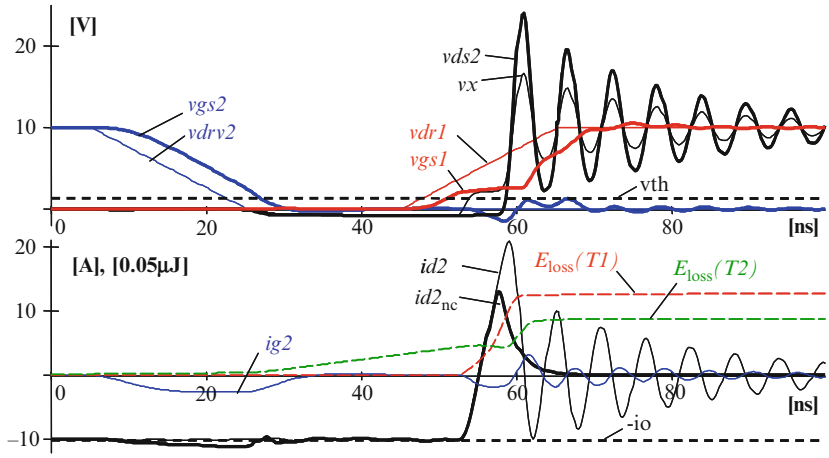

Fig. B.9 SPICE simulations case (a) of circuit diagram of Fig. B.8. Min(v_{DRV2}) = 0 V, max ($id2$) = 20.8 A, max($id2_{nc}$) = 13.4 A (reverse recovery), E_{loss}(T1, T2) = 1.08 μJ, temperature = 25°C

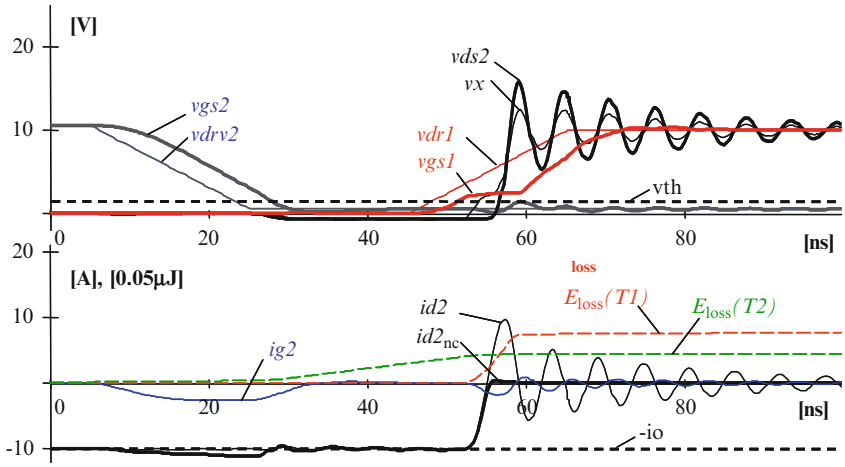

Fig. B.10 SPICE simulations case (b) of circuit diagram of Fig. B.8. Min(v_{DRV2}) = 0.5 V, max ($id2$) = 9.7 A, max($id2_{nc}$) = 0.4 A (reverse recovery), E_{loss}(T1, T2) = 0.61 μJ, temperature = 25°C

the parasitic resistance of the circuit. Note that the maximum peak of the voltage oscillation across v_{DS2} can be considerably high, even enough to cause breakthrough.

The loss energy in body diode and channel can be calculated by the subtraction of the capacitive current from the total drain current, i.e., looking at Fig. B.8 the subtraction leaves $id1_{nc}$ or $id2_{nc}$ [7], and multiplying the result by v_{DS} (i.e., v_{DS1} or v_{DS2} in the proposed example). It provides the power loss in the MOSFET

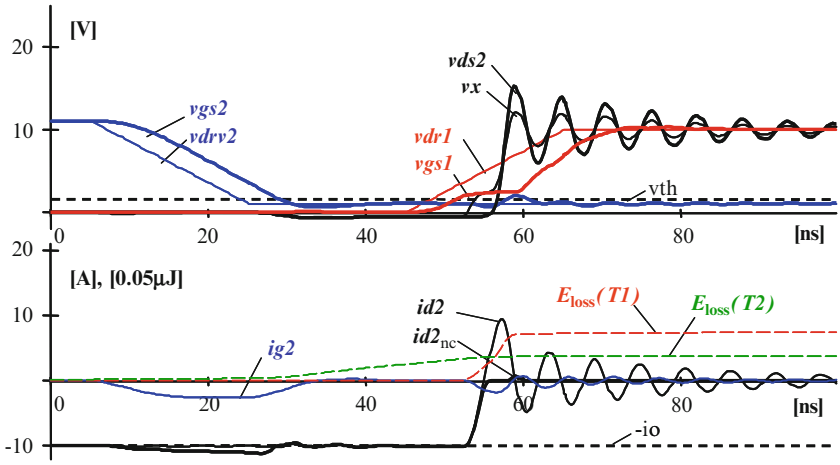

Fig. B.11 SPICE simulations case (c) of circuit diagram of Fig. B.8. Min(v_{DRV2}) = 1 V, max($id2$) = 9.4 A, max($id2_{nc}$) = 0.9 A (gate bouncing), E_{loss}(T1, T2) = 0.56 μJ, Temperature=25°C

excluding the gate, package and pins resistance at a certain instant of time. The loss energy is then obtained by integrating this instantaneous power along the time. In the example, this operation is calculated for switches T1 and T2 at the time interval (0, 100 ns). The resulting loss energy is 1.08 μJ.

In simulation results of Fig. B.9 (case (b)) a DC voltage of 0.5 V is added to the drive signal of switch T2. Therefore the upper limit of v_{DRV2} becomes 10.5 V and the lower limit 0.5 V. This change alone significantly impacts on the switching behavior. Three relevant aspects of the resulting waveforms must be pointed out. First, the positive voltage value across v_{GS2} during the third quadrant operation of switch T2 is sufficiently high to practically eliminate body diode conduction and thus reverse recovery. Note that during the turn-on of T1, v_{GS2} bounces around 0.5 V, always below threshold and above zero volts. Second, the mitigation of reverse recovery current has the direct implication of lowering down current and voltage oscillations, which in turn reduces switching power losses in switch T1 as well as electromagnetic interference (EMI). And third, voltage v_{DS2} during the third quadrant operation is slightly reduced, and so are the conduction losses. The calculated loss energy in this case is 0.61 μJ, which means a 43% reduction in comparison to case (a).

In the simulation of Fig. B.9 (case (c)), the driving voltage offset of switch T2 is further increased to 1 V, so that the lower limit corresponds to 1 V. This value is so critically close to the threshold voltage that a spurious turn on occurs due to gate bouncing voltage [7]. The described effects taking place in case (b) are slightly pronounced. That is, reverse recovery is completely vanished, the amplitude of the oscillations is further reduced and the conduction in the third quadrant is improved. This accounts for a loss reduction of about 48% in comparison to case (a).

B.4 Summary

The third quadrant DC output characteristics of a high density trench power MOSFET is analyzed using measurements, 2D numerical simulations, SPICE, and a table base macro MOSFET model. In contrast to the first quadrant conduction, a substantial third quadrant current in the threshold and subthreshold regions is observed in measurements and analyzed in simulations. This asymmetric current is essentially caused by channel electron conduction and not by body diode conduction. The repercussions of this effect in the application are illustrated with switching transient simulations of a synchronous buck converter in SPICE. The example demonstrates that the third quadrant output characteristics may strongly influence the converter behavior, up to the point where relevant issues such as reverse recovery, hard switching losses, and EMI can be reduced or even vanished. Therefore, the inclusion of the third quadrant output characteristics in circuital MOSFET models is a step forward to better understand and predict switching transients in SMPS.

The reverse recovery transient is accurately described with a proposed behavioral model for circuit simulators. According to the physical phenomena, the drain current is de-embedded in three components: Diode, channel, and capacitance currents. The dynamics of the body diode is effectively modeled with a simple empirical equation that only requires two fitting parameters. The model approach allows assessing the impact in the reverse recovery transient curve of the different current contributors.

References

1. Elferich R, López T (2005) Accurate behavioural modelling of power MOSFETs based on device measurements and device physics simulations. In: European power electronics, EPE 2005, Sept 2005
2. Dolny GM, Sapp S, Elbanhaway A, Wheatley CF (2004) The influence of body effect and threshold voltage reduction on trench MOSFET body diode characteristics. In: IEEE international symposium on power semiconductor devices and ICs, ISPSD 2004, pp 217–220
3. López T, Elferich R, Tolle T, Koper N, Duerbaum T (2004) Third quadrant output characteristics in high density Trench MOSFETs. In: IEEE international power electronics and motion control conference, EPE-PEMC 2004, vol 2, pp 26–34
4. Mouthaan T (1999) Semiconductor devices explained using active simulation. Wiley, New York, pp 274–278
5. Lauritzen PO, Ma CL (1991) A simple diode model with reverse recovery. IEEE Trans Power Electron 6(2):188–191
6. Maxim A (1998) The analog behavioural SPICE macro modelling – a novel method of power semiconductor devices modelling. In: IEEE Transactions on PE, 1998
7. Tolle T, Duerbaum T, Elferich R, López T (2003) Quantification of switching loss contributions in synchronous rectifier applications. In: European power electronics, EPE 2003

Appendix C
Reverse Recovery Lumped Models

Lumped models for circuit simulators are widely used for approximating the distributed effects of carrier diffusion and recombination phenomena in semiconductor diodes. Over the last 50 years a great number of diode lumped models has been presented. Most of the proposals are based upon the concept of concentrated charge storage nodes, which allows for simple implementations and fast simulation times.

Among the most relevant proposals, the lumped charge node models from [1–3] are implementations of the diffusion equation employing analogous physical variables. This feature enables a direct assessment of the circuit response to changes in inherent device physics properties, such as geometry, materials, and doping levels. Furthermore, in these proposed models, the computation time can be readily improved in detriment of accuracy by reducing the number of charge nodes [2, 3].

In most circuit simulations though, the models tend to take a rather simpler form to describe the physical principles. The variables of these models, whose values are typically determined from parametric measurements [4], are usually chosen to compromise between accuracy and mathematical convenience, and thus often do not necessarily keep a direct correlation to the physical variables of the device [5].

While there are existence of many alternatives (see [6]), the most extended concentrated charge-based model, which stands about halfway between physics and circuit considerations, is perhaps the simplest in its form and implementation, i.e., the charge-control model [7]. Nonetheless, eventhough the charge-control concept can be entirely treated as an equivalent circuit tool, its prediction for transient analysis can be highly inaccurate [8].

Today's increasing demands for high performance electronic systems trigger the need of accurate semiconductor models that allow for stringent design optimizations. Particularly, the reverse recovery of diodes is one of the crucial limiting factors of switching transient performance in many power switched converters. Consequently, proposed advanced diode models that have not gained much attention in the past years may now be potential candidates as alternatives to the often-misused charge-control model.

In this section, lumped models for circuit simulators are investigated to represent the body diode reverse recovery of low voltage power trench MOSFETs in synchronous rectifier applications. Three previously presented models are compared in

terms of internal constitution, circuit implementation, prediction accuracy, and required computing power.

2D device physics simulations of a trench MOSFET cell underlie the prediction accuracy study. device physics simulators of semiconductor structures can accurately model the electrical characteristics of a device from its physical properties, which makes them suitable for the development of manufacturing processes. However, circuit analysis based on device physics simulations is cumbersome, and requires high computation power. Thus their use is rather limited. The purpose of this work is to obtain an equivalent accurate lumped model of the "virtual" device to effectively analyze its performance in the circuit application before it is manufactured [5].

First, a systematic procedure is carried out to de-embed the body diode reverse recovery current from inductive switching simulations of the 2D structure. The resulting data are then used to adjust the parameters of the lumped models by means of curve fitting. It is therefore exposed how effectively these lumped models can reproduce the response from the device physics simulations under different load currents and switching speed conditions of the application.

C.1 Device Physics Simulations of Power Trench MOSFETs

Figure C.1a shows the 2D representation of a trench MOSFET cell. Due to the symmetry, only half of the structure is simulated. Note that a third dimension, z, orthogonal to x and y, is considered in order to compute the current through

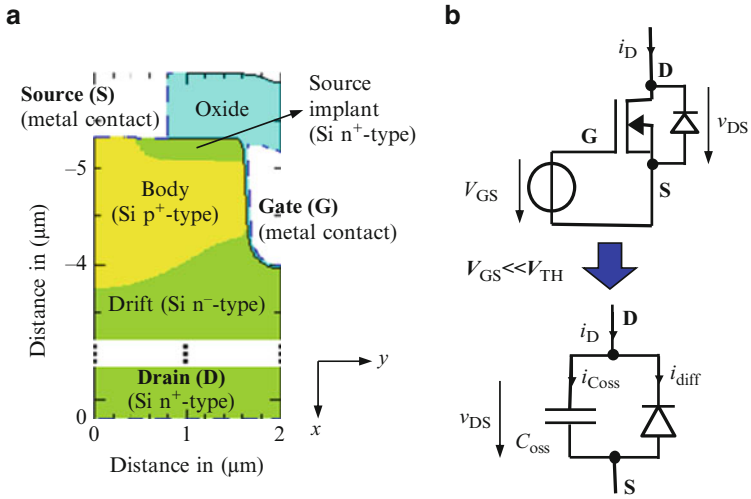

Fig. C.1 (**a**) 2D representation of a half trench MOSFET cell for low-voltage applications. (**b**) Simplified lumped model representation of a MOSFET at a strong negative gate voltage

a 1-mm^2 stripe. That is, although only two dimensions of half trench are simulated, the results shown here refer to a structure that has 4-μm length in the y direction, and extends 25 cm in the z direction.

To focus the study on the body diode behavior only, the experiments are performed at a strong negative gate voltage, thereby forcing the channel to block in both directions of the drain current, as described in [9]. Other effects of the MOSFETs are further modeled and combined in [5]. The MOSFET can therefore be represented by the body diode behavior in parallel to the output capacitance of the device, as shown in Fig. C.1b. The body diode diffusion current is obtained by,

$$i_{\mathrm{diff}}(t) = i_{\mathrm{D}}(t) - i_{C_{\mathrm{oss}}}(t) = i_{\mathrm{D}}(t) - C_{\mathrm{oss}}\frac{\mathrm{d}v_{\mathrm{DS}}(t)}{\mathrm{d}t}. \tag{C.1}$$

Capacitance C_{oss} is derived from small signal device physics simulations. Figure C.2a shows the resulting capacitance curve.

Table C.1 lists the parameter values used in the device physics simulations. Parameters W and p_{n0} are given as approximated averaged values.

Note that in low voltage diodes the length of the drift region is typically significantly shorter than the diffusion length, $W \ll L_{\mathrm{p}}$, where,

$$L_{\mathrm{p}} = \sqrt{D_{\mathrm{p}}\tau_{\mathrm{p}}}. \tag{C.2}$$

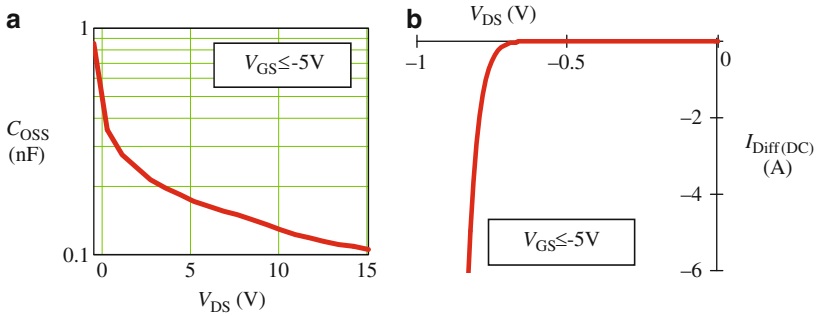

Fig. C.2 Device physics simulations of a trench MOSFET cell structure. (**a**) Output capacitance. (**b**) Static diffusion current

Table C.1 Device parameter values used in the device physics simulations

Parameter	Value
Cross-sectional area of the device, A	1 mm^2
Width of the drift region, W	3.4 μm
Temperature, T	300 K
Average equilibrium concentration of holes in the drift region, p_{n0}	10^9 cm^{-3}
Lifetime of holes in the drift region, τ_{p}	10 μs
Diffusion coefficient of holes, D_{p}	6.5 cm^2/s

Current i_{diff} is mainly caused by diffusion of holes in the drift region. In order to calculate it, the device physics simulator computes the continuity equation of excess of holes in the drift region, p'_n,

$$\frac{\partial p'_n}{\partial t} = -\frac{1}{q}\vec{\nabla}\cdot\overrightarrow{J_{\text{p}}} - \frac{p'_n}{\tau_{\text{p}}} \tag{C.3}$$

in combination with the diffusion-based transport equation, which is,

$$\overrightarrow{J_{\text{diff}}} = \overrightarrow{J_{\text{p}}} = -qD_{\text{p}}\vec{\nabla}p'_n. \tag{C.4}$$

The static characteristics of the body diode, shown in Fig. C.2b as $I_{\text{Diff(DC)}}(V_{\text{DS}})$, derive from the above two equations when (C.3) is set to equal zero. As it will be shown later, this static curve is required as input data to the lumped models.

Figure C.3 illustrates the circuit diagram for the generation of the inductive reverse recovery curves. Table C.2 lists the parameter values of the circuit. Inductance L is varied to adjust the ramp slope K_i of the current, which is expressed in units A/s. Capacitance C and resistance R are used to avoid an excessive voltage across v_{DS} that may drive the device into avalanche. The circuit simulation starts in static equilibrium with zero current through inductance L. The initial voltage V_{iC} across capacitance C depends on current I_{o} and the static characteristics of the body diode (see Fig. C.2b).

Figure C.4 shows an example of a reverse recovery transient curve derived from device physics simulator. Current i_{diff} is obtained from (C.1). Besides current I_{o} and current slope K_i, three other parameters are defined to characterize the reverse recovery curves. These are the reverse recovery charge, Q_{rr}, the reverse current peak, I_{rp}, and time t_{rp}, defined to be the time interval between the zero current crossing and I_{rp}, as indicated in Fig. C.4.

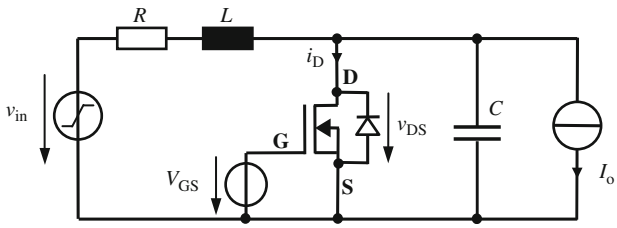

Fig. C.3 Inductive load reverse recovery circuit diagram

Table C.2 Default parameter values of circuit of Fig. C.3

R	L	C	V_{GS}	v_{in}
0.1 Ω	$\frac{10-V_{\text{iC}}}{K_i}$	1 nF	−5 V	Ideal step function from V_{iC} to 10 V

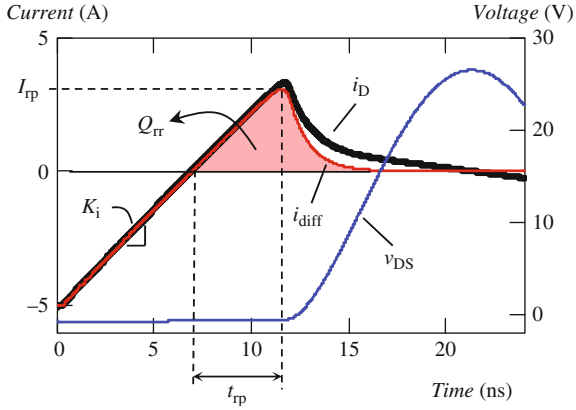

Fig. C.4 Inductive load reverse recovery waveforms corresponding to circuit diagram of Fig. C.1.3. 2D device physics simulations of the trench MOSFET cell of Fig. C.1.1(a)

C.2 Circuit Simulator Lumped Models

Three lumped models are analyzed. These are: the generalized lumped model approach based on the transmission line analogy presented in [1, 2], the model based on two charge storage nodes proposed in [4], and the empiric lumped model from [5]. The following subsections describe their internal constitution and basic circuit implementation.

C.2.1 Transmission Line Based Lumped Model

The model proposed in [1, 2] deals with a simplified 1D space problem of the diffusion equation, in the way indicated as follows,

$$p'_n = p'_n(x,t) \tag{C.5}$$

being the x direction in correspondence to the diagram of Fig. B.2a. Combining (C.3)–(C.5) yields the 1D diffusion equation of holes in the drift region,

$$D_p \frac{\partial^2 p'_n(x,t)}{\partial x^2} = \frac{\partial p'_n(x,t)}{\partial t} + \frac{p'_n(x,t)}{\tau_p}. \tag{C.6}$$

The diffusion current through the diode is calculated by,

$$i_{diff}(t) \cong i_{diff_{1D}}(t) = -qAD_p \left.\frac{dp'_n(x,t)}{dx}\right|_{x=X_p}. \tag{C.7}$$

Parameter X_p is the boundary between the depletion and quasi-neutral areas in the drift region.

The lumped models can be obtained by identifying the existing analogy between the diffusion equation in (C.6) and the electric transmission line equation (or telegrapher's equation) [3]. Figure C.5 shows the equivalent circuit of an incremental transmission line section, called basic transmission line lumped cell (TLLC).

According to the fact that two forms of energy behave identically when the basic differential equations that describe them have the same form and the initial and boundary conditions are identical, then applying the following equivalences,

$$p'_n(x,t) \Leftrightarrow v(x,t), \quad D_p \Leftrightarrow (RC)^{-1}, \quad \tau_p \Leftrightarrow \frac{C}{G}, \quad L = 0, \qquad \text{(C.8)–(C.11)}$$

where v is the voltage across the transmission line, R its resistance per unit length, C its capacitance per unit length, and G its transverse conductance per unit length.

The diffusion and recombination processes described by (C.6) can be precisely modeled with the transmission line circuit of Fig. C.6 when the number of employed TLLCs, N_c, tends to infinite and Δx tends to 0 for each individual TLLC.

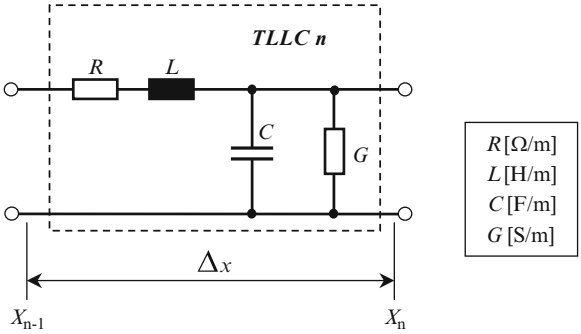

Fig. C.5 Basic transmission line lumped cell (TLLC)

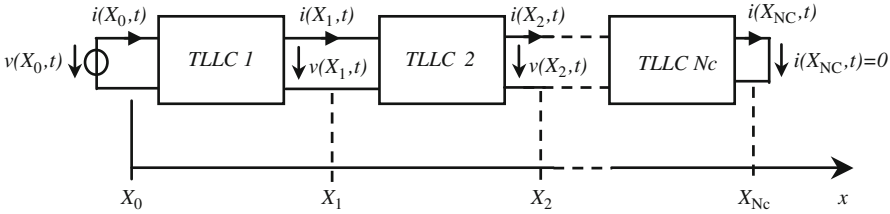

Fig. C.6 Analog circuit lumped model of diffusion of holes in the drift region of the body diode

According to the following equivalences,

$$X_{\mathrm{p}} \Leftrightarrow X_0, \quad W - X_{\mathrm{p}} \Leftrightarrow N_{\mathrm{c}}\Delta x. \tag{C.12)–(C.13}$$

It is straightforward to verify that the diode diffusion current is proportional to the current through the transmission line of Fig. C.6 at $x = X_0$, as follows,

$$\frac{i_{\mathrm{diff_TL}}(t)}{qA} \Leftrightarrow \frac{i(X_0, t)}{C}, \tag{C.14}$$

where $i_{\mathrm{diff_TL}}$ is approximately equal to (C.7) when N_{c} is sufficiently high. Note that the transmission line is terminated at $x = X_{N\mathrm{c}}$ with a short so as to emulate an idealized metal contact to the drain terminal. The boundary value at the other side of the transmission line varies instantaneously in proportion to the static characteristics [10], that is,

$$p_n'(X_0, t) = -\frac{K_{\mathrm{p}}}{qA} \cdot I_{\mathrm{Diff(DC)}}(v_{\mathrm{DS}}(t)), \tag{C.15}$$

where K_{p} is a parameter of the model to be determined. $I_{\mathrm{Diff(DC)}}$ in (C.15) corresponds to the simulated steady-state diffusion current from Fig. C.2b, which can be table based implemented in the circuit simulator. Parameter K_{p} must be adjusted to force the steady-state conditions in $i_{\mathrm{diff_TL}}$ equal to $I_{\mathrm{Diff(DC)}}$.

If expression (C.14) is multiplied by qA, then $i_{\mathrm{diff_TL}}$ is directly equivalent to $i(X_0, t)/C$. Thus, numerical operations with extreme magnitudes are mitigated.

C.2.2 Lumped Model Based on Two Lumped Storage Nodes

The proposed model from [4] implements approximately the diffusion current equation from (C.7) and a charge control continuity equation that derives from (C.6). The diffusion current from (C.7) is approximated by means of two charge storage nodes, q_{E} and q_{M}, as follows,

$$i_{\mathrm{diff}}(t) \cong i_{\mathrm{diff_L}}(t) = \frac{q_{\mathrm{E}}(t) - q_{\mathrm{M}}(t)}{T_{\mathrm{M}}}, \tag{C.16}$$

where,

$$q_{\mathrm{E}}(t) = \tau_{\mathrm{m}} \cdot I_{\mathrm{Diff(DC)}}(v_{\mathrm{DS}}(t)), \tag{C.17}$$

$$q_{\mathrm{M}}(t) = \int_0^t q_{\mathrm{E}}(t_{\mathrm{o}}) h_{\mathrm{L}}(t_{\mathrm{o}})\, \mathrm{d}t_{\mathrm{o}} + \frac{q_{\mathrm{E}}(0^-)}{1 + (T_{\mathrm{M}}/\tau_{\mathrm{m}})} \mathrm{e}^{-((1/T_{\mathrm{M}})+(1/\tau_{\mathrm{m}}))t}, \tag{C.18}$$

$$h_{\mathrm{L}}(t) = \frac{1}{T_{\mathrm{M}}} \mathrm{e}^{-((1/T_{\mathrm{M}})+(1/\tau_{\mathrm{m}}))t} \cdot u(t). \tag{C.19}$$

Note that $u(t)$ is the unit step function. The circuit implementation of the above equations results in a single TLLC, where the following equivalences apply,

$$T_{\mathrm{M}} \Leftrightarrow R, \quad \tau_{\mathrm{m}} \Leftrightarrow \frac{1}{G}, \quad L = 0. \tag{C.20)–(C.22}$$

Variable q_{E} represents the stored charge at the boundary between the depletion and quasi-neutral areas of the drift region, whereas q_{M} is the concentrated lumped charge in the quasi-neutral region. Thus, τ_{m} approximates the holes' lifetime, and T_{M} the diffusion time across the quasi-static region.

Due to its arrangement, the DC static current that the model predicts differs from $I_{\mathrm{Diff(DC)}}$. The error is proportional to the following factor,

$$I_{\mathrm{Diff(DC)}} \text{ error factor} = \left(1 + \frac{T_{\mathrm{M}}}{\tau_{\mathrm{m}}}\right)^{-1}. \tag{C.23}$$

In applications where current is impressed into the device, the above error might well be negligible in case of diodes with steep static characteristics.

C.2.3 Empirical Lumped Model

The empirical model from [5] aims at representing the reverse recovery of high current power MOSFETs. As its name indicates, the model does not derive from device physics theory. Instead, its parameters are arranged to allow for an effective curve fitting procedure to match reverse recovery transient curves from device physics simulations and/or measurements.

The diode diffusion current of the body diode is expressed as,

$$\begin{aligned} i_{\mathrm{diff}}(t) \cong i_{\mathrm{diff_E}}(t) &= \beta_{\mathrm{rr}} \cdot I_{\mathrm{Diff(DC)}}(v_{\mathrm{DS}}(t)) + \cdots \\ &+ \frac{1}{t_{\beta\mathrm{rr}}} \int \left[I_{\mathrm{Diff(DC)}}(v_{\mathrm{DS}}(t)) - i_{\mathrm{diff_E}}(t)\right] \mathrm{d}t + I_{qt=0}, \end{aligned} \tag{C.24}$$

where β_{rr} and $t_{\beta\mathrm{rr}}$ are the parameters of adjustment and $I_{qt=0}$ the initial conditions of the integral. Rearranging it follows that,

$$i_{\mathrm{diff_E}}(t) = \int_0^t r_{\mathrm{e}}(t_{\mathrm{o}}) h_{\mathrm{e}}(t - t_{\mathrm{o}})\, \mathrm{d}t_{\mathrm{o}} + I_{\mathrm{Diff(DC)}}(v_{\mathrm{DS}}(0)) \cdot \mathrm{e}^{-(t/t_{\beta\mathrm{rr}})}. \tag{C.25}$$

The convolution integral is composed by,

$$h_e(t) = e^{-(t/t_{\beta rr})} \cdot u(t), \tag{C.26}$$

$$r_e(t) = \beta_{rr} \frac{dI_{Diff(DC)}(v_{DS}(t))}{dt} + \frac{I_{Diff(DC)}(v_{DS}(t))}{t_{\beta rr}}. \tag{C.27}$$

Looking at (C.24) one identifies the following,

- For the DC diffusion current to be equal to $I_{Diff(DC)}$ the integral term plus the initial condition must equal to $(1-\beta_{rr})$ times the value of $I_{Diff(DC)}$.
- Parameter β_{rr} controls the contribution of $I_{Diff(DC)}$ to the total current. Increasing its value amplifies the current transient. Thus, β_{rr} allows adjusting the reverse current peak value.
- Parameter $t_{\beta rr}$ controls the integral factor, that is, the rate of change of total amount of charge being stored or removed during the transient current. Thus, $t_{\beta rr}$ allows adjusting the reverse recovery time, particularly, the decay curve time.

Unlike in [4], the steady-state diffusion current error is not present if the initial conditions of the integral are appropriately set.

The model can be realized in a circuit simulator by using (C.25). This requires though that the simulator allows for numerical expressions of mathematical formulations.

C.3 Models Performance

It is of general interest to investigate how accurately the models can predict the reverse recovery curves upon different circuit conditions, particularly, various output current levels and switching speeds. In the way described in Sect. C.2, device physics simulations are performed to produce inductive reverse recovery transients at current slopes from 100 to 1,000 A/μs in 1 mm^2 trench cell. The output current is varied from 0.5 to 5 A. These might well be usual ranges in applications such as point of load that employ multi-chip modules or advance discrete solutions. The values must be scaled according to the total active area of the device. For example, in a 10 mm^2 die size, the corresponding ranges are 1–10 A/ns and 5–50 A, respectively.

The device physics simulations curves are compared to those from the lumped models after calibrating their parameters. The latter is particularly simple in case of the transmission line based model, which only needs extracting parameter K_p. The rest of parameters are directly set according to the equivalences (C.8)–(C.13) and the physical parameter values from Table C.1. A single DC bias point calculation is sufficient to find the value of K_p for matching a point in the static curve of Fig. C.2b.

Table C.3 Simulated electrical conditions for the current flow line graphs

Voltage v_{DS} (V)	Voltage v_{GS} (V)	Current i_D (A)
−0.1	0	-400×10^{-12}
	1	-32×10^{-6}
−0.4	0	-30×10^{-6}
	1	−1.2
−0.8	0	−13.8
	1	−42

The other two lumped models require the derivation of their parameters by means of curve fitting of the reverse recovery transients. The square error of the diffusion current with $K_i = 505$ A/μs and $I_o = 5$ A is minimized. Table C.3 lists the extracted parameter values from the three models.

Regarding the lumped model from [4], the resulting value for τ_m is several orders of magnitude lower than the lifetime of holes τ_p, which suggests that no direct correlation exists between the two parameters. Parameter τ_m is though expected to have a closer value to τ_p for long drift devices, i.e. $L_p \gg W$, which is typical in high voltage diodes [11]. Anyway, parameter T_M cannot be deduced from the physical properties and thus curve fitting is always required.

Figures C.7 and C.8 compare reverse recovery transient curves predicted by the lumped models and device physics simulations. The lumped representations from [4, 5] virtually produce the same response and so the dashed curves refer to both models. They can predict the device physics simulations at the calibrated points with virtually no error. However, when K_i is varied and I_o is kept constant, i.e., upper graphs of Figs. C.7 and C.8, the accuracy error increases. The more K_i is deviated from the calibrated point, the higher the error gets. For the ranges given in the example, the maximum accuracy error is: 35, 30, and 16% in predicting Q_{rr}, I_{rp}, and t_{rp}, respectively. These errors occur when K_i is reduced by factor of 5 from the calibrated point. When I_o is varied and K_i is kept constant (lower graphs of Figs. C.7 and C.8), the maximum accuracy error is 32%, 28, and 27% for Q_{rr}, I_{rp} and t_{rp}, respectively. The latter worst-case numbers result from reducing I_o one order of magnitude from the calibrated point. When comparing the computation power it is observed that the device physics simulations are two orders of magnitude slower than the lumped models from [4, 5], which show similar simulation times.

The transmission line based model is inaccurate at low N_c. At high N_c though the accuracy rapidly increases, being comparable to the other two lumped models when N_c approaches 100. The recovery decay curves at high N_c are however slightly slower than those from device physics simulations, which result in an overestimation of Q_{rr}, as shown in Fig. C.8. Figure C.9 shows the dependency of the accuracy error and simulation time on N_c. The error rapidly reduces when increasing N_c up to 100. Above it the accuracy error practically does not change. Thus, the use of 100 TLLCs appears to be optimum, considering the rapid increase of required computation power at N_c above 100, as shown in Fig. C.9b. At $N_c = 100$, it already doubles the computation time of the other two lumped models, whose simulation times equal to those of a single TLLC (Table C.4).

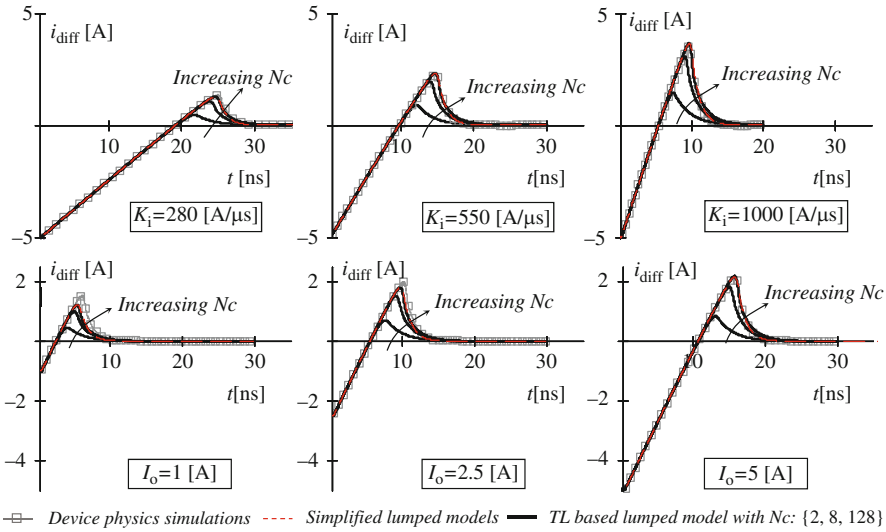

Fig. C.7 Inductive reverse recovery comparison at various current slopes and output currents

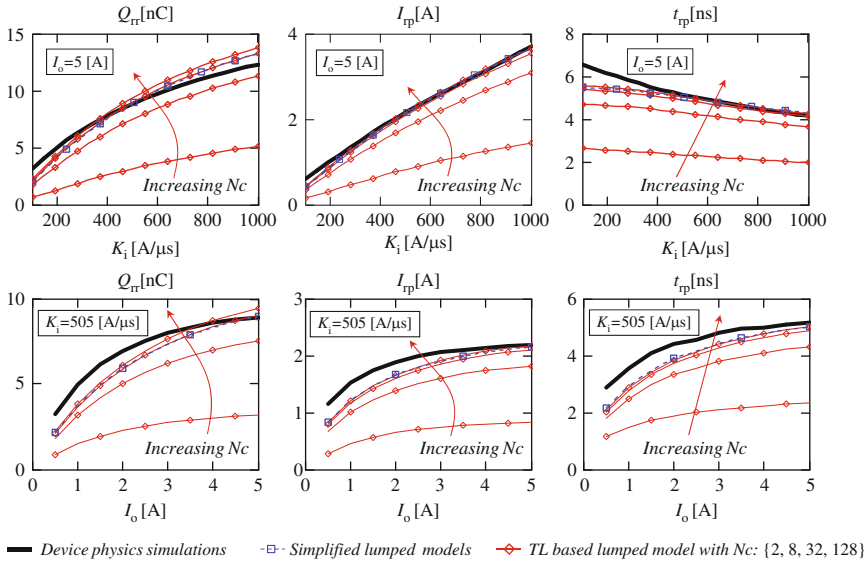

Fig. C.8 Inductive load reverse recovery parameters of various models as a function of the current slope (*upper* graphs), and as a function of the output current (*lower* graphs). From *left* to *right*: Total reverse recovery charge, Q_{rr}, maximum reverse recovery peak, time interval between zero current crossing and maximum reverse current peak, t_{rp}

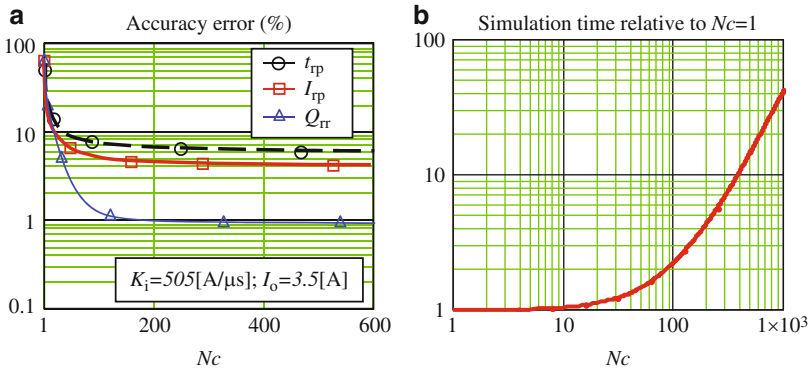

Fig. C.9 Transmission line based model performance from [1, 2] at various TLLCs. (**a**) Accuracy errors with respect to device physics simulations. (**b**) Simulation time relative to $N_c = 1$

Table C.4 Calibrated model parameters

TL model [1–3]	Single TLLC [4]	Empirical model from [5]
$K_p = 54$ μs/cm	$T_M = 1.3$ ns, $\tau_m = 6.8$ ns	$\beta_{rr} = 6.5$, $t_{\beta rr} = 1$ ns

C.4 Summary

Lumped diode models for circuit simulators are suitable for the representation of the body diode dynamics of low voltage trench MOSFETs. Here the considered lumped models require as input data the DC static characteristics of the body diode. Additionally, two parameters must be calibrated in the models from [4, 5] by means of curve fitting of a reference reverse recovery transient curve. This curve fitting involves a procedure to de-embed the diffusion current from the total drain current. device physics simulations can effectively be used to provide all the required data for the lumped models.

It is shown that the lumped models from [4, 5] have a very simple structure, are easy to implement, and furthermore predict with virtually no error the transient response of device physics simulations upon the circuit conditions of the parameters calibration. The accuracy error may though increase when these conditions are varied. Up to 35% prediction error in Q_{rr} is reached when the current ramp slope is reduced by a factor of 5 from the value used in the calibration. The parameters of these two models are not directly correlated to the physical magnitudes of the device. As example, it is shown that the parameter from [4] that is related to the lifetime of holes takes a value that is three orders of magnitude lower than the real value.

The transmission line based model from [1, 2] does not necessarily require the curve fitting of a transient curve for parameter calibration. Instead, only a very simple adjustment is needed. All but one model parameters can be directly deduced from the physical magnitudes of the device. The transmission line representation

requires of at least 100 TLLCs and twice computation time to approach the accuracy of the lumped models from [4, 5].

References

1. Linvill JG (1958) Lumped models of transistors and diodes. In: IEEE Proceedings of the IRE, vol 46, pp 1141–1152, June 1958
2. Wang PP, Branin FH Jr (1973) Multi-section network modeling of junction diodes. In: Proceedings of the 4th annual Pittsburgh conference modeling and simulation, pp 470–474
3. Chang F-Y (1996) Transient analysis of diode switching circuits including charge storage effect. In: IEEE transactions on circuits and systems, I: fundamental theory and applications, vol 43, no. 3, pp 177–190, March 1996
4. Lauritzen PO (1991) A simple diode model with reverse recovery. IEEE Trans Power Electron 6(2):188–191
5. Elferich R, López T, Koper N (2005) Accurate behavioural modelling of power MOSFETs based on device measurements and device physics simulations. In: IEEE 11th European conference on power electronics and applications, Sept 2005
6. Tan CM, Tseng K-J (1999) Using power diode models for circuit simulations – a comprehensive review. IEEE Trans Ind Electron 46(3):637–645
7. Koehler D (1967) The charge-control concept in the form of equivalent circuits, representing a link between the classic large signal diode and transistor models. Bell Syst Tech J 46:523–576, ISSN:0005-8580
8. Darling RB (1995) A full dynamic model for pn-junction diode switching transients. IEEE Trans Electron Dev 42(5):969–976
9. López T, Elferich R, Koper N (2006) Reverse recovery in high density trench MOSFETs with regard to the body effect. In: IEEE international symposium on power semiconductor devices and ICs, ISPSD 2006, pp 1–4
10. Sze SM (2002) Semiconductor devices physics and technology, 2nd edn New York, Wiley
11. López T, Alarcón E (2006) Performance comparison of pn-junction diode lumped models for circuit simulators. In: IEEE international symposium on circuit and systems, ISCAS 2006

Appendix D
Loss Quantification

As seen in Chap. 2, the proposed circuit models level 0 and 1 allow breaking down the overall power losses into the individual lossy elements of the converter circuit in the predefined switching time intervals of Sect. 2.5.1.1. This however does not provide a direct correlation between the separated quantities and the loss mechanisms defined in Sect. 2.5.1.2.

In order to quantify loss mechanisms, the dissipated power in every loss by element is systematically regarded as the sum of individual contributions from various current loops in the circuit, each of which can be mathematically formulated and related to a loss mechanism.

D.1 Conceptual Approach

The diagram of Fig. D.1 represents N different current loops formed by the path of resistor R and, paralleled to it, N additional current branches. The instantaneous power contribution to heat dissipation in R caused by the loop of the ith current branch is defined as,

$$p_i = R \cdot i_R^2 \cdot \Gamma_t^N. \tag{D.1}$$

Function Γ expresses the weight of loss contribution of a given loop as follows,

$$\Gamma_i^N = t_{r0}(i_i, i_R) \cdot \left(\sum_{m=1}^{N} t_{r0}(i_m, i_R) \right)^{-1}. \tag{D.2}$$

Function t_{r0} is defined as,

$$t_{r0}(x, y) = \begin{cases} x, & \text{sign}(x) = \text{sign}(y), \\ 0, & \text{otherwise}. \end{cases} \tag{D.3}$$

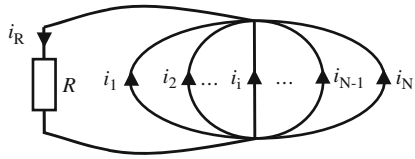

Fig. D.1 Basic current loops diagram of parallel current branches

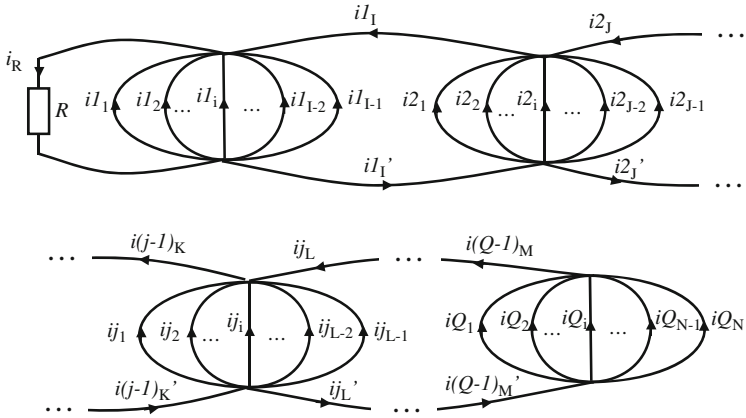

Fig. D.2 Diagram of concatenated groups of parallel current branches

According to (D.1)–(D.3), the loops of those current branches with opposite current direction to that of R have a null contribution to losses. The sum of all current loop contributions must be equal to the total power dissipation in R, that is,

$$\sum_{k=1}^{N} \Gamma_k^N = 1. \tag{D.4}$$

The above definition also applies in case the current through R is formed by a single loop of several series interconnected circuit elements. In such case, the currents in (D.2) must simply be replaced by the voltages across the series elements.

Figure D.2 depicts an extension of the diagram of Fig. D.1. Each current loop may be any closed path formed by the concatenation of two or more current branches. However, as in the simple diagram of Fig. D.1, only those loops containing the current branch of R are considered.

In the extended diagram, series branches (i.e. $i1_I$, $i2_J$, $i(j-1)_K$,...) concatenate groups of parallel branches in a cascade configuration. For instance, group 2 contains $J-1$ parallel branches and 2 series concatenating branches, i.e. $i2_J$ and $i2_{J'}$.

Note that $i2_J = i2_{J'}$. In such arrangement, the power contribution in R of the loop containing the ith parallel branch of the jth group is defined to be,

$$p_{j_i} = \begin{cases} R \cdot i_R^2 \cdot \Gamma_{j_i}^{n(j)} \cdot \prod_{k=1}^{j-1} \Gamma_{k_{n(k)}}^{n(k)}, & j > 1, \\ R \cdot i_R^2 \cdot \Gamma_{j_i}^{n(j)}, & j = 1. \end{cases} \tag{D.5}$$

Function $n(k)$ provides the number of branches of a group minus 1, e.g., $n(k) = L$ in Fig. D.2. For the particular case of the last group of the chain, $n(k)$ equals to the total number of parallel branches of the group since it does not contain series branches. The defined weight of contribution Γ of a current branch is given by,

$$\Gamma_{j_i}^{L} = t_{r0}\left(ij_i, \sum_{k=1}^{L} ij_k\right) \cdot \left(\sum_{m=1}^{L} t_{r0}(ij_m, ij_k)\right)^{-1}. \tag{D.6}$$

Note from (D.5) that the loss contribution of a current loop may be dependent on the product of multiple Γ functions. The total number of different current loops that include R is,

$$\text{Number of loops} = 1 - Q + \sum_{k=1}^{Q} n(k). \tag{D.7}$$

Thus, (D.7) provides the total number of loss contributors in R, each of which corresponds to the current loop of a particular parallel current branch.

D.2 Implementation

The formulation of the previous section is now put in practice by deriving the corresponding current loops diagram of each lossy element of the switched circuit. Figure D.3 illustrates the case of the CtrlFET channel. It is straightforward to verify

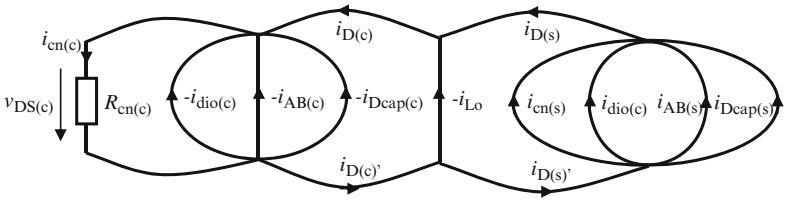

Fig. D.3 Diagram of current loops corresponding to the CtrlFET channel

that all current loops of the diagram that include $i_{\mathrm{cn(c)}}$ have a correspondence to the circuit model of Fig. D.3.

Expressions (D.5) and (D.6) are applied to assess the loss contribution of the various current loops in the form of a power quantity. Thus, for instance, the instantaneous power loss contribution of the output current loop in the CtrlFET channel is,

$$p_{\mathrm{cn(c)_{io}}} = v_{\mathrm{DS(c)}} \cdot i_{\mathrm{cn(c)}} \cdot \Gamma_{\mathrm{cn(c)_{dC}}} \cdot \Gamma_{\mathrm{cn(c)_{io}}}. \tag{D.8}$$

The product $\Gamma_{\mathrm{cn(c)_{dC}}}$ by $\Gamma_{\mathrm{cn(c)_{io}}}$ from (D.8) is the weight of the contribution of the output current loop. Their individual quantities are calculated as follows,

$$\Gamma_{\mathrm{cn(c)_{dC}}} = \frac{t_{r0}\left(i_{\mathrm{D(c)}}, i_{\mathrm{cn(c)}}\right)}{\mathrm{den}\ \Gamma_{\mathrm{cn(c)_{CtrlF}}}}, \tag{D.9}$$

$$\Gamma_{\mathrm{cn(c)_{io}}} = \frac{t_{r0}\left(i_{\mathrm{Lo}}, i_{\mathrm{D(c)}}\right)}{t_{r0}\left(i_{\mathrm{Lo}}, i_{\mathrm{D(c)}}\right) + t_{r0}\left(i_{\mathrm{D(s)}}, i_{\mathrm{D(c)}}\right)}, \tag{D.10}$$

$$\begin{aligned}\mathrm{den}\ \Gamma_{\mathrm{cn(c)_{CtrlF}}} = {} & t_{r0}\left(-i_{\mathrm{dio(c)}}, i_{\mathrm{cn(c)}}\right) + t_{r0}\left(-i_{\mathrm{AB(c)}}, i_{\mathrm{cn(c)}}\right) + \cdots \\ & + t_{r0}\left(-i_{\mathrm{Dcap(c)}}, i_{\mathrm{cn(c)}}\right) + t_{r0}\left(i_{\mathrm{D(c)}}, i_{\mathrm{cn(c)}}\right).\end{aligned} \tag{D.11}$$

Likewise, the loss contribution of the loops corresponding to the body diode and avalanche breakdown branches can be calculated from their equivalent current loops diagrams.

The current loops diagrams corresponding to the drain and source resistances of the MOSFETs differ according to the state of the switches. Namely, the current flow through these resistances may be attributed to the output load, the gate circuit path, and the paths of the corresponding off-state device. Regarding the OFF state device paths, current flow may be produced by gate bounce, capacitive charge variation, reverse recovery and avalanche breakdown. Thus, the considered current loops in the diagram may be those containing as parallel branches the output coil, the gate circuit and the internal branches of the OFF state device.

Figure D.4 shows the diagram for $R_{\mathrm{S(c)}}$ during the ON conduction time of the CtrlFET. In the example of Sect. 2.5.1, this time may correspond to any that is contained in the interval [$t1$, $t7$]. Similarly, Fig. D.5 shows the loops diagram for $R_{\mathrm{S(c)}}$ during the OFF state of the CtrlFET.

The deduction of the loss contribution quantities corresponding to the six current loops of Figs. D.4 and D.5 is immediate employing (D.5) and (D.6). Likewise, the calculations of the loss contributions in resistances $R_{\mathrm{D(c)}}$, $R_{\mathrm{D(s)}}$, $R_{\mathrm{S(s)}}$ result from similar current loop diagrams.

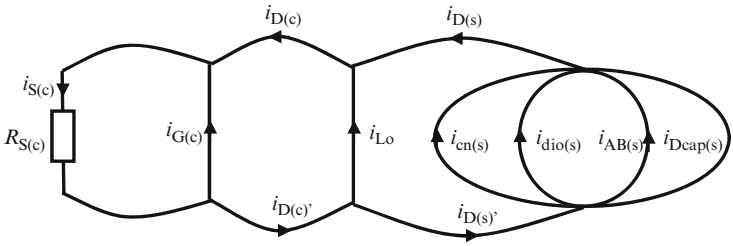

Fig. D.4 Diagram of current loops corresponding to the CtrlFET source resistance during the ON state of the device

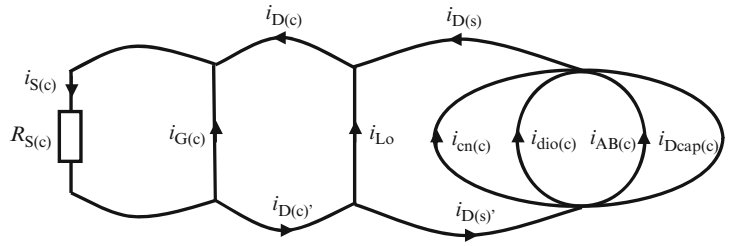

Fig. D.5 Diagram of current loops corresponding to the CtrlFET source resistance during the OFF state of the device

D.3 Loss Mechanisms Formulation

This section formulates the relation between the voltage and current contributions to power losses and the different loss mechanisms defined in Chap. 2.

D.3.1 Load Current Hard-Switching

According to its definition, snubbed hard-switching is related to the loss contribution of the output current loop and the CtrlFET channel voltage without the contribution of the half-bridge inductance voltage. This can be expressed as follows,

$$p_{\mathrm{SHS}} = v_{\mathrm{DS(c)}} \cdot [\Gamma_{\mathrm{cn(c)}V_{\mathrm{in}}} + \Gamma_{\mathrm{cn(c)}v_{\mathrm{DS(s)}}}] \cdot i_{\mathrm{cn(c)}} \cdot \Gamma_{\mathrm{cn(c)dC}} \cdot \Gamma_{\mathrm{cn(c)_{io}}}. \tag{D.12}$$

Functions $\Gamma_{\mathrm{cn(c)}V_{\mathrm{in}}}$ and $\Gamma_{\mathrm{cn(c)}_{v_{\mathrm{DS(s)}}}}$ are the weights of loss contributions of voltages V_{in} and $v_{\mathrm{DS(s)}}$. These quantities are obtained by replacing currents for voltages in (D.12) according to the following expression,

$$v_{\mathrm{DS(c)}} = V_{\mathrm{in}} - V_{\mathrm{L}} - v_{\mathrm{DS(s)}}. \tag{D.13}$$

Voltage V_L is the voltage induced across the half-bridge inductances. Note from (D.13) that the voltages across R_S and R_D from both MOSFETs are, for this case, neglected.

D.3.2 Half-Bridge Charging

Half-bridge charging is related to the loss contributions of the MOSFET output capacitive currents, and the over voltage across the CtrlFET channel caused by the half-bridge inductances during hard-switching. The latter is calculated as follows,

$$p_{\mathrm{HBC(L)}} = v_{\mathrm{DS(c)}} \cdot \Gamma_{\mathrm{cn(c)}V_{\mathrm{L}}} \cdot i_{\mathrm{cn(c)}} \cdot \Gamma_{\mathrm{cn(c)dC}} \cdot \Gamma_{\mathrm{cn(c)_{io}}}. \tag{D.14}$$

Function $\Gamma_{\mathrm{cn(c)}_{V_{\mathrm{L}}}}$ is the weight of loss contribution of the half-bridge inductances. Like $\Gamma_{\mathrm{cn(c)}_{V_{\mathrm{in}}}}$ and $\Gamma_{\mathrm{cn(c)}_{v_{\mathrm{DS(s)}}}}$ in (D.12), function $\Gamma_{\mathrm{cn(c)}_{V_{\mathrm{L}}}}$ results from (D.2) and (D.13).

The output capacitance current contributions to heat dissipation are obtained from (D.5) to (D.6) for each lossy element of the half-bridge, i.e., from their corresponding current loops diagrams. For instance, the loss contribution of the SyncFET output capacitance current loop in the CtrlFET channel is,

$$p_{\mathrm{cn(c)_{coS}}} = v_{\mathrm{DS(c)}} \cdot i_{\mathrm{cn(c)}} \cdot \Gamma_{\mathrm{cn(c)_{dC}}} \cdot \Gamma_{\mathrm{cn(c)_{dS}}} \cdot \Gamma_{\mathrm{cn(c)_{coS}}}. \tag{D.15}$$

The product of $\Gamma_{\mathrm{cn(c)_{dC}}}$, $\Gamma_{\mathrm{cn(c)_{dS}}}$ and $\Gamma_{\mathrm{cn(c)_{coS}}}$ is the weight of loss contribution of the SyncFET output capacitance current loop corresponding to the diagram of Fig. D.3.

D.3.3 Gate Charging

Gate charging is associated to the power loss in the gate drive circuit. It includes the total power dissipation in the drivers and gate resistances, and also part of the dissipation in the source resistances. The latter requires discrimination of the loss contributions from the gate and drain currents. Thus, the following expression is applied for the case of the CtrlFET,

$$p_{\mathrm{Rs(c)_{igC}}} = R_{\mathrm{S(c)}} \cdot i^2_{\mathrm{S(c)}} \cdot \Gamma_{\mathrm{Rs(c)_{igC}}}, \tag{D.16}$$

where $i_{\mathrm{S(c)}}$ is the source current and $\Gamma_{\mathrm{Rs(c)_{igC}}}$ the weight of loss contribution of the gate current. Similarly, for the case of the SyncFET,

$$p_{\mathrm{Rs(s)_{igS}}} = R_{\mathrm{S(s)}} \cdot i^2_{\mathrm{S(s)}} \cdot \Gamma_{\mathrm{Rs(s)_{igS}}}. \tag{D.17}$$

D.3.4 Reverse Recovery

Reverse recovery is related to the loss occurring in the half-bridge path during the reverse recovery time intervals. Outside this interval, the reverse recovery tail generates further loss in the half-bridge. For instance, the loss in the CtrlFET channel is calculated as follows,

$$p_{\mathrm{cn(c)_{dioS}}} = v_{\mathrm{DS(c)}} \cdot i_{\mathrm{cn(c)}} \cdot \Gamma_{\mathrm{cn(c)_{dC}}} \cdot \Gamma_{\mathrm{cn(c)_{dS}}} \cdot \Gamma_{\mathrm{cn(c)_{dioS}}}. \tag{D.18}$$

The product of $\Gamma_{\mathrm{cn(c)_{dC}}}$, $\Gamma_{\mathrm{cn(c)_{dS}}}$, and $\Gamma_{\mathrm{cn(c)_{dioS}}}$ is the weight of contribution of the SyncFET body diode current loop corresponding to the diagram of Fig. D.3. The loss contribution in the other lossy elements of the half-bridge can be likewise calculated.

D.3.5 Gate Bouncing

Gate bounce related loss is derived from the current contribution of the MOSFETs channel that is spuriously turned on. For instance, the loss contribution of the SyncFET channel loop in $R_{\mathrm{S(c)}}$ due to gate bounce is,

$$p_{\mathrm{Rs(c)_{cnS}}} = R_{\mathrm{S(c)}} \cdot i^2_{\mathrm{S(c)}} \cdot \Gamma_{\mathrm{Rs(c)_{dC}}} \cdot \Gamma_{\mathrm{Rs(c)_{dS}}} \cdot \Gamma_{\mathrm{Rs(c)_{cnS}}}. \tag{D.19}$$

The product of $\Gamma_{\mathrm{Rs(c)_{dC}}}$, $\Gamma_{\mathrm{Rs(c)_{dS}}}$ and $\Gamma_{\mathrm{Rs(c)_{cnS}}}$ is the weight of contribution of the SyncFET channel loop according to the diagram of Fig. D.4. The contributions of this loss mechanism in the other half-bridge lossy elements are similarly calculated.

D.3.6 Avalanche Breakdown

Most of the avalanche breakdown related loss occurs in the avalanching device. It is readily calculated as,

$$p_{\mathrm{AB}} = v_{\mathrm{DS}} \cdot i_{\mathrm{AB}}. \tag{D.20}$$

The avalanche current i_{AB} may further generate heat dissipation in the half-bridge. For instance, the instantaneous power loss in $R_{\mathrm{S(c)}}$ due to CtrlFET avalanche is quantified as,

$$p_{\mathrm{Rs(c)_{abC}}} = R_{\mathrm{S(c)}} \cdot i^2_{\mathrm{S(c)}} \cdot \Gamma_{\mathrm{Rs(c)_{dC}}} \cdot \Gamma_{\mathrm{Rs(c)_{dS}}} \cdot \Gamma_{\mathrm{Rs(c)_{abC}}}. \tag{D.21}$$

The product of $\Gamma_{Rs(c)_{dC}}$, $\Gamma_{Rs(c)_{dS}}$ and $\Gamma_{Rs(c)_{abC}}$ is the weight of contribution of the CtrlFET avalanche current loop corresponding to the diagram of Fig. D.5.

D.3.7 Output Current ON Conduction

It accounts for the loss contribution of the output current loop in the MOSFETs throughout the ohmic and dead time intervals. Expressions (D.8)–(D.11) provide the instantaneous loss contribution of i_{Lo} in the CtrlFET channel. The loss contributions from the other half-bridge lossy elements result from similar calculations.

Appendix E
Magnetic Losses

This section presents illustrative calculations on magnetic losses and parasitic impedances in a PCB track section, a power MOSFET package and an output filter coil for high switching frequency VR converters. Magnetic fields created by time dependent excitation currents are numerically solved by means of an FEM software [1, 2]. Eddy current losses are determined in the time domain by applying typical excitation waveforms of the converter. Alternatively, harmonic calculations leading to estimations on ESR will be used to analytically approximate transient Eddy current losses. For simple cases, the ESR will be analytically expressed as a function of physical parameters such as the skin depth.

Simulations in the frequency domain will also be applied to estimate the ESL of a multilayer PCB track section and the leadframe of the power LFPak. The latter is modeled in 3D in combination with a multilayer PCB layout from which the source inductance will be estimated and compared to experimental results.

Simulations of the power coil include the nonlinear behavior of the ferrite material, in particular, the characteristics of the B–H curves, for which the hysteresis model from Jiles–Atherton is implemented in the device physics simulator. Besides Eddy current and hysteresis losses, excess loss will be derived from specific power loss curves of manufacturer data in combination with the field calculations.

E.1 Quasi-Static Formulation

The quasi-static formulation of time varying electromagnetic fields is suitable for the analysis of structures with a size much smaller than the characteristic wavelength. The physical assumption of this situation is that the current and charges generating the electromagnetic fields vary so slowly in time that are practically the same everywhere within the domain structure at every instant as if they had been generated by stationary sources.

This approximation implies that the equation of continuity can be written as,

$$\vec{\nabla} \cdot \vec{J} = 0. \tag{E.1}$$

Also, the electric displacement can be disregarded in the Maxwell-Ampère's law, thus yielding,

$$\vec{\nabla} \times \vec{H} = \vec{J}. \tag{E.2}$$

Vector $\vec{J}$ is the current density, which may be formed by an external supply and the time varying magnetic field, i.e.,

$$\vec{J} = \sigma \vec{E} = \sigma \left(\overrightarrow{J_{\mathrm{e}}} - \frac{\partial \vec{A}}{\partial t} \right), \tag{E.3}$$

where parameter σ is the material's conductivity, current vector $\overrightarrow{J_{\mathrm{e}}}$ the current density created by an external source and $\vec{A}$ the magnetic vector potential, which is related to the magnetic field $\vec{B}$ through the curl operator. Furthermore, from Faraday's law, it follows that,

$$\vec{\nabla} \times \vec{E} = -\frac{\partial \vec{B}}{\partial t}. \tag{E.4}$$

Combining (E.1)–(E.4) yields the following partial differential equation,

$$\sigma \frac{\partial \vec{A}}{\partial t} + \vec{\nabla} \times (\mu^{-1} \vec{\nabla} \times \vec{A}) = \overrightarrow{J_{\mathrm{e}}}. \tag{E.5}$$

Parameter μ is the material's permeability that relates $\vec{B}$ and $\vec{H}$. Equation (E.5) is solved numerically by the FE method in order to estimate the effects of Eddy currents in parts of the converter circuit.

E.2 PCB Layout

It is frequently advantageous to base the PCB layout design on multilayer structures where the inner layer is used as return ground path in such a way that the loop inductance is minimized. Figure E.1 depicts a cross-sectional view of such layout arrangement, where the currents in the top and bottom traces are equal in magnitude but flow in opposite directions. For simplicity, only the section to the right of the line of symmetry is represented and simulated.

Harmonic device physics simulations of the PCB cross section allow calculating the associated ESR and ESL contribution as a function of frequency. The results of Fig. E.2 show that the skin effect becomes significant at frequencies around 1 MHz and above, reaching 10 times higher ESR at 25 MHz with respect to DC operation.

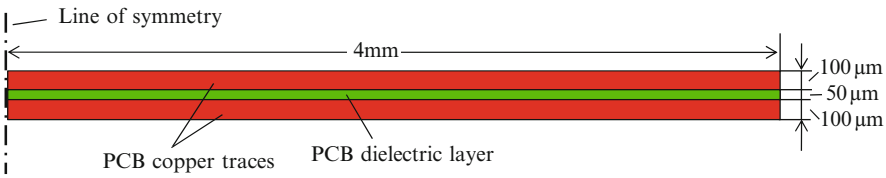

Fig. E.1 Simulated 2D cross-sectional geometry corresponding to a double-layer PCB

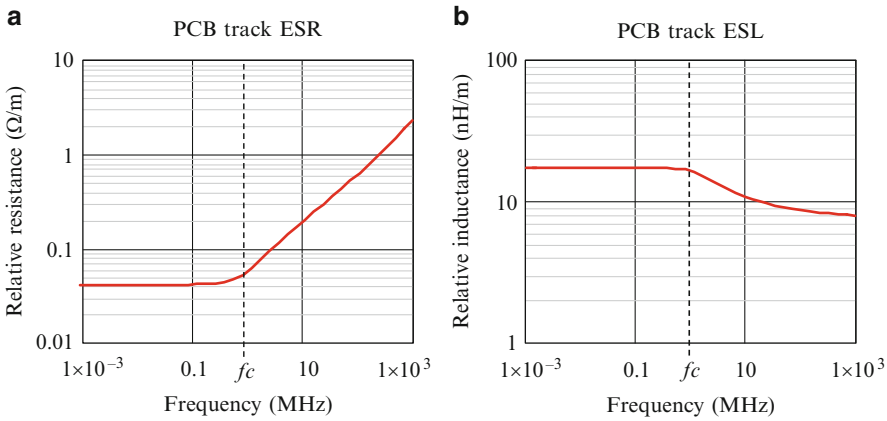

Fig. E.2 Harmonic simulations of the double-layer PCB layout of Fig. E.1

The influence of the dielectric thickness on the ESL is reflected in the curves of Fig. E.3, showing that the loop area increase boosts the parasitic ESL in a nonlinear fashion. This contrasts with the ESR, which is fairly independent of the separation distance between the two parallel conductive layers.

A relevant physical quantity related to magnetic losses is the *skin depth*, which defines the penetration distance of the magnetic field into a conductive material. The skin depth is defined as,

$$\delta(f) = \frac{1}{\sqrt{\pi \cdot \mu_0}} \sqrt{\frac{\rho}{\mu_r \cdot f}} \approx 503 \sqrt{\frac{\rho}{\mu_r \cdot f}}. \tag{E.6}$$

Figure E.4 shows an example of the skin depth dependence on the frequency in the case of copper material.

The AC resistance estimated from harmonic calculations can be analytically calculated for simple geometries like that shown in Fig. E.1. Provided that the current density mainly crowds in the conductor sides in contact to the dielectric layer, the ESR may be approximately expressed as follows,

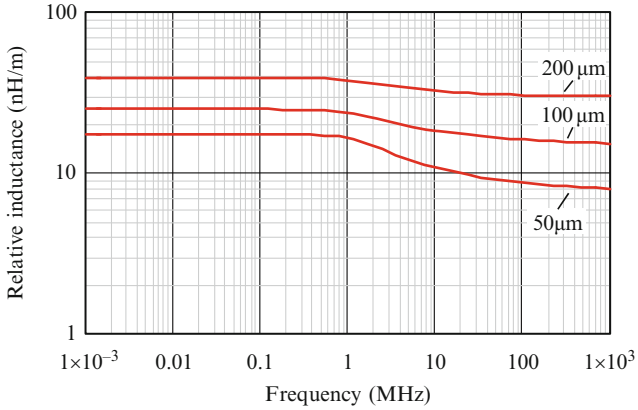

Fig. E.3 Harmonic simulations of the double-layer PCB layout of Fig. E.1. Inductance extraction for various gap thickness

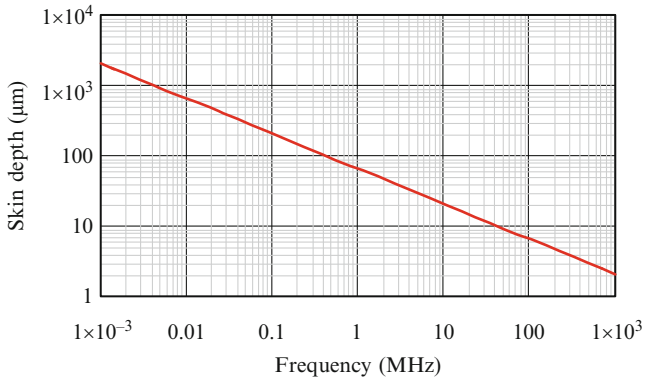

Fig. E.4 Skin depth in copper material at 25°C. ρ = 16.67 nm, $\mu_r = 1$

$$R_{\text{pcb}}(f) = 2\rho \begin{bmatrix} 2 \cdot \left(H_x - 2 \cdot \min\left(\frac{H_x}{2}, \delta(f)\right)\right) \cdot \min\left(\frac{L_x}{2}, \delta(f)\right) + \cdots \\ 2 \cdot \left(L_x - 2 \cdot \min\left(\frac{L_x}{2}, \delta(f)\right)\right) \cdot \min\left(\frac{H_x}{2}, \delta(f)\right) + \cdots \\ 4 \cdot \min\left(\frac{H_x}{2}, \delta(f)\right) \cdot \min\left(\frac{L_x}{2}, \delta(f)\right) \end{bmatrix}^{-1} . \quad \text{(E.7)}$$

Parameters H_x and L_x are the thickness and width of the conductive layers, respectively (e.g. 100 µm and 8 mm in the example of Fig. E.1). Comparing device

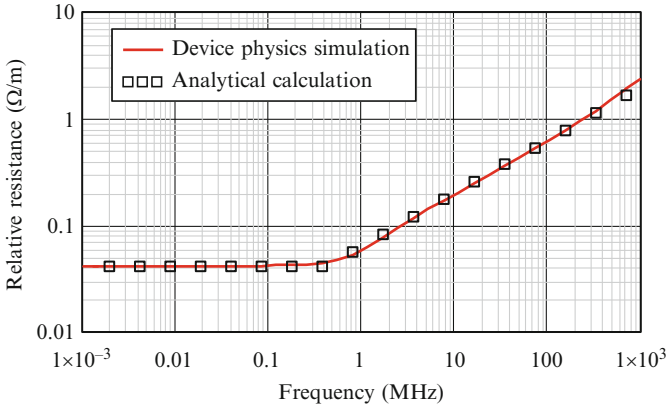

Fig. E.5 AC resistance of the double layer PCB track section of Fig. E.1. Comparison between device physics simulations and analytical calculations, i.e., (E.7) with $H_x = 100$ μm and $L_x = 8$ mm

physics simulations with (E.7) as in Fig. E.5 shows that the approximations adopted are adequate for this particular case.

In the application of interest, however, PCB losses may result from trapezoidal current waveforms rather than sinusoidal excitations. The following establishes a relation between the above calculated AC resistance and the power losses associated to ramp current waveforms.

The transient skin effect simulations of Figs. E.6–E.8 show current crowding plots resulting from a current ramp excitation of 10 A/μs. Regardless of the magnitude of the slope, however, the current density distribution varies as a function of time from a boundary conduction at $t = 0$, to a quasi uniform distribution across the cross-sectional area of the copper layers in steady-state, i.e., as $t \rightarrow \infty$.

The transient time between the two states strongly depends on the geometry and is proportional to a time constant defined by the cut-off frequency in the harmonic domain (i.e., f_c in Fig. E.2). Steady-state operation may thus be considered for $t > 5\tau_c$, where,

$$\tau_c = \frac{1}{2 \cdot \pi \cdot f_c}. \tag{E.8}$$

The same expression can be used to relate the energy loss at any time instant to its corresponding resistance in the frequency domain as follows,

$$w_{rx}(t_x) = R_x(t_x) \int_0^{t_x} i^2 \, \mathrm{d}t \cong R_{\mathrm{pcb}} \left(\frac{1}{2 \cdot \pi \cdot t_x} \right) \int_0^{t_x} i^2 \, \mathrm{d}t, \tag{E.9}$$

where w_{rx} represents the energy loss per unit length.

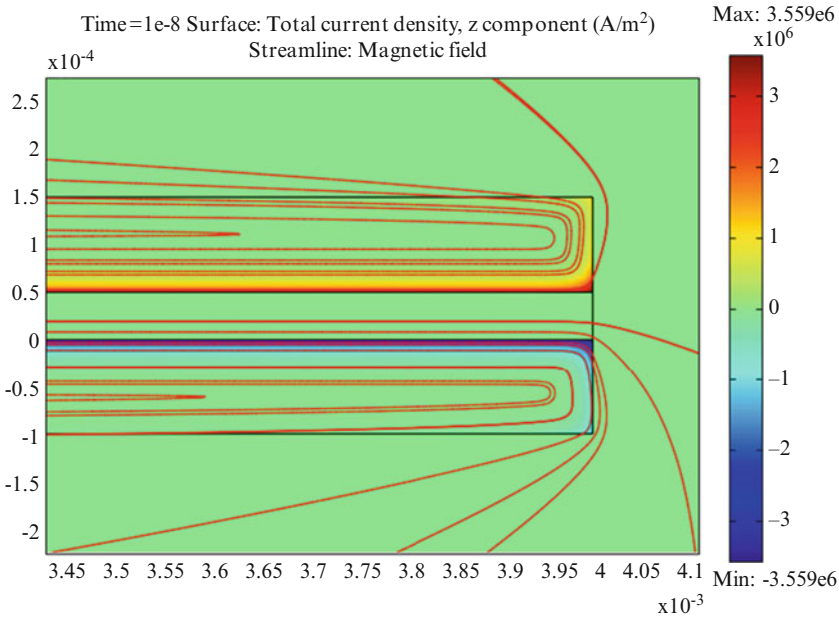

Fig. E.6 2D transient skin effect simulation of the double-layer PCB track section of Fig. E.1. Cross-sectional view of the right edge. Ramp excitation of 10 A/μs starting with zero initial conditions. Total current density distribution and magnetic field lines at $t = 10$ ns

Similarly, the equivalent ESL may be calculated from the stored magnetic energy at any given time,

$$L_x(t_x) = \frac{2 \cdot w_{mx}(t_x)}{\int_0^{t_x} i^2 \, \mathrm{d}t}. \tag{E.10}$$

Figure E.9 depicts the close correlation between the estimated ESR and ESL in both frequency and time domains.

Expression (E.9) can be applied to approximate the PCB power loss corresponding to a trapezoidal current waveform as shown in Fig. E.10a. The approximation consists of dividing the waveform into three sections defined by the ramp slopes and computing (E.9) in each of the resulting intervals. This is, for the case example of Fig. E.10, as follows,

$$P_\mathrm{T} \cong \frac{1}{T_\mathrm{s}} \left[R_x(10\,\mathrm{ns}) \cdot \left(\int_0^{10\,\mathrm{ns}} i^2(t) \cdot \mathrm{d}t + \int_{50\,\mathrm{ns}}^{60\,\mathrm{ns}} i^2(t) \cdot \mathrm{d}t \right) + R_x(40\,\mathrm{ns}) \int_{10\,\mathrm{ns}}^{50\,\mathrm{ns}} i^2(t) \cdot \mathrm{d}t \right]$$
$$= 3.3\,\mathrm{W/m}. \tag{E.11}$$

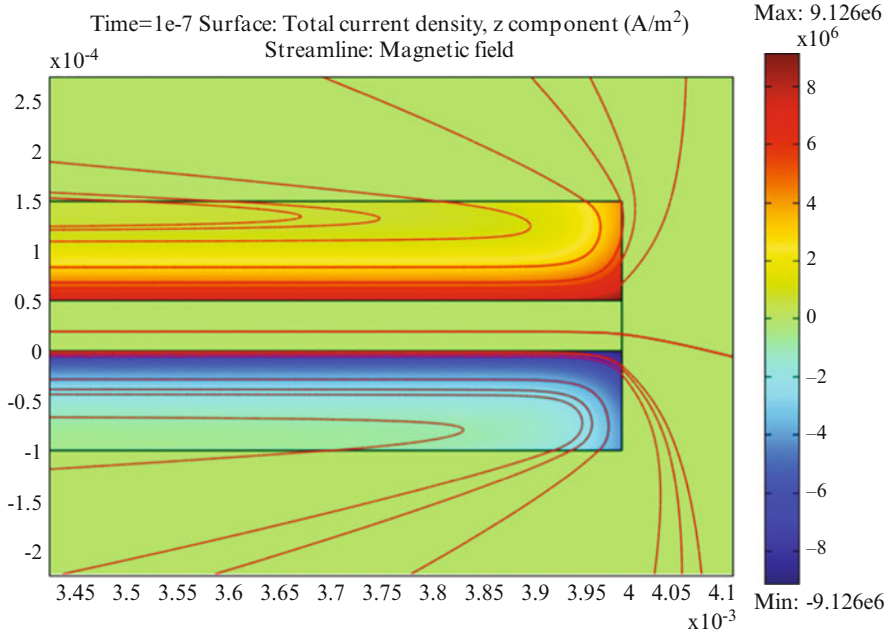

Fig. E.7 2D transient skin effect simulation of the double-layer PCB track section of Fig. E.1. Cross-sectional view of the right edge. Ramp excitation of 10 A/μs starting with zero initial conditions. Total current density distribution and magnetic field lines at $t = 100$ ns

This result matches the average power loss estimated from calculations, as shown in the instantaneous power loss plot of Fig. E.10b.

The trapezoidal signal of Fig. E.10a resembles the typical current waveform through the CtrlFET, where the ON time is generally much shorter than the switching period. While adequate for short ON times, expression (E.11) becomes inaccurate for calculating the resistive losses of the SyncFET path since the ON time of the switch is closer to the switching period. In this case the following expression appears to be more accurate,

$$w_{rs} = [R_x(0) \cdot I_{\mathrm{RMS}}^2 + R_x(T_{\mathrm{S}}) \cdot (I_{\mathrm{RMS}} - |I_{\mathrm{AVG}}|)^2] \cdot T_{\mathrm{s}}^{-1}. \tag{E.12}$$

Currents I_{RMS} and I_{AVG} in (E.12) are the RMS and average quantities of the impressed waveform, respectively. The second term accounts for the AC component and vanishes as the duty cycle approaches unity.

Figure E.11 shows transient skin effect simulations of the PCB track section of Fig. E.1 with an impressed current that resembles that of the SyncFET path. Applying (E.12) with the use of Fig. E.9 yields an estimated track section loss of 6.5 W/m, which is close to the average value of the instantaneous power curve of Fig. E.11b.

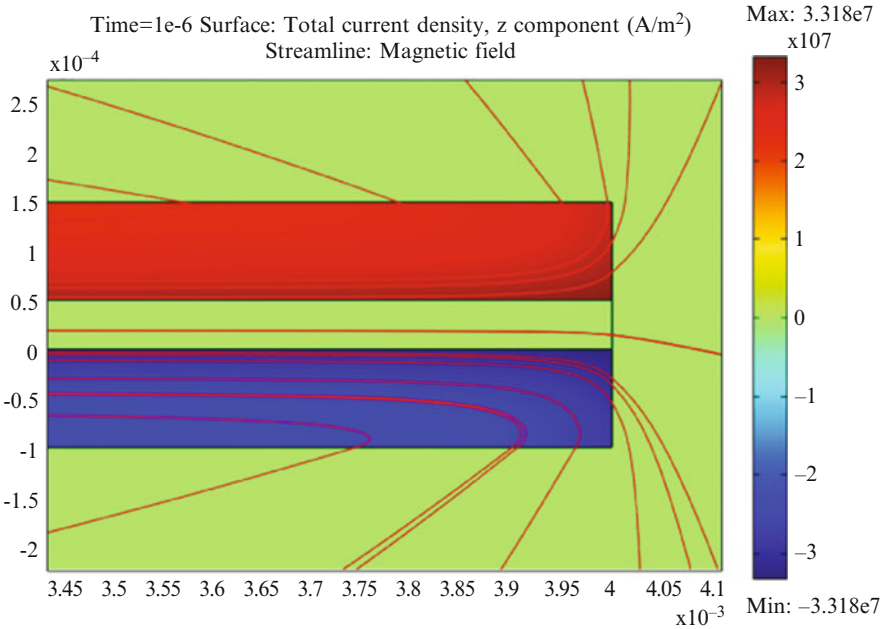

Fig. E.8 2D transient skin effect simulation of the double-layer PCB track section of Fig. E.1. Cross-sectional view of the right edge. Ramp excitation of 10 A/μs starting with zero initial conditions. Total current density distribution and magnetic field lines at $t = 1{,}000$ ns

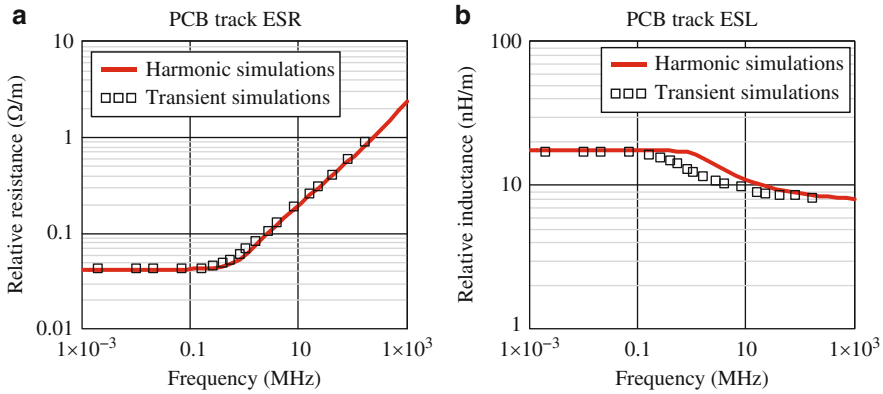

Fig. E.9 Relative effective ESR and ESL of the double-layer PCB track section of Fig. E.1. Comparison between harmonic and transient simulations

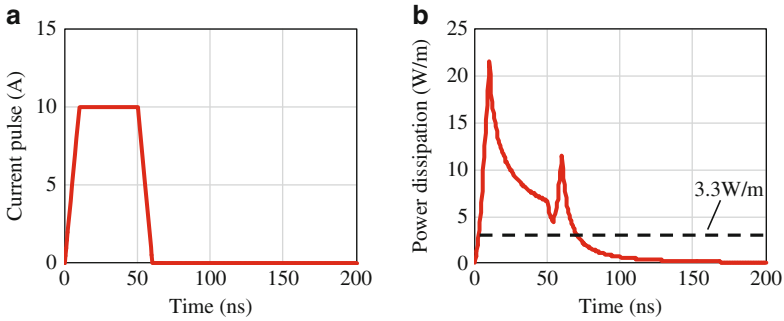

Fig. E.10 2D transient skin effect simulation of the double-layer PCB track section of Fig. E.1. (**a**) Excitation current waveform of CtrlFET drain current path. (**b**) Instantaneous and average power dissipation

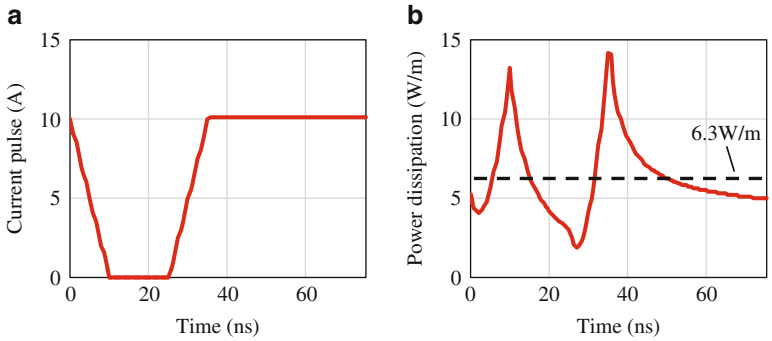

Fig. E.11 2D transient skin effect simulation of the double-layer PCB track section of Fig. E.1. (**a**) Excitation current waveform of SyncFET drain current path. (**b**) Instantaneous and average power dissipation

For low and moderate ripple currents, empirical equation (E.12) may also be adequately applied to approximate the resistive losses of the PCB track section corresponding to the output filter inductor path.

E.3 Power MOSFET Package: LFPak

This section presents simulation results on the LFPak impedance, in particular, the leadframe of the source contact. This electrode contributes predominantly to the overall package resistance as well as the source inductance. The goal is to estimate these two parameters in a wide frequency range. In order to emulate operating

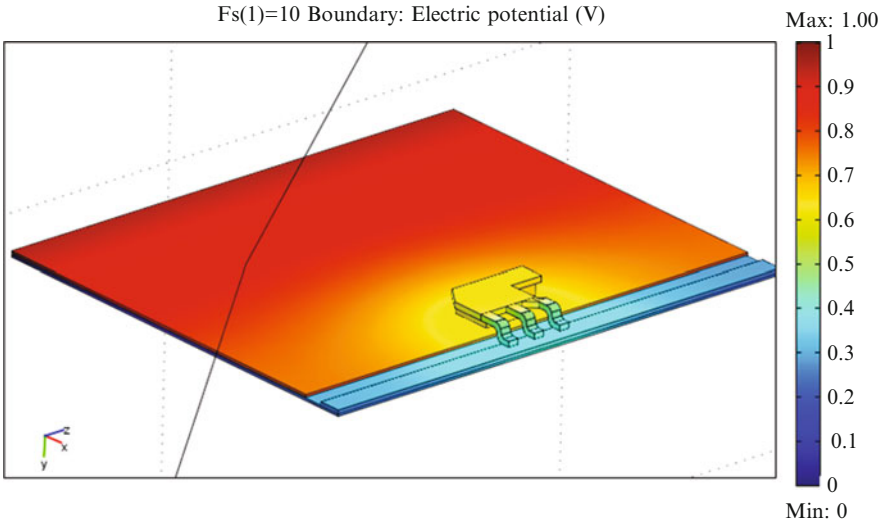

Fig. E.12 Simulated LFpak leadframe mounted on a double layer PCB. View of the voltage distribution in DC operation

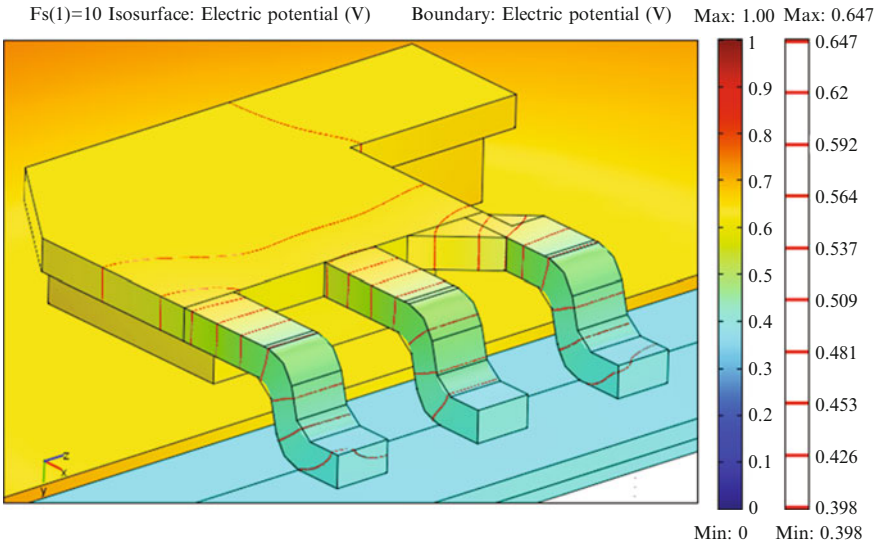

Fig. E.13 Zoom in view of the LFpak leadframe corresponding to the simulation of Fig. E.12

conditions similar to the application at hand, the simulations include both package leadframe and PCB board with a ground layer that confines the magnetic field and thus minimizes the loop inductance.

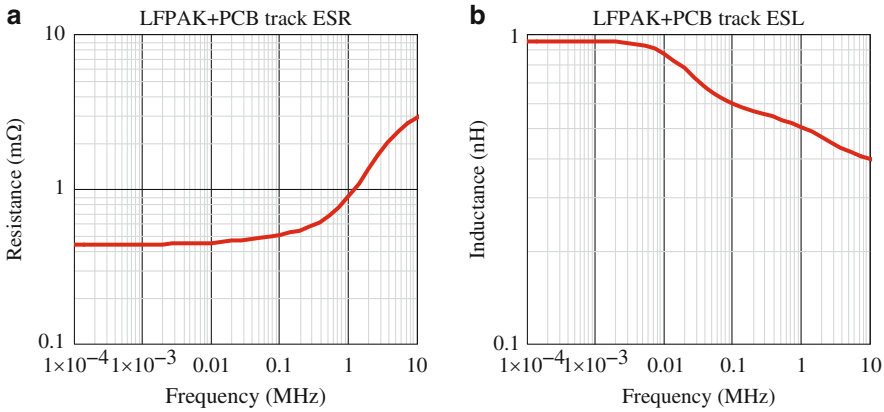

Fig. E.14 3D harmonic simulations of the LFpak leadframe impedance mounted on a double layer PCB (see Fig. E.12)

Figures E.12 and E.13 show a 3D view of the simulated leadframe plus PCB board arrangement comprising two metal layers (top and bottom) separated by a 50 μm dielectric layer. The excitation signal is impressed across the conductive layers in the y–z plane at $x = X_o$, X_o being at the PCB edge furthest away from the leadframe.

The isolines of Fig. E.13 describe the voltage distribution across the leadframe, which corresponds to DC operation. The total voltage across the leadframe divided by the total current yields a source resistance of ~110 μΩ. This is 25% of the total estimated resistance, as it can be derived from Fig. E.14a.

According to the simulations of Fig. E.14, the ESL at 1 MHz is around 500 pH, whereas the ESR increases to 0.9 mΩ from the 0.42 mΩ of DC operation. From these total 0.9 mΩ AC resistance, approximately 0.4 mΩ belong to the leadframe, which suffers a dramatic resistance increase due to Eddy currents. As to the ESL, the PCB tracks contribute with ~150 pH according to 2D simulations like shown in Sect. E.2. This leaves a ~350 pH of source inductance in the proposed geometrical arrangement.

The ESR frequency dependence is a consequence of Eddy currents in the conductors that force the current flow to confine at the conductor boundaries as the frequency increases. This is illustrated in Figs. E.15–E.17 at various harmonic frequencies. The plots show that Eddy currents are low at 10 kHz and below, whereas in the MHz range, strong current crowding is manifested in the corner leads on the leadframe as shown in Fig. E.17.

E.4 Power Coil

The purpose of this section is to illustrate the performance of a VR power inductor for high-switching frequency operation by means of device physics simulations and the theory of magnetism in ferromagnetic materials. The results provide

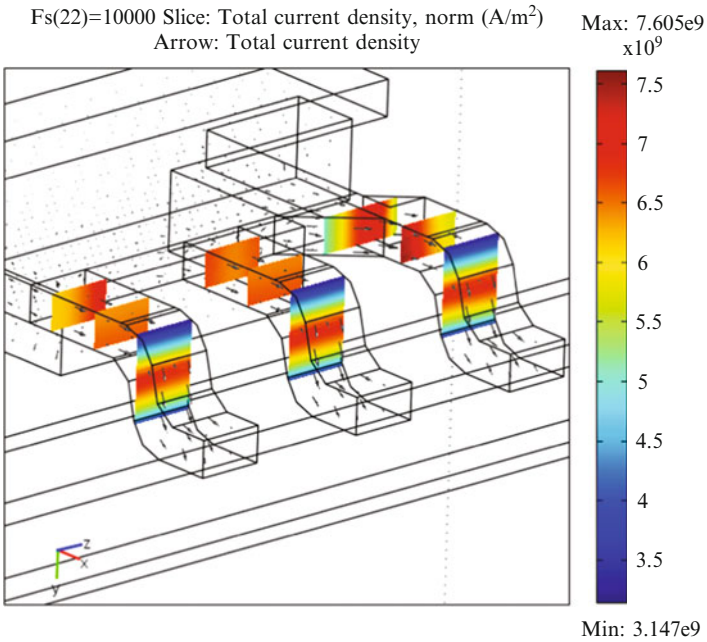

Fig. E.15 3D harmonic simulation of the LFpak leadframe mounted on a double layer PCB as shown in Fig. E.14. Current distribution through the source leads at 10 kHz

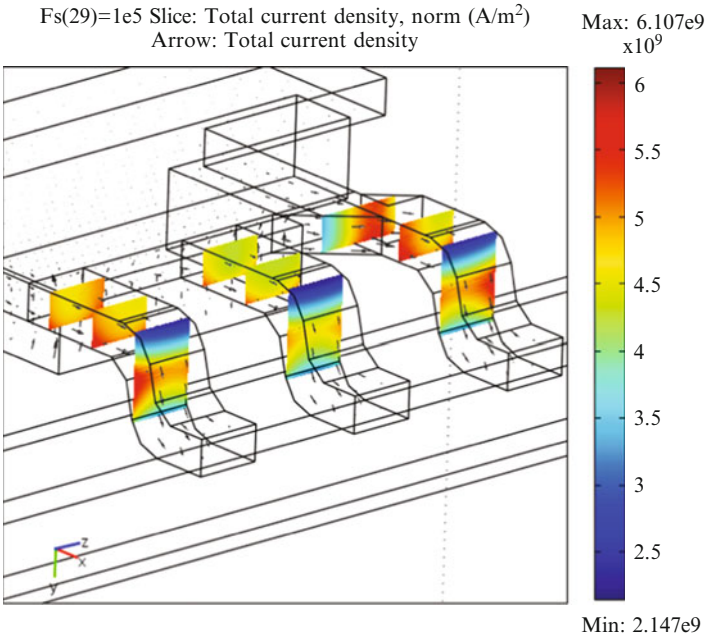

Fig. E.16 3D harmonic simulation of the LFpak leadframe mounted on a double layer PCB as shown in Fig. E.14. Current distribution through the source leads at 100 kHz

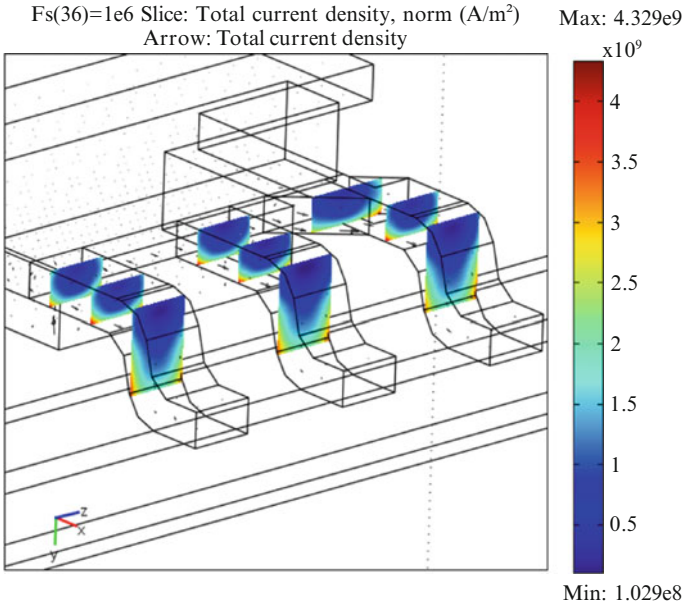

Fig. E.17 3D harmonic simulation of the LFpak leadframe mounted on a double layer PCB as shown in Fig. E.14. Current distribution through the source leads at 1 MHz

estimations on inductor losses in a wide range of operating conditions in the VR circuit as described in Chaps. 5 and 6. Furthermore, insights on the magnetic field distribution and loss breakdown allow identifying potential improvement options in the coil design.

The magnetic loss calculations presented herein are founded upon the assumption that the overall coil losses can be decomposed into the sum of three contributions, namely the *classical Eddy current loss*, *hysteresis loss*, and *excess loss*. While the first contributor is present in all materials and governed according to the classical theory of electromagnetism, the other two portions particularly manifest in ferromagnetic materials due to the existence of multiple magnetic domains that may divide the medium into regions with different magnetic moment alignments called magnetic domains. The reason of magnetic domains within the crystal structure is that their formation reduces the magnetic free energy. The notion of magnetic domains was initially introduced by Weiss in 1906 as a hypothesis, and later in 1949, Williams, Borzot, and Shockley demonstrated experimentally their existence. Providing mathematical treatment to stochastic processes and other existing mechanisms in the microscopic scale, it can be consistently shown that the movement, rotation, and interaction between the magnetic domains at their interfaces (also called magnetic walls) are fundamentally responsible for significant losses in the ferrite materials. The theory of magnetic domains and domain wall motion is comprehensibly described in [3].

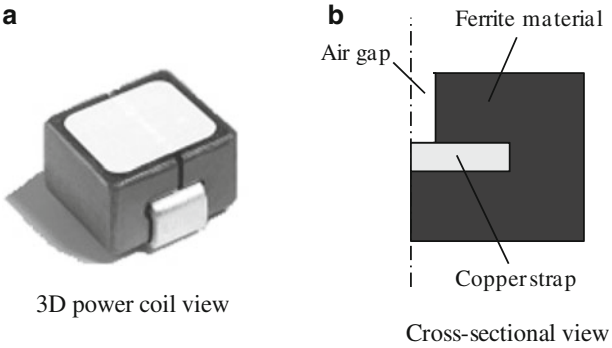

Fig. E.18 Commercial power coil inductor for high-current, high-switching frequency operation from Coilcraft (part number SCL7649S-360KL). 3D view and 2D cross-sectional representation. Total airgap = 850 μm

The three loss components derive from macroscopic models of the magnetic medium can be combined with the field calculations provided that the field sources are known. The latter is not a generalization given the fact that magnetic losses can influence the current waveforms, in which case the direct coupling existing between the loss and field equations may need to be taken into account.

The following subsections briefly describe the underlying physics of magnetic losses and the model implementation with the software package Comsol Multiphysics [1]. The description is illustrated with modeling results referring to the commercial power inductor of Fig. E.18a [4], from which specific material data are available. The geometry is simplified and described in 2D as depicted in Fig. E.18b. Likewise, other coil structures may be analyzed based on the same proposed methodological approach.

E.4.1 Classical Eddy Current Loss Model

Classical Eddy current losses are calculated from Maxwell's equations as described in Sect. E.1 and illustrated for the cases of the PCB and package impedance calculations of Sects. E.2 and E.3. From a macroscopic perspective, the magnetic material is assumed to be homogeneous where the effects of magnetic domains are averaged out.

E.4.2 Hysteresis Loss Model

The survey of magnetic core material models provided in [5] shows the great diversity of approaches to describe magnetization phenomena. Among the most

widespread hysteresis models is that of Jiles–Atherton (J–A) [6], which can predict the associated hysteresis losses by a nontrivial differential function dependent on the magnetic field. One of the advantageous features of the J–A model is that such differential equation is computationally efficient, simple to use, and employs few and physically related material parameters.

In the J–A model, magnetization M is represented as the sum of the irreversible magnetization M_{irr} due to domain wall displacement and the reversible magnetization M_{rev} due to domain wall bending. In the ideal case, where the solid is free of impedances to changes in magnetization, the relation between M and magnetic field H follows a single-valued curve referred to as the anhysteretic curve M_{an} (i.e., curve without hysteresis), which is represented with a modified Langevin expression. Along this curve, both M_{rev} and M_{irr} take place at low H, whereas M_{irr} dominates at higher H. In the region of saturation, where all domain moments line up, domain rotation processes may dominate and be responsible for additional quasi-static effects, which are not considered by the presented approach.

The model's fundamental assumption for the cause of hysteresis in ferromagnets is the presence of pinning sites in the solid that locally oppose the motion of domain walls and trigger domain wall bulging. The pinning mechanism arises as a consequence of imperfections in the material such as dislocations, nonmagnetic inclusions within the grain, and inhomogeneous strains, all of which are identified without distinction as pinning sites or impedances to domain wall motion.

In terms of energy balance, the magnetization energy is the difference between the energy produced by the bulk magnetization in the lossless case and the energy associated to the frictional type of force produced by the pinning sites. This yields the following differential expression for the irreversible magnetization,

$$\frac{\mathrm{d}M_{\mathrm{irr}}}{\mathrm{d}H_{\mathrm{e}}} = \frac{M_{\mathrm{an}} - M_{\mathrm{irr}}}{k\delta}. \tag{E.13}$$

Parameter k is the pinning coefficient and is related to the density of pinning defects in the medium. Also, $\delta \equiv \mathrm{sign}(\mathrm{d}H_{\mathrm{e}}/\mathrm{d}t)$, where $H_{\mathrm{e}} = H + \alpha M$ is an effective field, and is analogous to the Weiss mean field experienced by the individual magnetic moments within a domain.

The total magnetization M is expressed as the sum of M_{rev} due to domain wall bending and M_{irr} due to wall displacement, i.e.,

$$M = M_{\mathrm{irr}} + M_{\mathrm{rev}}. \tag{E.14}$$

The reversible component is proportional to the difference between M_{irr} and M_{an}, giving,

$$M_{\mathrm{rev}} = c(M_{\mathrm{an}} - M_{\mathrm{irr}}). \tag{E.15}$$

The anhysteretic curve, which is the locus of global equilibrium states, is empirically defined with a modified Langevin expression,

$$M_{\mathrm{an}}(H_{\mathrm{e}}) = M_{\mathrm{s}}\left(\coth\left(\frac{H_{\mathrm{e}}}{a}\right) - \frac{a}{H_{\mathrm{e}}}\right). \tag{E.16}$$

Parameter a has dimensions of magnetic field and characterizes the shape of M_{an}, whereas M_{s} defines the saturation magnetization.

Figure E.19 illustrates the use of the presented model to closely reproduce the characteristic B–H curves of a commercial ferrite material. A representation of the decomposed magnetization field is shown in Fig. E.20.

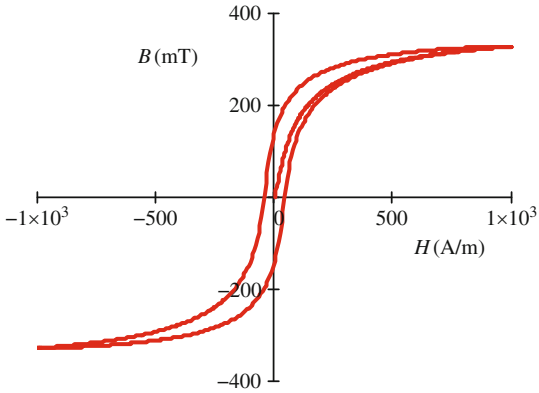

Fig. E.19 Jiles–Atherton model based representation of typical $B(H)$ loop of the 3F5 material from Ferroxcube at 100°C. Parameter values: $M_{\mathrm{s}} = 2.9 \times 10^5$ (A/m), $a = 115$ (A/m), $k = 280$ (A/m), $c = 0.77$, $\alpha = 0.001$

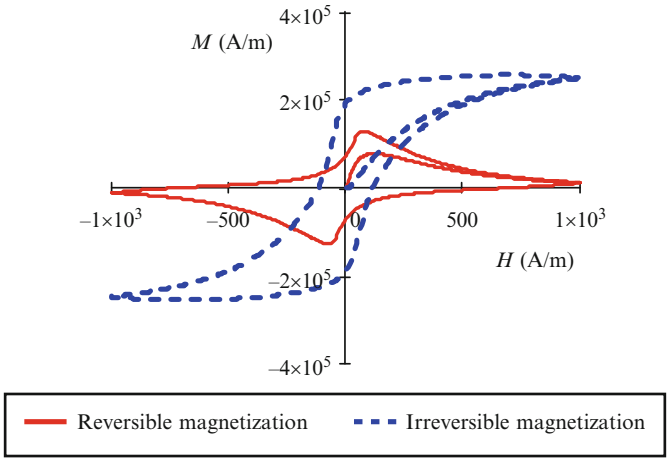

Fig. E.20 Reversible and irreversible magnetization curves corresponding to the $B(H)$ loop example of Fig. E.19

The hysteresis model is implemented in the device physics simulator. After computing the field distribution, the hysteresis energy losses can be numerically calculated from,

$$w_{\text{hys}} = \int_0^B H \, \mathrm{d}B. \tag{E.17}$$

Equation (E.17) is expressed in J/m^3. The total power loss thus results from integrating the energy over the entire volume and multiplying the Joules quantity by the switching frequency.

E.4.3 Excess Loss Model

Thus far, Eddy current losses formulated under the basis of the classical electromagnetic field theory have been calculated in homogeneous materials such as PCB traces and package leads. In ferromagnetic materials, however, additional Eddy current losses arise due to the existence of magnetic domains and the dynamics of their associated domain walls. Namely, when the excitation field varies, the domain walls move accordingly producing changes in the magnetization only in or near the domain walls, leaving the magnetization inside the bulk practically unchanged. Since domain walls occupy only a small fraction of the total volume, the change in the magnetization in and around the walls has to be much larger than the average magnetization over the entire specimen. As a consequence, the locally induced Eddy currents by fluctuations of the flux density caused by domain wall motion are generally higher than those calculated on the basis of uniform magnetization. The formed *excess field* H_{ex}, which is part of the external field needed to compensate the fields originated by the local Eddy currents, gives rise to additional losses termed *anomalous* or *excess losses*.

The concept of magnetic object MO, corresponding to a group of neighbor walls evolving in a highly correlated fashion, is introduced in [3] in order to take into proper consideration the role of these short-range internal correlation fields. It is then assumed that H_{ex} is proportional to the velocity of variation of the local flux induced by MO moving. This proportionality is given in (E.18), where G expresses the MO friction coefficient and σ the material's conductivity.

$$H_{\text{ex}} = G\sigma \frac{\mathrm{d}\phi}{\mathrm{d}t}. \tag{E.18}$$

The velocity of variation of the global flux $S(\mathrm{d}B/\mathrm{d}t)$ results from the contribution of the number n_{om} of MO taking place in the magnetization process. This is expressed as,

$$S\frac{\mathrm{d}B}{\mathrm{d}t} = n_{\text{om}}(t)\frac{\mathrm{d}\phi}{\mathrm{d}t}. \tag{E.19}$$

Parameter S is the cross-sectional area of the magnetic material with assumed sheet shape. Experimental results obtained by Bertotti for several crystalline magnetic materials show that there exists a linear relationship between H_{ex} and n_{om} as,

$$n_{\mathrm{om}} = \frac{H_{\mathrm{ex}}}{V_0}. \tag{E.20}$$

The energy loss per unit volume originated by the n_{om} MO is given by,

$$w_{\mathrm{ex}} = \int_0^T H_{\mathrm{ex}} \frac{\mathrm{d}B}{\mathrm{d}t}\,\mathrm{d}t. \tag{E.21}$$

Combining expressions yields the following expression for the mean value of excess loss in units J/m^3,

$$w_{\mathrm{ex}} = \sqrt{\sigma G V_0 S} \int_0^T \left|\frac{\mathrm{d}B}{\mathrm{d}t}\right|^{\frac{3}{2}} \mathrm{d}t. \tag{E.22}$$

The term outside the integral sign can be adjusted to best match the specific power loss plots from the manufacturer datasheets [7, 8].

E.4.4 Simulation Results

Figure E.21 depicts the inductor current resulting from applying a zero average square voltage as in the buck converter operation. From the ripple current, the total inductance is estimated to be 33 nH, a value within the specified range according to the specifications of the miniaturized coil. From the total inductance, 27 nH are actually resulting from the simulated cross-sectional area of the power

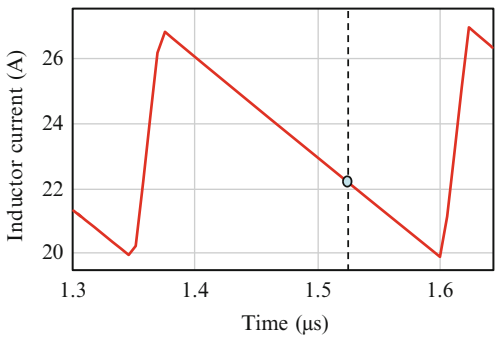

Fig. E.21 Example of simulated steady-state current resulting from an applied squared voltage as in a buck converter with $V_{\mathrm{in}} = 12$ V, $V_{\mathrm{o}} = 1$ V, $F_{\mathrm{s}} = 4$ MHz and 23 A load current

coil. The other 6 nH are added to account for the total portion of the external leads.

The magnetic flux density plot of Fig. E.22 reveals high stress in the interior corners and airgap boundaries of the ferrite core that may induce local magnetic saturation with a consequent loss increase and development of hot spot areas.

The current density distribution of Fig. E.23 describes high current crowding in the region nearby the airgap, thus suggesting a dramatic increase of the conductor resistance in the MHz frequency range. The graph further indicates that the low conductivity of the ferrite appears very effective in this frequency range as no signs of Eddy current across the core are present.

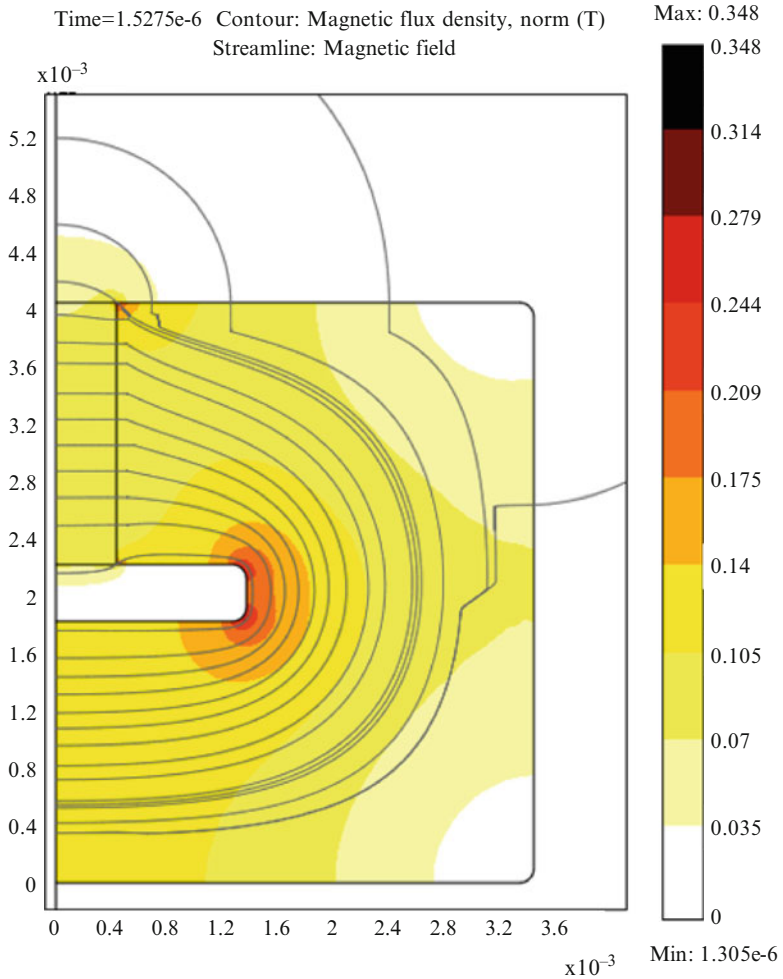

Fig. E.22 Magnetic flux density and field lines corresponding to the transient simulation of Fig. E.21 at time $t = 1.53$ μs

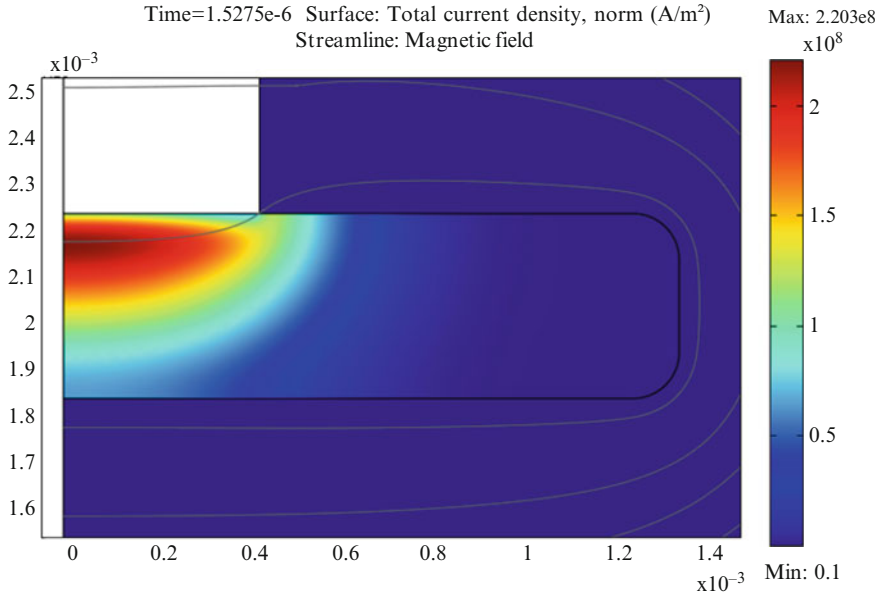

Fig. E.23 Total current density distribution and magnetic field lines corresponding to the transient simulation of Fig. E.21 at time $t = 1.53$ μs

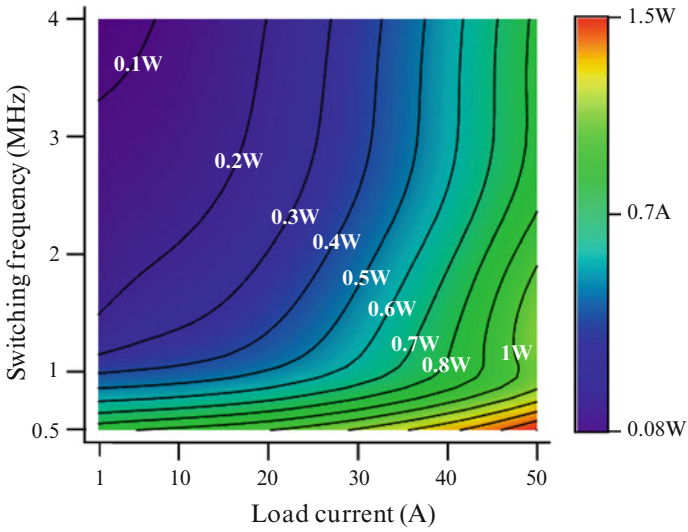

Fig. E.24 Simulated losses of a buck converter coil as a function of the switching frequency and load current at $V_{in} = 12$ V, $V_o = 1$ V, and 100°C. Reference part: SCL7649S-360 from Coilcraft

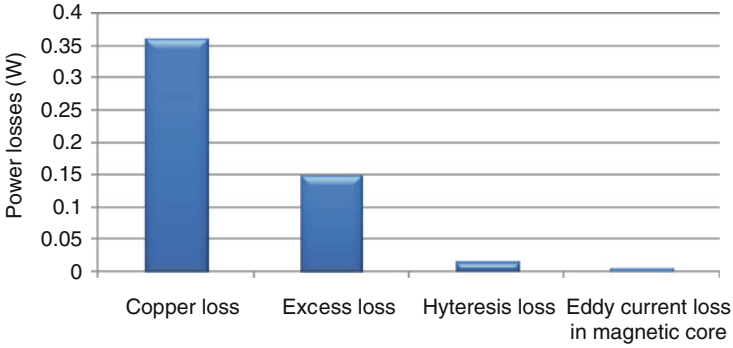

Fig. E.25 Estimated buck converter coil loss breakdown. Simulated conditions: $V_{in} = 12$ V, $V_o = 0.7$ V, $F_s = 2$ MHz, 33.3 A average coil current and 100°C coil temperature

Figure E.24 shows the simulated coil loss as function of the switching frequency and load current under typical VR operating conditions. Due to thermal limitations, the power consumption may typically be limited to a maximum of ~0.5 W, which prevents the use of the inductor in the kHz range to avoid excessive current ripple.

As the contour plot indicates, losses are weakly dependent on the switching frequency above 3 MHz since the ripple current amplitude becomes low. Nonetheless, the maximum load current with negligible ripple current might be lower than 40 A so as to maintain the coil temperature within its specified limits. Higher current operation may be enabled with the used of heat dissipation enhancement measures (e.g., fans).

The loss breakdown of Fig. E.25 shows that in a potential operating target regime heat generation is mainly dominated by copper losses, while hysteresis and Eddy current loss in the magnetic material may be neglected. Excess loss appears as a significant loss mechanism with a ~30% contribution. This is consistent with [8] and references therein.

References

1. Comsol Multiphysics version 3.5a, www.comsol.com
2. Bastos JPA, Sadowski N (2003) Electromagnetic modeling by finite element methods. Marcel Dekker, New York, ISBN: 0-8247-4269-9
3. Bertotti G (1998) Hysteresis in magnetism for physicists, materials scientists and engineers, Academic, New York, ISBN-10: 0-12-093270-9
4. SMT Power Inductors – SLC7649 Series. Datasheet document 481-1, April 2008, www.coilcraft.com
5. Takach MD, Lauritzen PO (1995) Survey of magnetic core models. In: Applied power electronics conference and exposition, APEC, March 1995, vol 2, pp 560–566

6. Jiles DC, Atherton DL (1986) Theory of ferromagnetic hysteresis. J Magn Magn Mater 61: 48–60
7. Albach M, Duerbaum T, Brockmeyer A (1996) Calculating core losses in transformers for arbitrary magnetizing currents a comparison of different approaches. In: 27th annual IEEE power electronics conference, PESC 1996, vol 2, pp 1463–1468
8. Li J, Abdallah T, Sullivan CR (2001) Improved calculation of core loss with nonsinusoidal waveforms. In: IEEE industry applications society annual meeting, October 2001, pp 2203–2210

Appendix F
Quality Factor in Resonant Gate Drivers

For years, resonant gate drivers have been presented as alternatives to conventional solutions to drive power MOSFETs with reduced energy loss. The conceptual idea of resonant gate drivers consists of replacing the resistance of the path through which gate charge flows in the conventional approach by an inductance. With the absence of dissipative elements, the full energy required to change the state of the power device can be controllably recovered and returned to the power supply, or alternatively stored in auxiliary tanks for reuse. Several basic circuit topologies have been proposed to most effectively implement this concept [1, 2].

Commonly, the inductance of the resonant gate drivers determines the switching speed of the power MOSFET as the gate resistance does in the conventional way. Thus, in high-switching frequency applications, the use of low lossy resonant gate drivers featuring low inductance may be of high interest, for size and switching times need also be reduced.

On the other hand, reducing the gate inductance negatively impacts the gate losses as soon as parasitic resistances are no longer negligible. In fact, the gate path circuit is not exempt from dissipative elements. Parasitic resistances exist in the polysilicon gate of the power MOSFET, in the gate switches and as equivalent series to the gate inductance and other storage elements that may be present in the gate circuit. Attempts in reducing the resistance may result in a loss increase due to the parasitic charge of the gate switches. Therefore, whenever the inductance of the resonant gate driver is to be minimized, both the gate parasitic charge and resistance may have to be considered for optimization. This strong loss dependence on the switching speed in resonant gate drivers is in contrast to the behavior of conventional solutions.

Quality factor Q is a measure of the rate of energy dissipation in a resonant system. Q is defined as the ratio of energy stored in the resonant circuit and the energy dissipated per oscillation cycle. Its use is frequent for characterizing the quality of oscillators.

This section makes use of Q to analyze the performance of the resonant gate driver topologies of Fig. F.1 in terms of energy loss, resonant inductor size, and switching speed capability. Simplified resonant gate driver models are expressed as a function of the fundamental variable Q. It results into compact and general analytical close-form expressions that provide easy and direct assessment as to how the different topologies compare. The magnitudes of comparison are given in

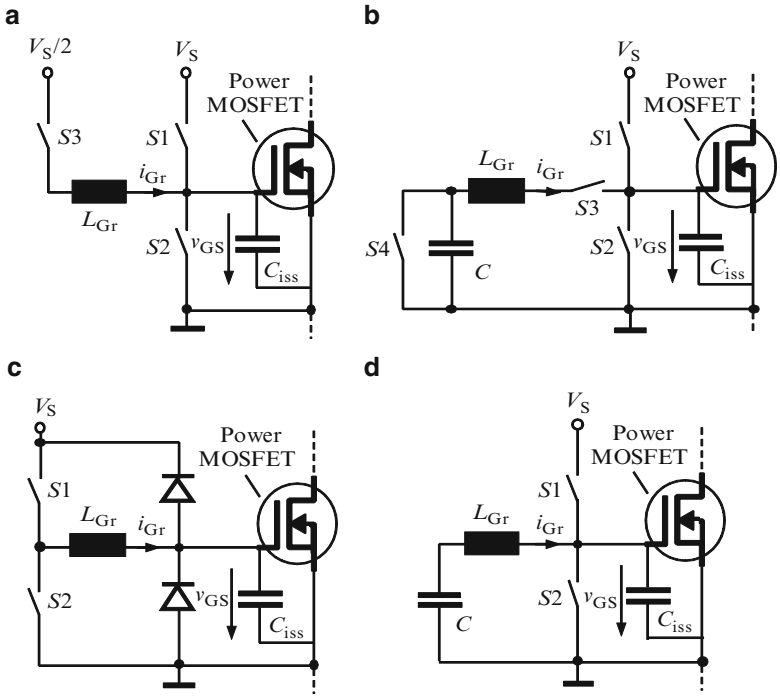

Fig. F.1 Investigated resonant gate driver topologies Topology (a) corresponds to [7], whereas (b) is proposed by 1261 [8], (c) by [9] and (d) by [3].

terms of normalized quantities against performance figures of conventional gate drivers. This further allows highlighting the differences between resonant and conventional solutions, thereby providing further value, generalization, and compactness to the information contained in the equations.

Seeking for the circuit topology that offers maximum switching speed capability at minimum energy loss and inductor size, conclusions reveal that such topology does not exist among those considered. Instead, the topology of choice must result from compromising driving requirements according to a particular application. This is illustrated with an example and demonstrated with circuit simulations employing a rather accurate representation of the gate driver and power MOSFET. The model allows parameters optimization, such as power MOSFET chip size and driving voltage, that minimizes the overall power loss in zero voltage switching applications.

F.1 Gate Driver Requirements

Further loss reduction in resonant gate drivers is possible in detriment of the switching speed, e.g. [3, 4], which usually translates into an increase of switching losses in the power train, i.e., energy dissipation in the channel and/or body diode

Table F.1 Case example. Parameter values of resonant gate driver topology (a)

Basic specifications of synchronous buck converter	Input voltage = 12 V Output voltage = 1.5 V Average output current = 15 A Output ripple current = 6 A Switching frequency = 3 MHz
Power MOSFET (SyncFET)	$C_{iss} = 0.61$ nF/mm^2 Specific ON resistance = 25 mΩ/mm^2 Chip area = 11 mm^2 Polysilicon gate resistance = $R_{GM} = 0.2\ \Omega$
MOSFET switches $S1$ and $S2$	ON resistance = $R_{Sc} = 0.7\Omega$ $C_{iss} = C_{iSc} = 57$ pF $C_{oss} = C_{oSc} = 57$ pF
Two anti-series MOSFET switch $S3$	ON resistance = $R_{Sr} = 0.2\Omega$ $C_{iss} = C_{iSr} = 0.4$ nF $C_{oss} = C_{oSr} = 0.2$ nF (values of one MOSFET)
Gate driving voltages	Gate switches = $V_{drvS} = 3.5$ V, power MOSFET = 7 V ($V_S = 3.5$ V)
Dead times	4 ns for both leading and falling edges
Gate inductor L_{Gr}	25 nH, negligible ESR

of the power MOSFET. In some cases it may even occur that the loss reduction achieved in the gate does not compensate the loss increase in the power train. An optimum switching time must therefore exist that minimizes the overall losses.

Hard-switching operation of the power device usually involves faster switching times than zero voltage switching, ZVS. Since the benefits can thus be greater, this work focuses on the study of resonant gate drivers for ZVS applications.

In the following example, the resonant gate driver (a) from Fig. F.1 is designed to illustrate the demands for driving a synchronous rectifier MOSFET of a step down converter for high current applications. Table F.1 summarizes the most relevant parameters of the proposed application example.

A circuit model of both driver and power MOSFET is employed for carrying out parameter sweeps that yield identification of minimum energy loss conditions. Optimized parameters include the chip area of the power device, inductance L_{Gr}, and driving voltage V_S. Figure F.2 shows simulated waveforms of the steady-state switching cycle operation upon optimized conditions.[3] Both drain current id and drain-to-source voltage v_{DS} are accurately predicted during third quadrant operation, when the losses in the channel and body diode are mainly generated. Note that the third quadrant behavior is modeled according to [5, 6]. Furthermore, the simulation incorporates dead time control functionality to minimize body diode conduction. An algorithm controls the beginning of the turn-on and turn-off times such that the minimum voltage across v_{DS} equals to a predefined value, V_{thd}. In the example of Fig. F.2, $V_{thd} = -0.3$ V, which corresponds to a dead time (t_d) of approximately 4 ns for both leading and falling edge transitions of v_{GS}. Dead time t_d

[3]The loss model is described in the following sections.

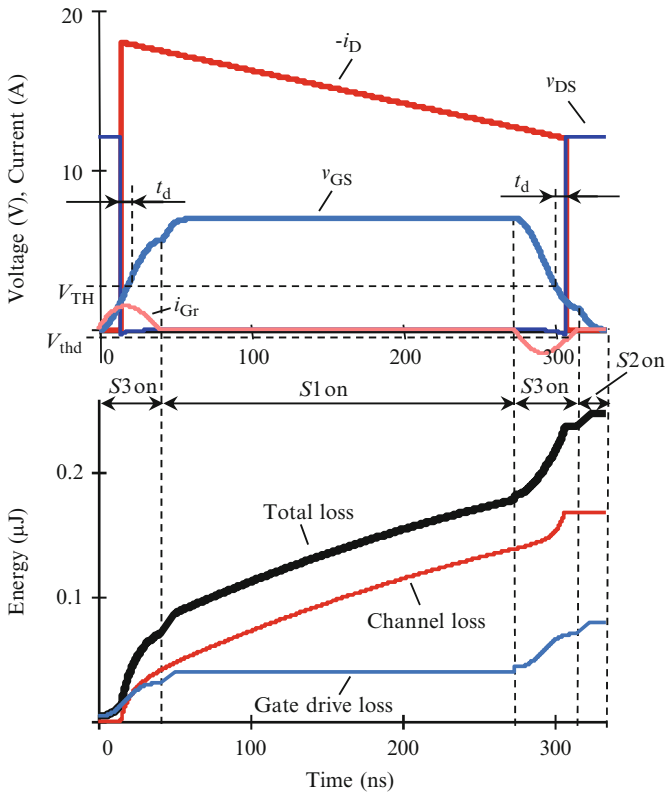

Fig. F.2 Switching cycle operation of topology (a) for a case example upon optimized power loss conditions (see Table C.1)

is defined as the interval between the time instant for v_{DS} to reach the threshold voltage V_{TH} of the power MOSFET and the time of reversion of v_{DS}.

As depicted in the lowest plot of Fig. F.2, energy loss in gate results from current through the parasitic gate resistances during the switching times and from the stored charge of parasitic capacitances from switches $S1$–$S3$. Note that all parasitic elements of the gate circuit are assumed linear. Significant energy loss also occurs across the terminals drain and source during the switching times as a consequence of the channel resistance and current id. This loss contribution can be reduced by further shortening the dead times, or increasing the switching speed. The latter is possible by reducing L_{Gr}, as illustrated in Fig. F.3, which depicts the power loss dependence on resonant inductor L_{Gr} and for various dead times.

It becomes obvious that the dead time increase significantly worsens the overall power loss. Thus, faster switching speed is required, which limits the size of L_{Gr}. In the given example, the optimum size of L_{Gr} varies from 25 nH to just a few nH for a dead time increase of 7 ns. It indicates that the loss reduction achieved with the use

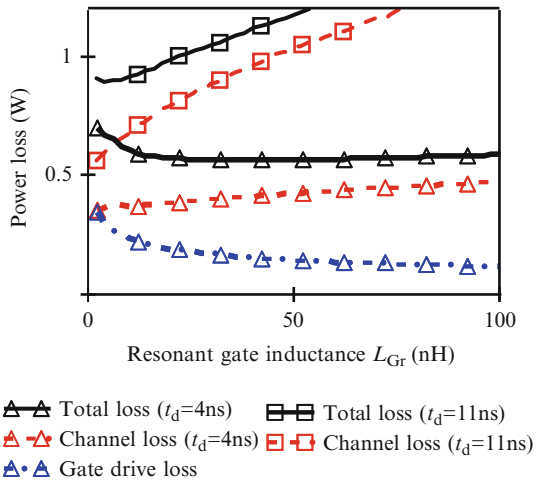

Fig. F.3 Power loss in both power MOSFET channel and gate circuit as a function of L_{Gr} and for various dead times

of resonant gate drivers may be extremely conditioned by the switching speed demands.

F.2 Formulation of Basic Resonant Gate Driver Topologies

This section describes various fundamental resonant gate drive topologies as a function of Q, and compares their performance in terms of switching speed, energy loss, and inductor size.

F.2.1 Basic Resonant Gate Driver Topologies

Figure F.1 shows the four different fundamental resonant gate driver topologies under investigation. Topology (a) corresponds to [7], whereas (b) is proposed by [8], (c) by [9] and (d) by [3].

F.2.2 Assumptions and Definitions

Along the formulation it is assumed that the driven power MOSFET operates in ZVS. Thus, its input capacitance may be assumed fairly linear. A capacitance C_{iss} is defined as the average input capacitance over the operating gate voltage range. Likewise, the output and input capacitance of the gate switches C_{oS} and C_{iS} are

defined as average quantities. The switches of the gate driver are MOSFETs. Their parasitic ON resistance and capacitances are related by the figure of merits $\mathrm{FoM}_i = C_{\mathrm{iS}}R_{\mathrm{S}}$ and $\mathrm{FoM}_o = C_{\mathrm{oS}}R_{\mathrm{S}}$. ON resistance R_{S} is assumed linear and independent on the current flow. Further parasitic elements may also be considered, like the equivalent series resistance (ESR) of the resonant inductor and the gate resistance of the power MOSFET. The turn-on and turn-off times of the gate switches are assumed ideally zero.

Topologies (a) and (b) require switch $S3$ to be bidirectional. Such feature is realized by means of two anti-series MOSFETs.

In the next sections, the energy loss and switching speed of the resonant gate drivers are expressed as normalized quantities against those of conventional gate drivers, which are given by,

$$E_{\mathrm{CGD}} = \frac{1}{2}(C_{\mathrm{iss}} + 2C_{\mathrm{oSc}})V_{\mathrm{s}}^2 + C_{\mathrm{iSc}}V_{\mathrm{DRV(s)}}^2, \tag{F.1}$$

$$\tau_{\mathrm{CGD}} = 5C_{\mathrm{iss}}(R_{\mathrm{GM}} + R_{\mathrm{Sc}}). \tag{F.2}$$

Parameters C_{iSc}, C_{oSc}, and R_{Sc} are the input capacitance, the output capacitance and the ON resistance of the gate switches, respectively. Voltage V_{drvS} is the driving voltage of the gate switches. The energy loss of (F.1) corresponds to one switching transient. The switching time of (F.2) is defined as the time required to reach 99.3% the final value after beginning of commutation. Note that the impact of the parasitic inductances on the switching time is neglected.

F.2.3 Resonant Gate Driver (a)

The principle of operation of this resonant gate driver is described in the example of Fig. F.2. Power loss occurs due to three different causes: the stored charge in the gate switches $S1$–$S3$, the resonant current through the parasitic resistances during the charge of C_{iss}, and the voltage clamping across C_{iss} at the end of the resonant transitions. Based on the aforementioned assumptions the following normalized energy loss expression for one switching transition can be obtained,

$$e_{\mathrm{n(a)}} = \frac{e_{\mathrm{nrc(a)}}\left(1+\frac{\alpha}{2}\right)\beta^2 + \delta + \frac{1}{2}\phi_{\mathrm{a}}\left(\frac{\beta}{2}\right)^2 + 2\phi_{\mathrm{a}}\delta}{\left(1+\frac{\alpha}{2}\right)\beta^2 + \delta}, \tag{F.3}$$

$$\alpha = \frac{C_{\mathrm{iss}}}{C_{\mathrm{oSc}}}, \quad \beta = \frac{V_{\mathrm{s}}}{V_{\mathrm{DRV(s)}}}, \quad \delta = \frac{\mathrm{FoM}_i}{\mathrm{FoMo}}, \quad \phi_{\mathrm{a}} = \frac{R_{\mathrm{Sc}}}{R_{\mathrm{Sr}}}. \tag{F.4 – F.7}$$

As indicated in Table C.1, R_{Sc} and C_{oSc} refer to clamping switches $S1$ and $S2$. R_{Sr} is the ON resistance of any of the two MOSFETs constituting bidirectional

switch $S3$. V_{drvS} is the driving voltage of gate switches $S1$–$S3$. As α increases, expression (F.3) tends to,

$$e_{\mathrm{nrc(a)}} = \frac{1}{2}\left(1 - \mathrm{e}^{-\frac{\pi}{2\sqrt{Q_{\mathrm{a}}^2 - \frac{1}{4}}}}\right). \tag{F.8}$$

The series equivalent resonant capacitance is approximated as the sum of C_{iss} and C_{oSc}, which yields the following quality factor,

$$Q \equiv Q_{\mathrm{a}} = \frac{1}{R_{\mathrm{L}} + R_{\mathrm{GM}} + 2R_{\mathrm{Sr}}}\sqrt{\frac{L_{\mathrm{Gr}}}{C_{\mathrm{iss}} + 2C_{\mathrm{oSc}}}}. \tag{F.9}$$

Resistances R_{L} and R_{GM} are the parasitic ESRs of L_{Gr} and the power MOSFET, respectively.

The normalized switching time can also be analytically calculated as a function of Q as follows,

$$\tau_{\mathrm{n(a)}} = \frac{\alpha + 2}{5\alpha}\frac{\rho_{\mathrm{a}}\pi Q_{\mathrm{a}}^2}{\sqrt{Q_{\mathrm{a}}^2 - \frac{1}{4}}} + \frac{1}{5}\ln\left(\frac{1 - \mathrm{e}^{-\frac{\pi}{2\sqrt{Q_{\mathrm{a}}^2 - \frac{1}{4}}}}}{2\mathrm{e}^{-5}}\right), \tag{F.10}$$

$$\rho_{\mathrm{a}} = \frac{R_{\mathrm{GM}} + R_{\mathrm{Sc}}}{R_{\mathrm{L}} + R_{\mathrm{GM}} + 2R_{\mathrm{Sr}}}. \tag{F.11}$$

The first term in (F.10) refers to the time during the resonant transition, whereas the second one accounts for the time after the activation of the clamping switch, i.e., $S1$ at turn-on, and $S2$ at turn-off. This latter term is valid as long as the voltage across C_{iss} at the end of the resonant transition has not yet arrived at the 99.3% of its final value. It should otherwise be ignored, that is, whenever the term within the logarithm becomes lower than one.

Due to the assumed linearity at the transitions, (F.3)–(F.11) apply to both turn-on and turn-off transients.

F.2.4 Resonant Gate Driver (b)

This topology is conceptually equal to (a) with respect to the resonant charge duration, i.e., half resonant period, as well as the clamping means. The main difference lays in its realization, which allows the use of a single power supply. For an optimum operation, capacitance C is set to equal to C_{iss}, whereas the output capacitance of switches $S1$ and $S2$ should equal half value from that of switch $S4$.

The principle of operation is as follows: Prior to turn-off, switch $S4$ resets voltage across C. At turn-off, the stored energy in C_{iss} is resonantly transferred to

C through switch $S3$. Switch $S2$ clamps v_{GS} to zero at the end of the resonant semi-cycle. The stored energy in C is sent back to C_{iss} at turn-on. Switch $S1$ clamps the ON state to voltage V_S as soon as current i_{Gr} reaches zero at the end of the resonant semi-cycle.

Similarly to topology (a), the normalized energy loss against (F.1) can be calculated by,

$$e_{n(b)} = \frac{e_{nrc(b)}\left(1+\frac{\alpha}{2}\right)\beta^2 + 2\delta(1+\phi_b) + \frac{1}{16}\beta^2\phi_b[4+(1+e^{-\chi_b})^2]}{\left(1+\frac{\alpha}{2}\right)\beta^2+\delta}, \tag{F.12}$$

$$\chi_b = \frac{\frac{\pi}{2\sqrt{2}}}{\sqrt{Q_a^2 - \left(\frac{1}{2\sqrt{2}}\right)^2}}, \quad \phi_a = \phi_b = \frac{R_{Sc}}{R_{Sr}}, \tag{F.13, F.14}$$

$$Q \equiv Q_b \frac{1}{R_C + R_L + R_{GM} + 2R_{Sr}} \sqrt{\frac{L_{Gr}}{C_{iss} + 2C_{oSc}}}, \tag{F.15}$$

$$e_{nrc(b)} = \frac{1}{4}[3 - e^{-\chi_b}(2 + e^{-\chi_b})]. \tag{F.16}$$

Expression (F.12) simplifies to (F.16) for large α. The switching time results, after normalization, in,

$$\tau_{n(b)} = 2\frac{\alpha+2}{5\alpha}\rho_b Q_b^2 \chi_b + \frac{1}{5}\ln\left(\frac{1 - e^{-(\pi/(2\sqrt{2}))\Big/\sqrt{Q_b^2 - \left(\frac{1}{2\sqrt{2}}\right)^2}}}{2e^{-5}}\right), \tag{F.17}$$

$$\rho_b = \frac{R_{GM} + R_{Sc}}{R_C + R_L + R_{GM} + 2R_{Sr}}. \tag{F.18}$$

As in topology (a), the second term in (F.17) should be ignored whenever it becomes negative.

The symmetry of the turn-on and turn-off transitions allows the use of (F.12)–(F.18) to obtain the total power loss in gate.

F.2.5 Resonant Gate Driver (c)

As in drivers (a) and (b), topology (c) resonantly charges C_{iss}. The duration of the transition is though approximately one quarter of the resonant period, just when v_{GS}

is clamped by the action of the diodes. The remaining stored energy in L_{Gr} is delivered to V_S after the resonant interval. The normalized energy loss within one switching interval can be derived from the following expression,

$$e_{n(c)} = \frac{0.5(e_{nr(c)} + e_{nc(c)} + e_{nd(c)})\alpha\beta^2 + \delta + 2\beta^2}{0.5\alpha\beta^2 + \delta + \beta^2}, \tag{F.19}$$

where,

$$e_{nr(c)} = 1 - e^{-2\chi_c}, \tag{F.20}$$

$$e_{nc(c)} = 2\left(\frac{1+\varepsilon_c}{\phi_c}Q_c\right)^2 \ln\left(1 + \frac{\phi_c}{1+\varepsilon_c}\frac{e^{-\chi_c}}{Q_c}\right) + \left(e^{-\chi_c} - 2\frac{1+\varepsilon_c}{\phi_c}Q_c\right)e^{-\chi_c}, \tag{F.21}$$

$$e_{nd(c)} = 2\varepsilon_c\left(\frac{Q_c}{\phi_c}\right)^2\left[\frac{\phi_c}{Q_c}e^{-\chi_c} - (1+\beta)\ln\left(1 + \frac{\phi_c}{1+\varepsilon_c}\frac{e^{-\chi_c}}{Q_c}\right)\right], \tag{F.22}$$

$$\chi_c = \frac{\pi - \tan^{-1}\left(\sqrt[2]{Q_c^2 - \left(\frac{1}{2}\right)^2}\right)}{\sqrt[2]{Q_c^2 - \left(\frac{1}{2}\right)^2}}, \tag{F.23}$$

$$\phi_c = \frac{R_{Sc} + R_L}{R_{Sc} + R_L + R_{GM}}, \quad \varepsilon_c = 2\frac{V_d}{V_S}. \tag{F.24, F.25}$$

Voltage V_d in (F.25) is the forward voltage of the diodes. Their ESR is neglected. The quality factor differs from topologies (a) and (b) as,

$$Q \equiv Q_c = \frac{1}{R_L + R_{GM} + R_{Sc}}\sqrt{\frac{L_{Gr}}{C_{iss}}}. \tag{F.26}$$

The normalized energy losses of (F.20)–(F.22) are related to the resonant transition, the time interval of energy recovery of L_{Gr}, and the contribution of the clamping diodes, respectively.

Finally, the normalized switching time is,

$$\tau_{n(b)} = \frac{1}{5}\rho_c Q_c^2 \chi_c, \tag{F.27}$$

$$\rho_c = \frac{R_{GM} + R_{Sc}}{R_{Sc} + R_L + R_{GM}}. \tag{F.28}$$

Equations (F.19)–(F.28) are applicable to both turn-on and turn-off switching times. For large α, (F.19) simplifies to the sum of (F.20)–(F.22).

F.2.6 Resonant Gate Driver (d)

Unlike topologies (a)–(c), this resonant gate driver employs L_{Gr} as a constant current means to charge C_{iss}. One of the conditions to guarantee the principle of operation is that the time constant formed by L_{Gr} and the parasitic resistances of the charging path has to be much larger than the converter's switching period. For, say, a factor 5 higher, the following minimum Q is required,

$$Q_{\min} = \frac{5\rho_{\mathrm{d}}\sqrt{2}}{\sqrt{d(1-d)p}}, \tag{F.29}$$

where ρ_{d} is defined as,

$$\rho_{\mathrm{d}} = \frac{6p \cdot R_{\mathrm{GM}} + R_{\mathrm{Sc}}(1-6p) + R_{\mathrm{C}} + R_{\mathrm{L}}}{R_{\mathrm{C}} + R_{\mathrm{L}} + R_{\mathrm{GM}}}. \tag{F.30}$$

Furthermore, d is the duty cycle and p is the ratio switching time to the switching period. Resistance R_{C} is the ESR of blocking capacitor C. The quality factor is, for this topology,

$$Q \equiv Q_{\mathrm{d}} = \frac{1}{R_{\mathrm{L}} + R_{\mathrm{GM}} + R_{\mathrm{C}}}\sqrt{\frac{L_{\mathrm{Gr}}}{C_{\mathrm{iss}} + 2C_{\mathrm{oSc}}}}. \tag{F.31}$$

Approximating the input capacitance of the power MOSFET as the sum of C_{iss} and $2C_{\mathrm{oSc}}$, and following the assumptions from [3] yield the following expressions for the normalized energy loss,

$$e_{\mathrm{n(d)}} = \frac{e_{\mathrm{nr(d)}}(\alpha+2)\beta^2 + 2\delta}{(\alpha+2)\beta^2 + 2\delta}, \tag{F.32}$$

$$e_{\mathrm{nr(d)}} = \frac{1+\frac{2}{\alpha}}{6\rho_{\mathrm{d}}pQ_{\mathrm{d}}}\sqrt{\frac{2d(1-d)}{p}}. \tag{F.33}$$

The normalized switching time is,

$$\tau_{\mathrm{n(d)}} = \frac{Q_{\mathrm{d}}}{5}\frac{1+\frac{2}{\alpha}}{\phi_{\mathrm{d}}}\sqrt{\frac{2p}{d(1-d)}}, \tag{F.34}$$

$$\phi_{\mathrm{d}} = \frac{R_{\mathrm{GM}} + R_{\mathrm{Sc}}}{R_{\mathrm{C}} + R_{\mathrm{L}} + R_{\mathrm{GM}}}. \tag{F.35}$$

Finally, combining (F.29) and (F.35) yields the minimum normalized switching time capability of the driver,

$$\tau_{\mathrm{n(d)min}} = 2\frac{\rho_{\mathrm{d}}}{\phi_{\mathrm{d}}}\frac{1 + (2/\alpha)}{d(1-d)}. \tag{F.36}$$

F.3 Topology Comparison

The formulation provided previously is used in this section to compare the proposed topologies. Table F.2 summarizes the values assigned to the gate driver parameters, which may correspond to an application example similar to that of Sect. F.3. Note that parameter α may rather be higher in topologies (a) and (b) than in (c) and (d) as the ON resistance of clamping switches $S1$ and $S2$ of the first ones do not affect Q (see (F.19), (F.15), (F.26), and (F.31)).

Figure F.4 compares the required quality factor among the four topologies. As already indicated, Q increases monotonically with the switching time in all cases, that is to say, the switching time increases with L_{Gr}.

However, there exist large differences in the required Q depending on the topology of choice. Topology (a) features the lowest required Q, whereas topology (d) may need as much as a factor 10 higher than (a) for low p. This translates into an inductance 100 times larger for equal values of C and R in Q.

Somewhere in between is found topology (c), which offers the shortest switching times, even shorter than conventional gate drivers at very low Q. Topology (d) has the lowest switching speed capability, limited to a factor 7 slower than conventional gate drivers in the given example. It is followed by topology (a), with a factor 1.5 slower at $Q = 0.5$.

Figure F.5 compares the loss reduction as function of the switching speed. Requiring the largest Q, topology (d) features the highest energy reduction at low switching times. The overall performance of this driver in terms of loss reduction and Q improves as p increases. Its use is though limited to rather large switching times.

Topology (a) provides the second best energy loss reduction capability at moderate and high-switching times.

Table F.2 Parameter values of the analyzed resonant gate drivers

Topology (a)	$\alpha = 100$, $\beta = 1$, $\delta = 1$, $\phi_{\mathrm{a}} = 2$, $\rho_{\mathrm{a}} = 1$
Topology (b)	$\alpha = 100$, $\beta = 1$, $\delta = 1$, $\phi_{\mathrm{b}} = 2$, $\rho_{\mathrm{b}} = 1$
Topology (c)	$\alpha = 50$, $\beta = 1$, $\delta = 1$, $\phi_{\mathrm{c}} = 0.5$, $\rho_{\mathrm{c}} = 0.95$, $\varepsilon_{\mathrm{c}} = 0.1$
Topology (d)	$\alpha = 50$, $\beta = 1$, $\delta = 1$, $\phi_{\mathrm{d}} = 1.2$, $\rho_{\mathrm{d}}(p = 5\%) = 1$, $d = 50\%$

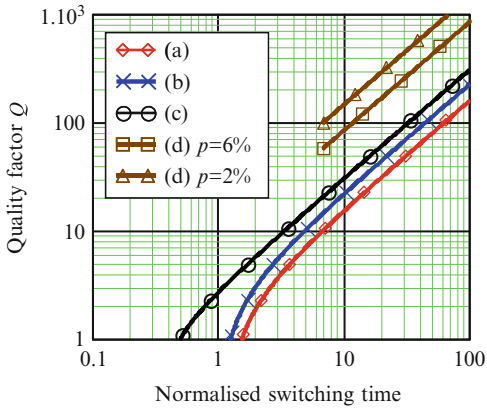

Fig. F.4 Quality factor vs. normalized switching time of the proposed resonant gate driver topologies

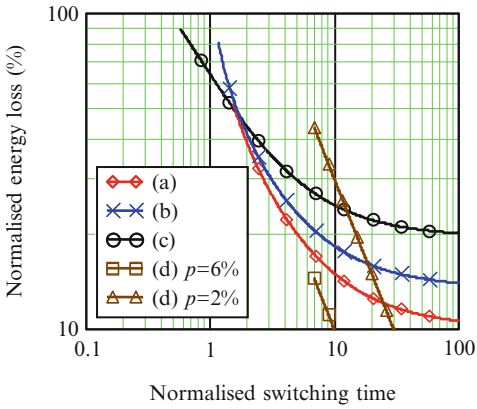

Fig. F.5 Normalized energy loss vs. normalized switching speed of the proposed resonant gate driver topologies

Table F.3 Summary of the topology comparison study

	Switching speed	Inductance size	Loss savings
Topology (a)		✓	
Topology (b)		✓	☒
Topology (c)	✓		☒
Topology (d)	☒	☒	✓

✓ pros; ☒ cons

On the other hand, topologies (b) and (c) show the best performance in switching speed, though in detriment of rather high energy losses, e.g. close to 70% for topology (c) at normalized switching time equal to one.

In general terms, Table F.3 summarizes the information contained in Figs. F.4 and F.5.

F.4 Application Example

The above analysis suggests that the topology of choice must be dependent on the application. This implies to know a priori the characteristics of the power MOSFET, its mode of operation as well as the particular electrical conditions in the power train.

This section compares the performance of a conventional gate driver with topologies (a) and (c) for the application example given in Sect. F.2. In order to ensure minimum power losses, circuit parameters are optimized accordingly, as described in Sect. F.2. Results are shown in Tables F.4 and F.5 for topology (c) and a conventional gate driver, respectively. The optimization results of topology (a) are given in Table C.1.

Power losses are calculated from simulated waveforms as shown in Figs. F.2, F.6 and F.7. The gate drive losses result in the magnitudes predicted by the equations of Sect. F.3. Gate charge losses are obtained considering the assumptions of Sect. F.3.

Figure F.8 shows the overall power loss for each case upon optimized conditions. Topology (c) improves the overall losses (i.e., channel and driver) by 23%, whereas topology (a) does it by 34%. The main improvement with respect to the conventional solution lays on the gate driver part, though channel losses are also reduced. The latter is achieved in topology (a) with a smaller chip size power MOSFET due to a significantly higher V_S value.

The optimum switching time of the resonant gate drivers is relatively high, e.g., 60 ns in case of topology (a). As illustrated in Sect. F.2, this relaxed switching speed requirements are influenced by the soft-switching operation of the power MOSFET as well as the short dead times. Thus, according to Fig. F.5, topologies (a) and (d) provide higher loss reduction than (b) and (c). This agrees with the results of Fig. F.8. The optimized inductance results are also consistent with the predictions of Fig. F.4, i.e., topology (a) offers the lowest inductance, just 25 nH, which might

Table F.4 Optimized circuit parameters of topology (c)

Clamping switches $S1$ and $S2$	Input $R_{DSon} = R_{Sc} = 0.3\ \Omega$, $FoM_i = FoM_o = 40$ ps
Power MOSFET (SyncFET)	Chip area = 13 mm^2
Gate driving voltage	Gate switches $V_{drvS} = 5.5$ V, power MOSFET $V_S = 5.5$ V
Resonant gate inductor L_{Gr}	50 nH, negligible ESR

Table F.5 Optimized circuit parameters of a conventional gate driver

Clamping switches $S1$ and $S2$	Input $R_{DSon} = R_{Sc} = 0.4\ \Omega$, $FoM_i = FoM_o = 40$ ps
Power MOSFET (SyncFET)	Chip area = 13.5 mm^2
Gate driving voltage	Gate switches $V_{drvS} = 4.5$ V, power MOSFET $V_S = 4.5$ V

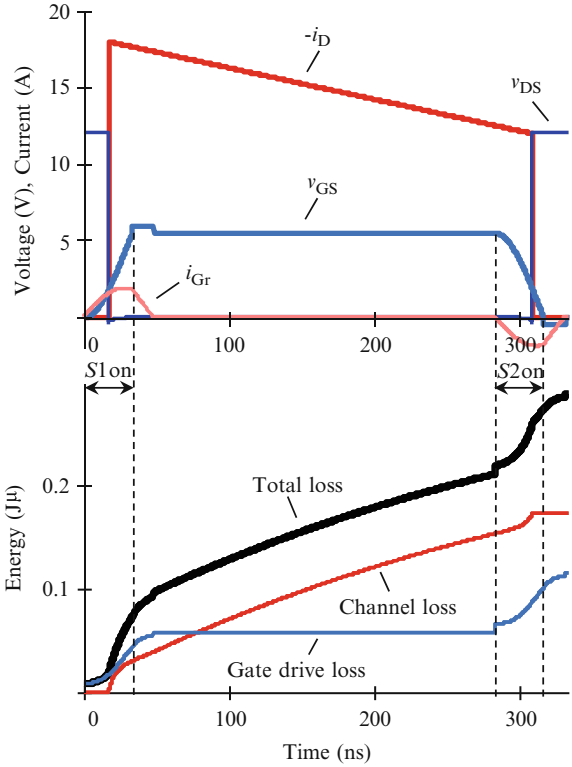

Fig. F.6 Switching cycle operation of topology (c) for a case example upon optimized power loss conditions

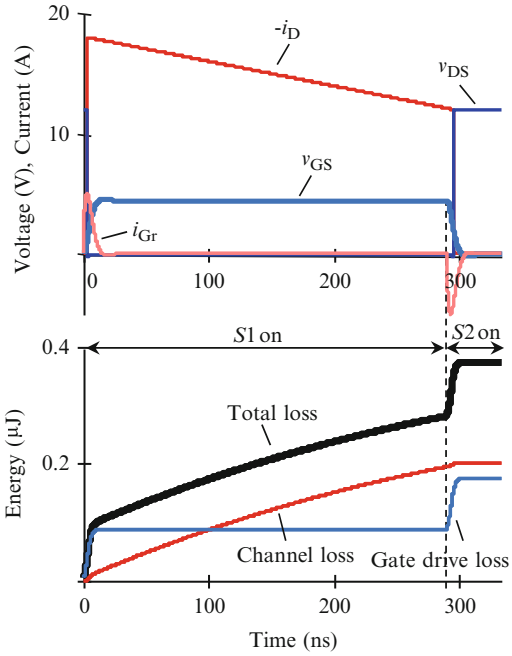

Fig. F.7 Switching cycle operation of a conventional gate driver for a case example upon optimized power loss conditions. Switches *S*1 and *S*2 refer to the upper and lower switch, respectively

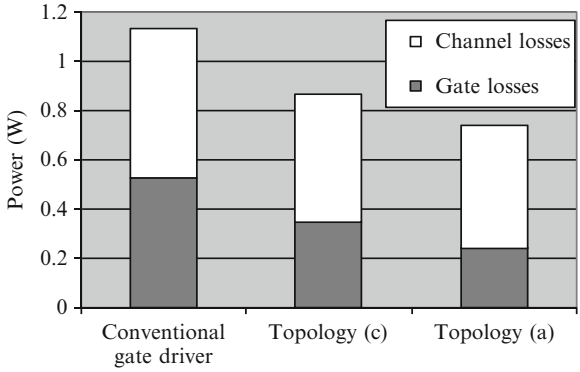

Fig. F.8 Power loss comparison of various optimized gate drivers

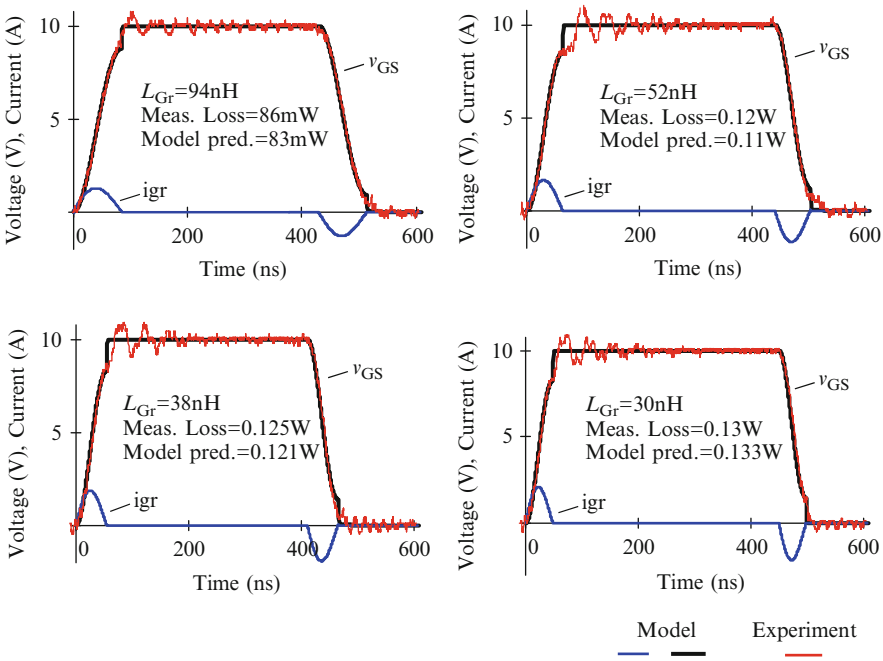

Fig. F.9 Measured and simulated data of topology (a) for various L_{Gr}

well be suitable for integration. This contrasts with typical inductances for topology (d), which may provide even higher loss reduction, yet in detriment of a significantly higher inductance.

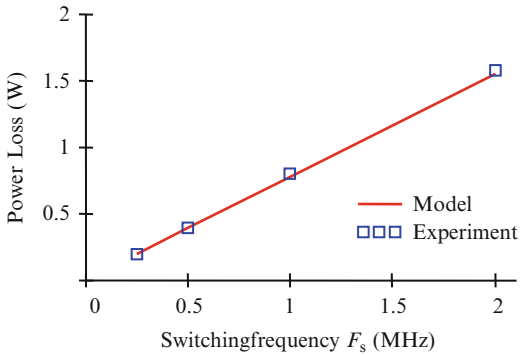

Fig. F.10 Conventional gate driver losses as function of switching frequency

Table F.6 Experimental setup data

Clamping switches *S*1 and *S*2 (used for conventional gate driver as well)	2xN-channel MOSFETs TN0200T from Vishay, $R_{DSon} = 0.25\ \Omega$, $C_{oss} = 160$ pF
Bidirectional switch S3 (two anti-series MOSFETs)	2xN-channel MOSFETs PHN110 from NXP Semiconductors, $R_{DSon} = 0.1\ \Omega$, $C_{oss} = 400$ pF
Power MOSFET (SyncFET)	Replaced by a ceramic capacitor: negligible R_{GM}, $C_{iss} = 6.9$ nF
Gate driving voltage V_s	10 V
Switching frequency F_s	1 MHz (Unless otherwise specified)
Resonant gate inductor L_{Gr}	See Fig. F.9, negligible ESR

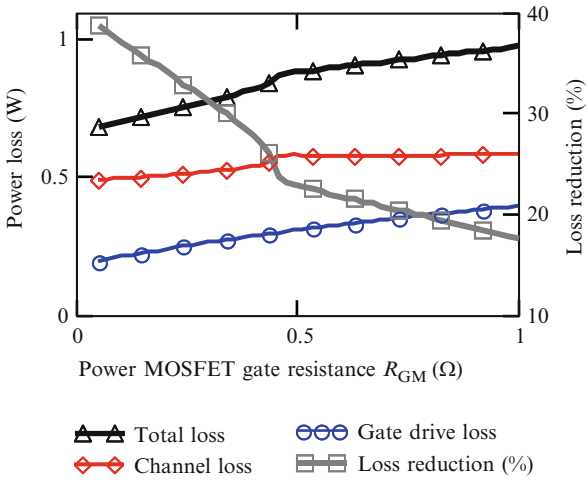

Fig. F.11 Influence of power MOSFET gate resistance on power losses. Results refer to application example of section F.2 employing topology (a)

F.5 Experimental Results

The circuit model and equations of Sect. F.3 corresponding to the conventional gate driver and topology (a) are experimentally validated. Figure F.9 shows the good agreement between experimental and simulated waveforms as well as measured and predicted power losses upon various operating conditions. Note that the gate drive losses of the gate switches are not considered.

In order to validate (F.1), Fig. F.10 compares the measured and predicted power loss of a conventional gate driver. Table F.6 provide information of the measurement setup.

F.6 Discussion and Conclusions

Several aspects shall be considered: First, the polysilicon gate resistance R_{GM} strongly impacts power losses and thus it should be reduced. Current typical values are near to 1 Ω, which may yield to a poor loss reduction, as illustrated in Fig. F.11. Note that the sudden gradient change in the channel loss curve at around 0.45 Ω is entirely attributed to artifacts of the dead time controller. Second, the switching speed of conventional gate drivers is typically limited by the saturation of the gate switches due to the high current peaks. This may be mitigated in resonant gate drivers since current peaks are lower. Third, slowing down the switching speed may limit the use of extreme duty cycles. Four, miniaturization is typically the main motivation for going into high-switching frequency operation. Topologies (a) and (b) may offer the lowest inductance, i.e., the smallest size. Yet, both circuit and mode of operation are in principle more complex than topologies (c) and (d). When size and switching speed are less demanding, then topology (d) may be the most appropriate choice, for its simplicity and reduced power loss. Five, considerations of the power MOSFETs operating conditions are crucial to identify the topology of choice and optimize design parameters.

References

1. Strydom JT, de Rooij MA, van Wyk JD (2004) A comparison of fundamental gate driver topologies for high frequency applications. In: IEEE applied power electronics conference, APEC 2004, pp 1045–1052
2. Dwane P, O' Sullivan D, Egan MG (2005) An assessment of resonant gate drive techniques for use in modern low power DC-DC converters. In: IEEE applied power electronics conference, APEC 2005, pp 1572–1580
3. Maksimovic D (1991) A MOS gate drive with resonant transitions. In: IEEE power electronics specialists conference, PESC 1991, pp 527–532

4. López T, Sauerlaender G, Duerbaum T, Tolle T (2003) A detailed analysis of a resonant gate driver for PWM applications. In: IEEE applied power electronics conference, APEC 2003 pp 873–878
5. Dolny GM, Sapp S, Elbanhaway A, Wheatley CF (2004) The influence of body effect and threshold voltage reduction on trench MOSFET body diode characteristics. In: International symposium in power semiconductor devices, ISPSD 2004, pp 217–220
6. López T, Elferich R, Koper N (2006) Reverse recovery in high density trench MOSFETs with regard to the body-effect. In: IEEE international symposium in power semiconductor devices, ISPSD 2006, pp 1–4
7. Van Der Broeck H, Wendt M, Steinbush H (2006) Method of controlling a circuit arrangement for the AC power supply of a plasma display panel. US7064732B2, 20 June 2006
8. Steigerwald RL. Lossless gate driver circuit for a high frequency converter. Patent US5010261
9. Chen Y, Lee FC, Amoroso L (2004) A resonant MOSFET gate driver with efficient energy recovery. IEEE Trans Power Electron 470–477

Appendix G
Experimental Prototypes

This section presents the circuit diagrams and PCB layouts of the prototype boards employed throughout this thesis work. Three different converter circuits are experimented with for different purposes:

- Synchronous buck converter prototype for switching measurements
- Point-of-load converter based on discrete LFPak based MOSFETs for efficiency measurements
- Multi-phase buck converter based on the IPM PIP212-12M for efficiency measurements

G.1 Synchronous Buck Converter Board

Experimental switching waveforms presented in the model validation section of Chap. 2 are based on the following circuit board. Furthermore, MOSFET characterization parameters such as reverse recovery are also performed with this PCB as it allows both current and voltage measurements in practically all relevant loops and nodes of the switched converter. The board is designed for 30 V MOSFET devices and it allows high-current, high-frequency switching operation. MOSFETs temperature control is enabled by means of thermal pads on the bottom layer, right underneath the switch devices. External pulse generator for the individual control of the switches is required (Figs. G.1–G.6).

Fig. G.1 Synchronous buck converter prototype board. Designed by Dr. Tobias Tolle from Philips Research

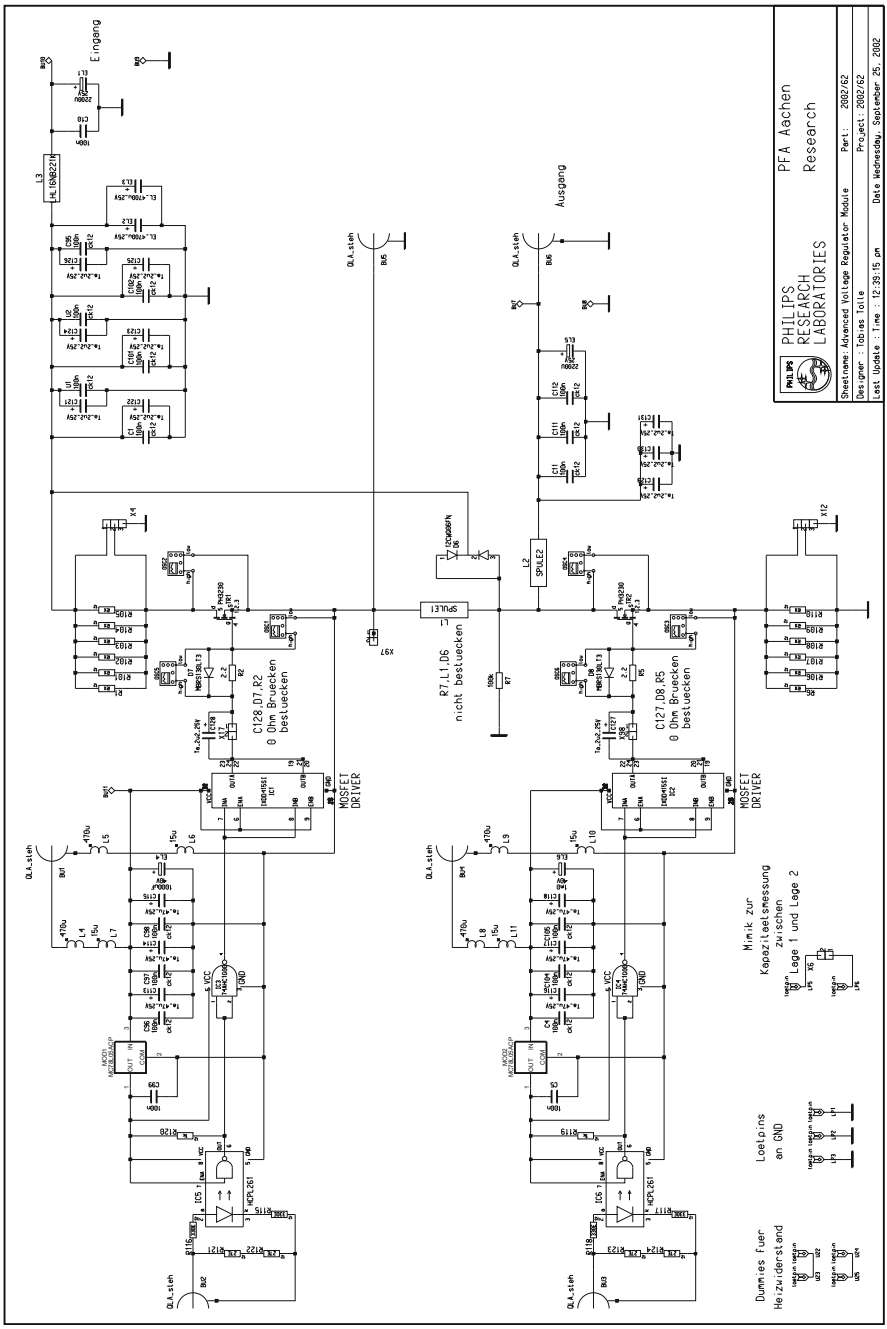

Fig. G.2 Circuit diagram of a synchronous buck converter prototype board of Fig. G.1

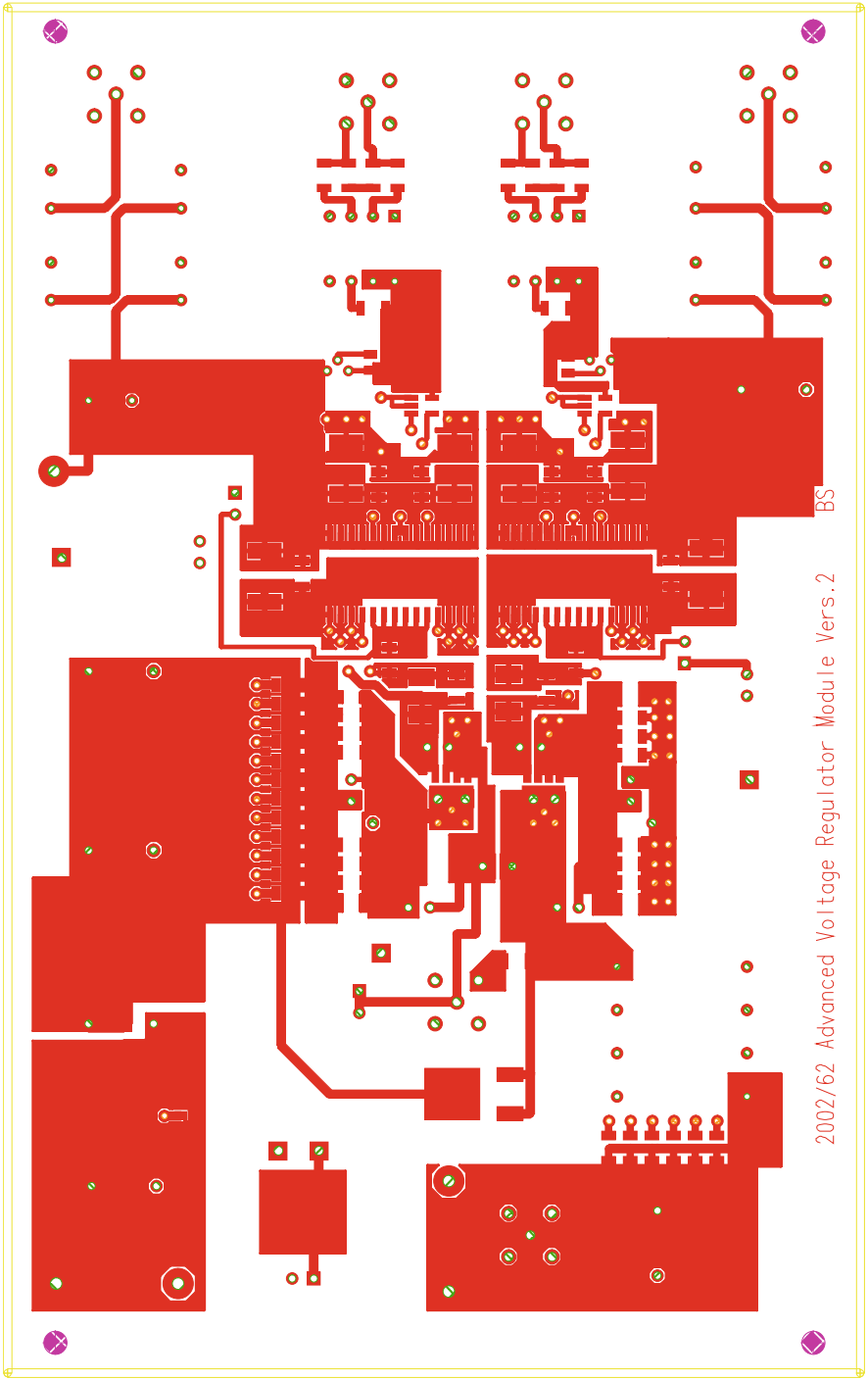

Fig. G.3 PCB design of top layer corresponding to the test board of Fig. G.1

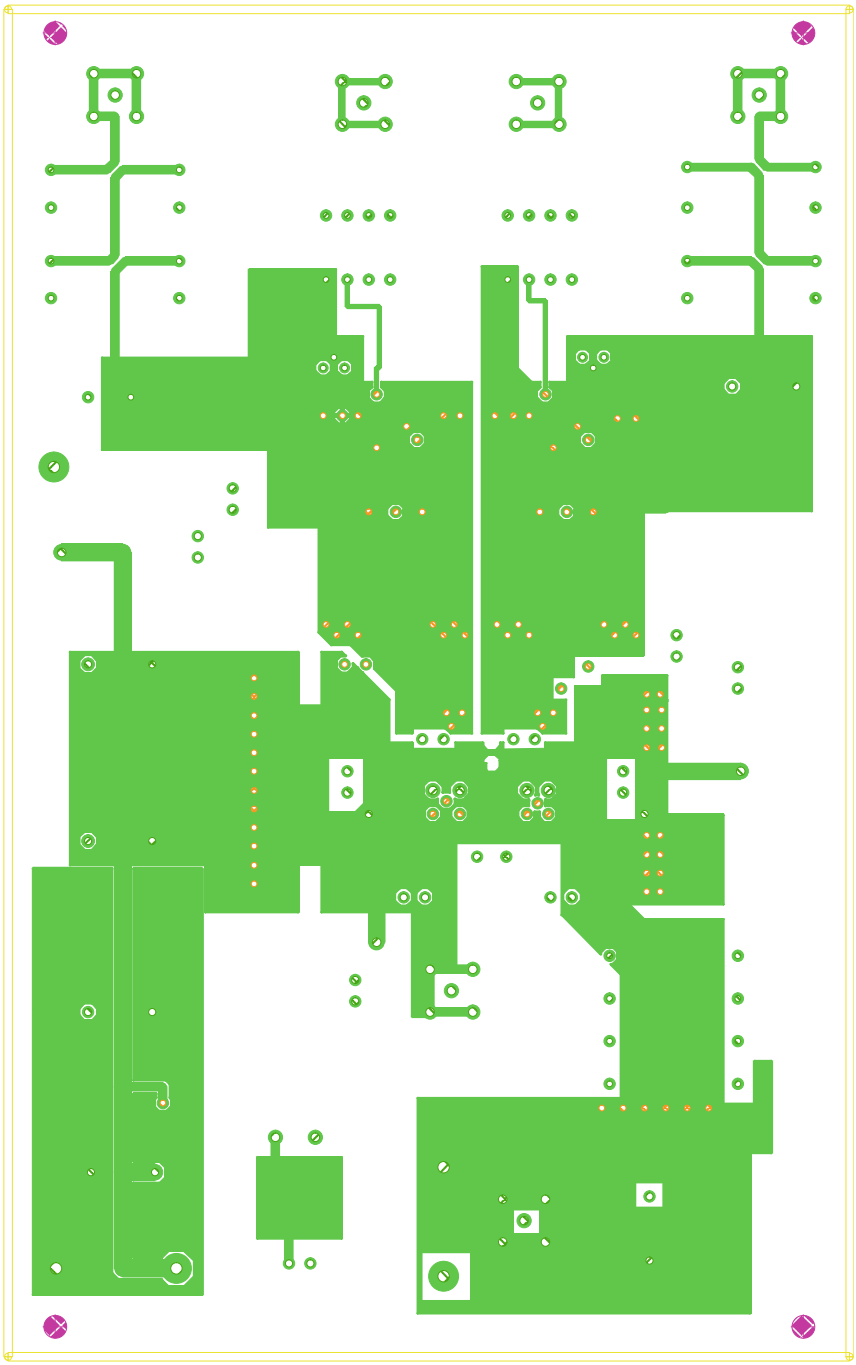

Fig. G.4 PCB design of inner layer corresponding to the test board of Fig. G.1

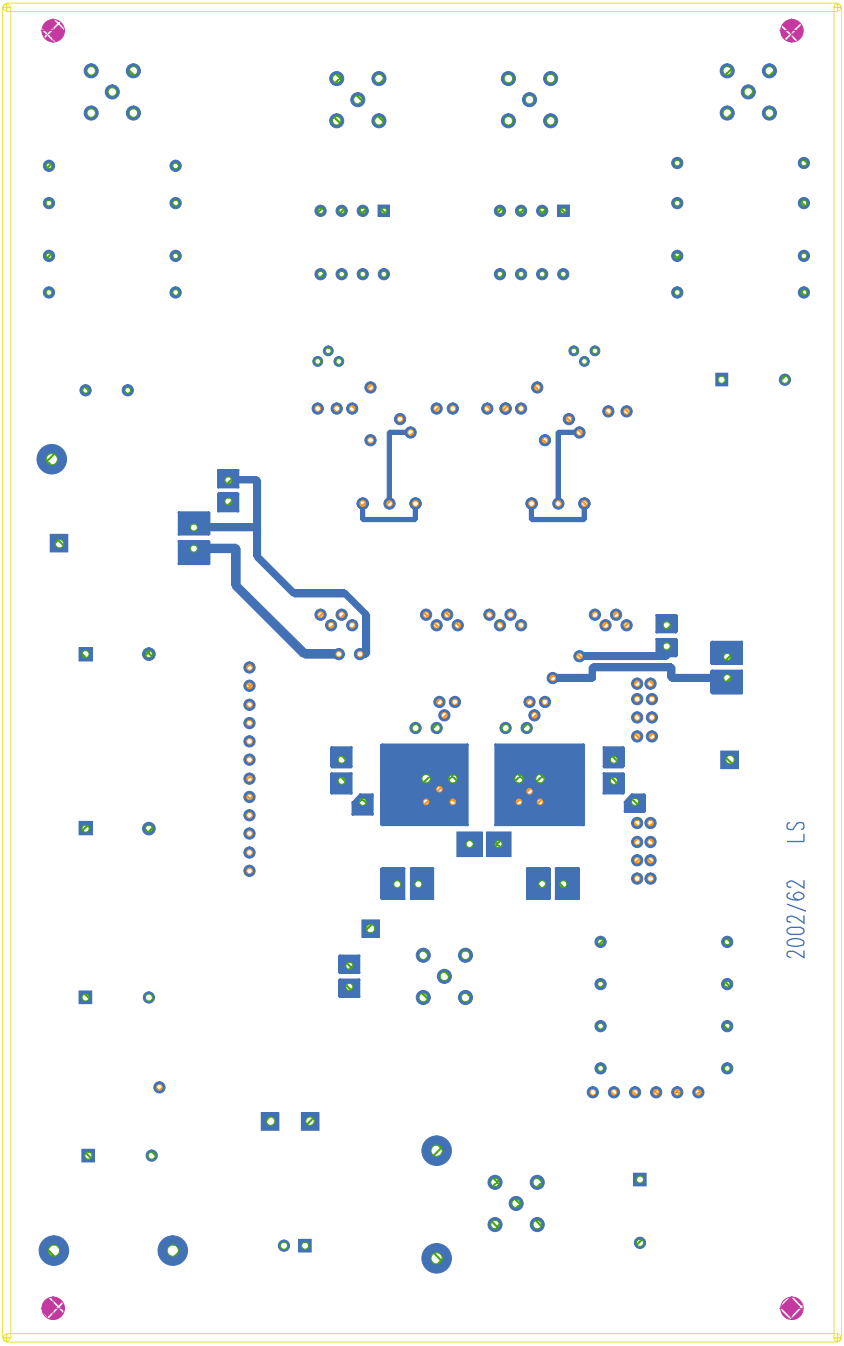

Fig. G.5 PCB design of bottom layer corresponding to the test board of Fig. G.1

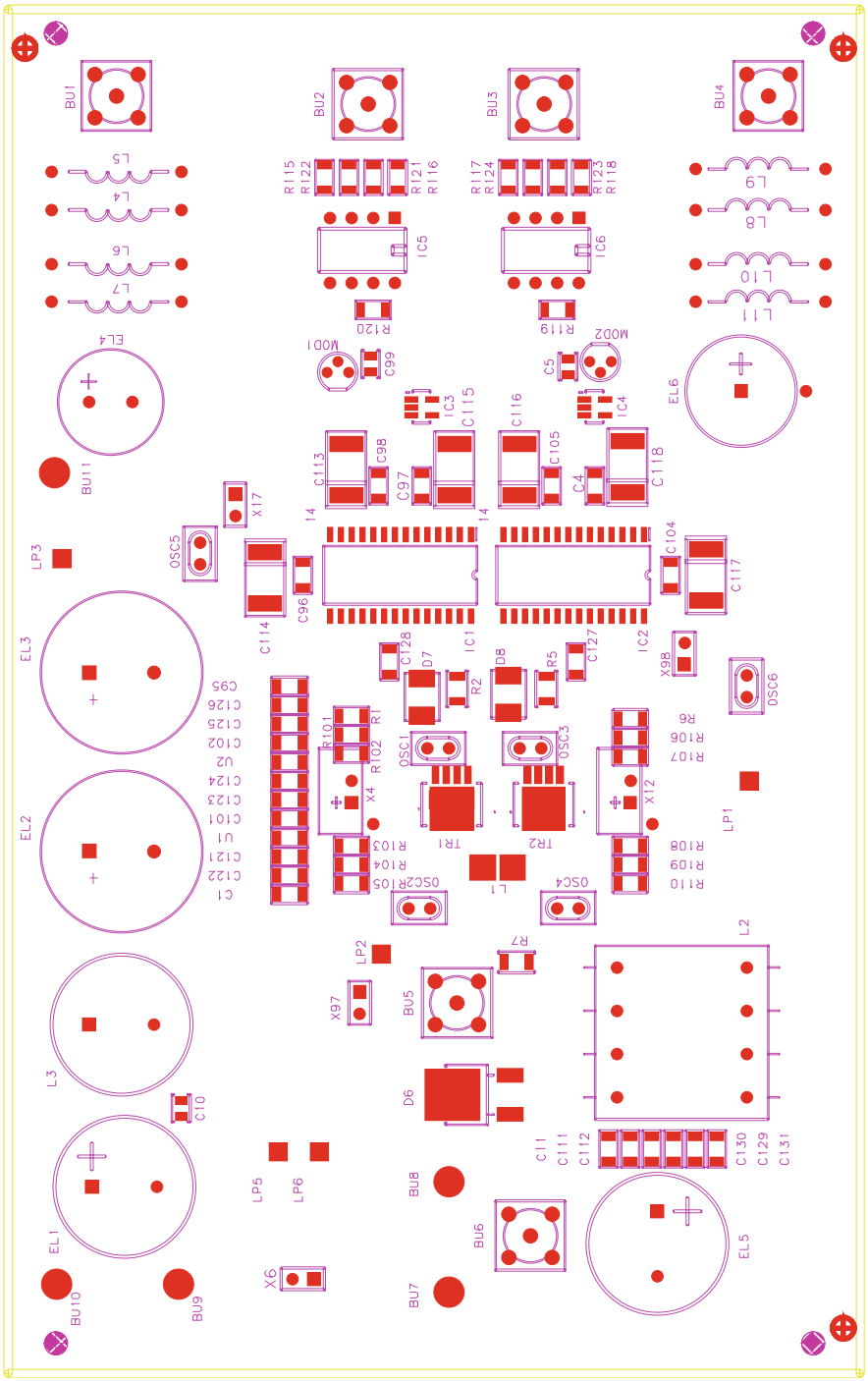

Fig. G.6 PCB design of top overlay corresponding to the test board of Fig. G.1

G.2 Point-of-Load Demo Board

The main purpose of this demo board for LFPak MOSFETs is to demonstrate the highest possible efficiency in an industry standard module size of 33 × 14.2 mm with the existing device technologies. Simulation results comparing Trench4 with Trench6 in Chap. 6 are performed on this test board, which is designed to feature low parasitic inductances and allow load currents up to 20 A. The PoL is equipped with a commercial synchronous buck converter regulator for high-switching frequency operation with automatic dead time reduction and other loss saving features (Figs. G.7– G.11).

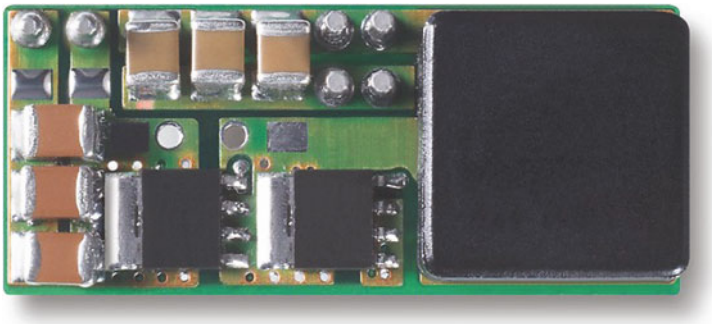

Fig. G.7 Point-of-load demo board. Designed by Victor Guijarro from Philips Semiconductors

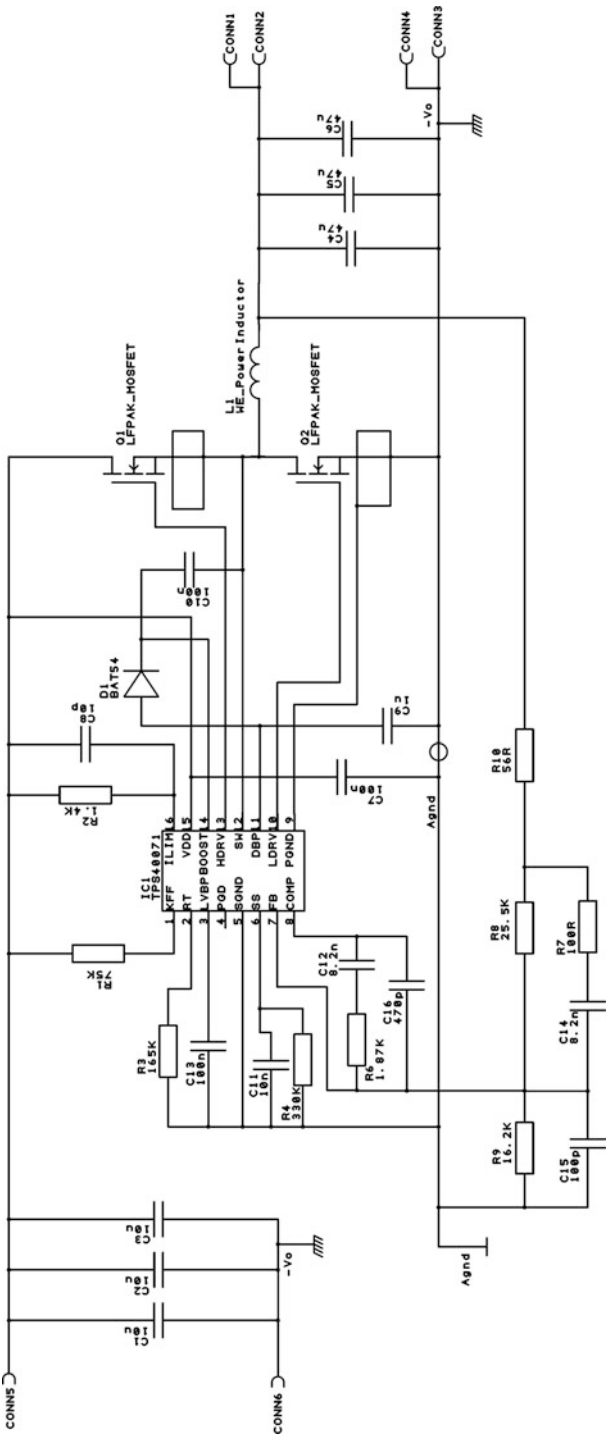

Fig. G.8 Circuit diagram of a synchronous buck converter prototype board of Fig. G.7

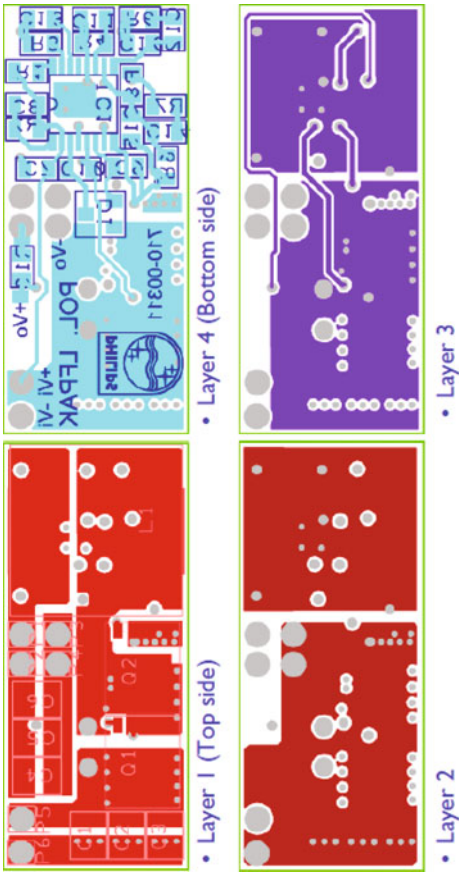

Fig. G.9 PCB layer design corresponding to the demo board of Fig. G.7

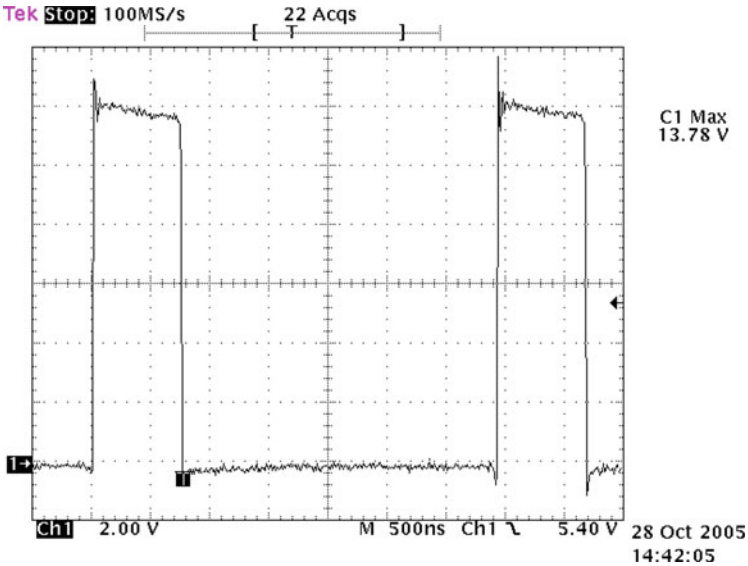

Fig. G.10 Measured switched-node waveform from PoL demo board of Fig. G.7. Employed MOSFETs: PH3330L (SyncFET) and PH8030L (CtrlFET). Conditions: $V_{in} = 12$ V, $V_o = 2.5$ V, $I_o = 17$ A. Scope settings: 500 ns/div

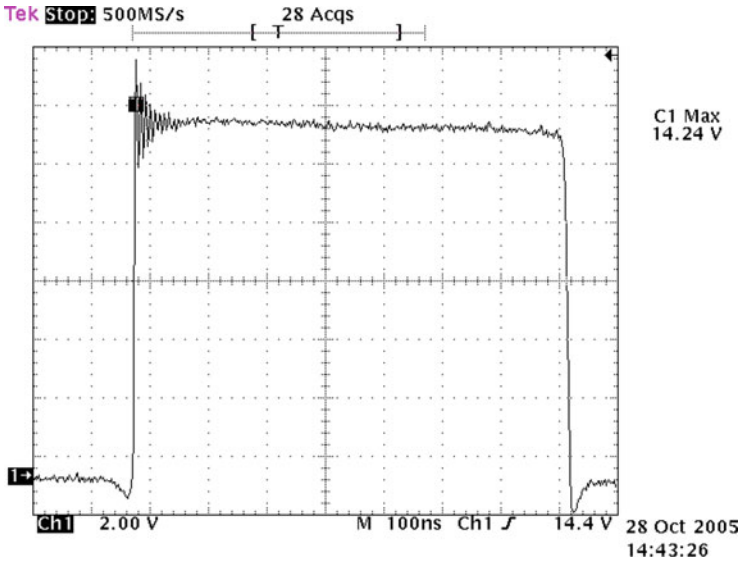

Fig. G.11 Measured switched-node waveform from PoL demo board of Fig. G.7. Employed MOSFETs: PH3330L (SyncFET) and PH8030L (CtrlFET). Conditions: $V_{in} = 12$ V, $V_o = 2.5$ V, $I_o = 17$ A. Scope settings: 100 ns/div

G.3 Multiphase VR Demo Board

This VR demo board allows performance evaluations of the IPM PIP212-12M in multiphase operation driving load currents up to 140 A. The nominal source voltage is 12 V and can be converted down to 0.8 V. Phases are controlled by a central unit and can be individually disabled. The demonstration board contains a low power onboard switching regulator to provide the gate drive voltage of the SyncFET and drive a series of LED indicators, which are turned-off for efficiency measurements. The experimental curves of the PIP212-12M from Chap. 3 are based on this test board (Figs. G.12–G.21).

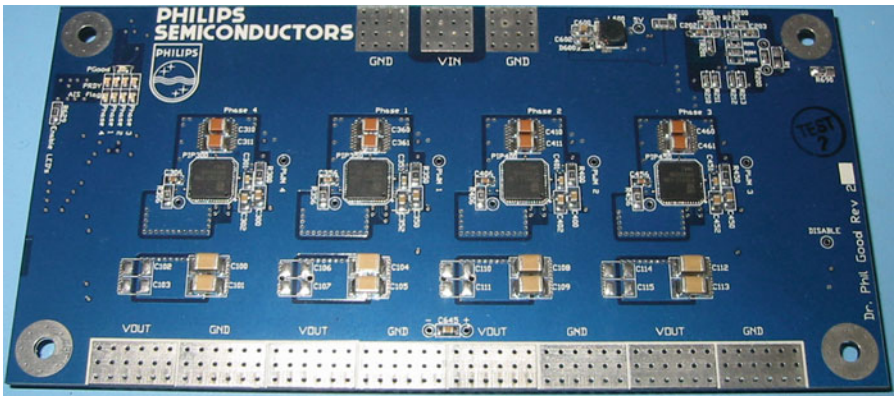

Fig. G.12 Multiphase voltage regulator test board. Designed by Dr. Phil Good, from Philips Semiconductors

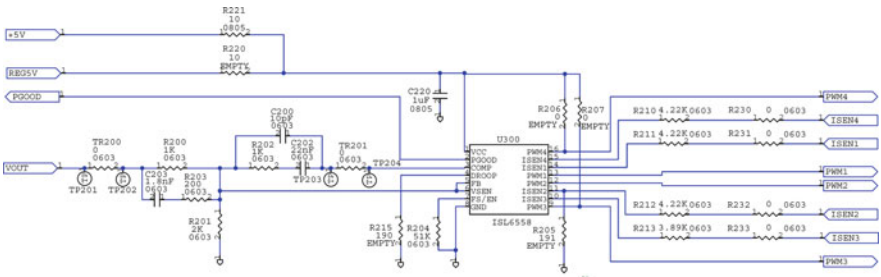

Fig. G.13 Circuit diagram of the multiphase VR test board of Fig. G.12. Multiphase regulator section

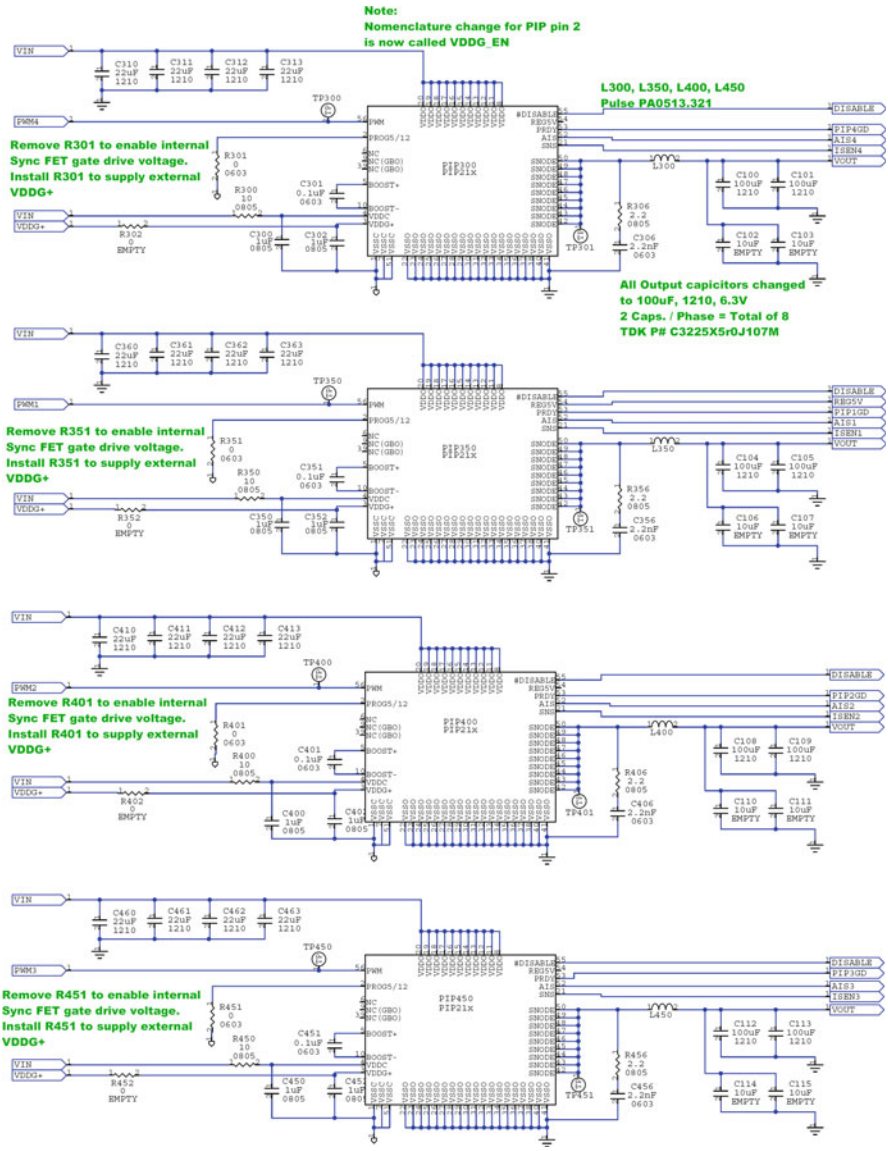

Fig. G.14 Circuit diagram of the multiphase VR test board of Fig. G.12. Converter phases

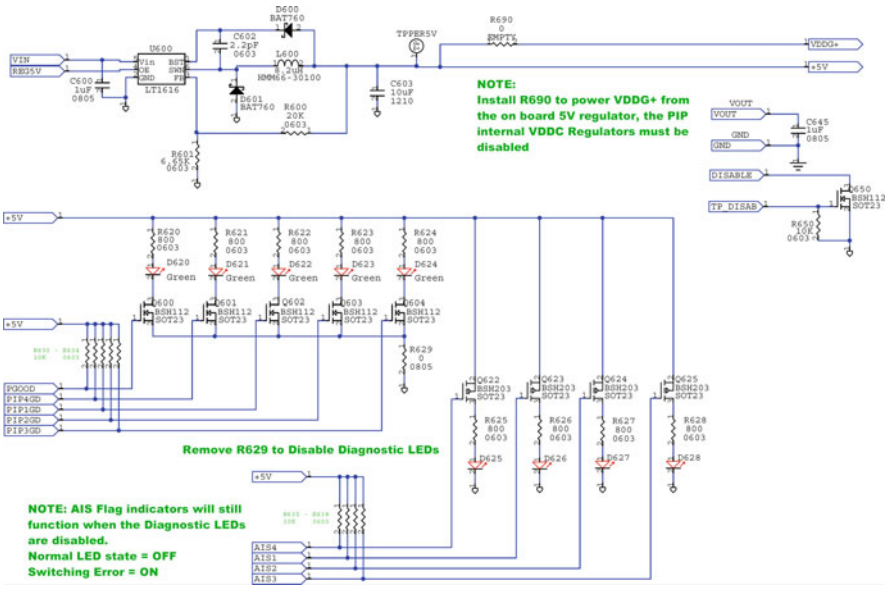

Fig. G.15 Circuit diagram of the multiphase VR test board of Fig. G.12. Low power regulator and signal LED circuitry

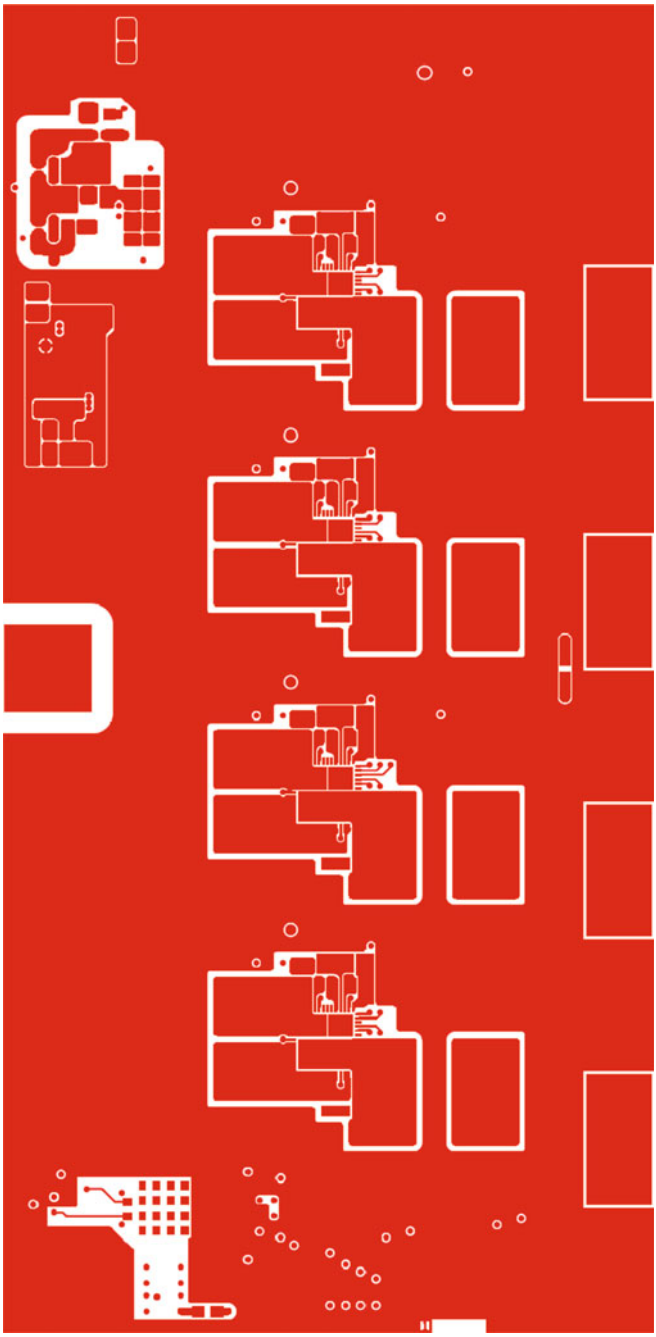

Fig. G.16 PCB design of top layer corresponding to the test board of Fig. G.12

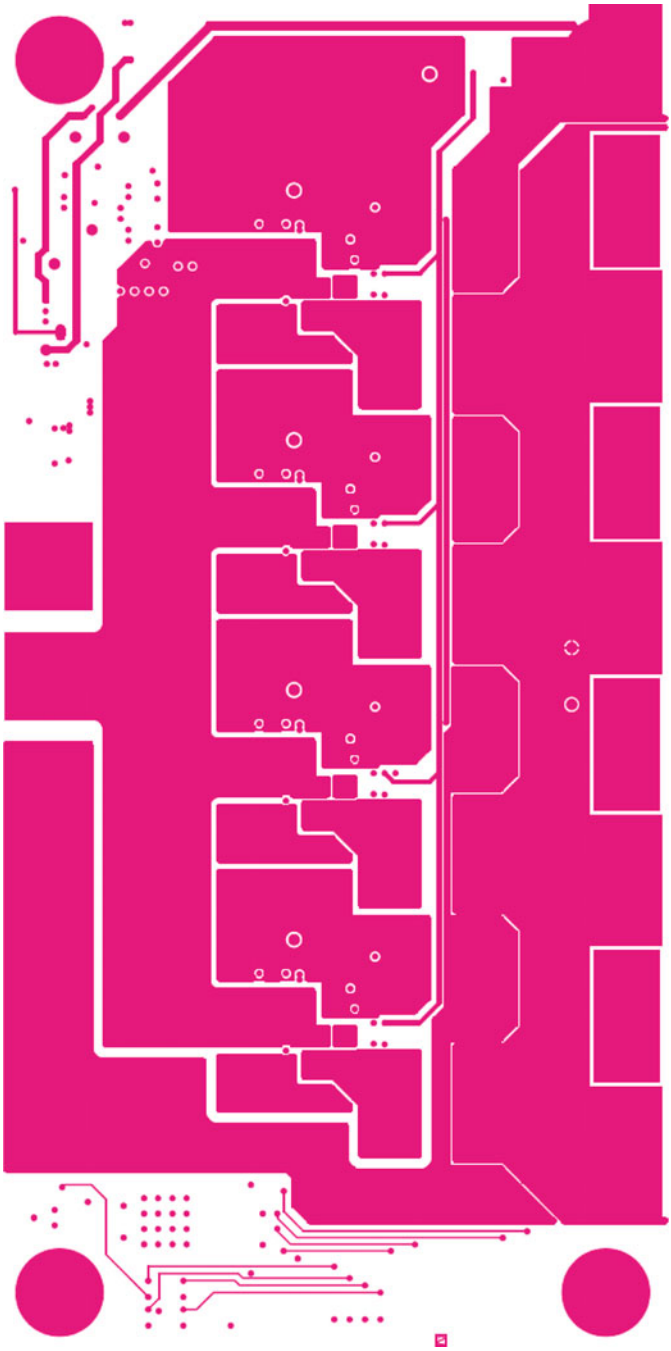

Fig. G.17 PCB design of inner layer 1 corresponding to the test board of Fig. G.12

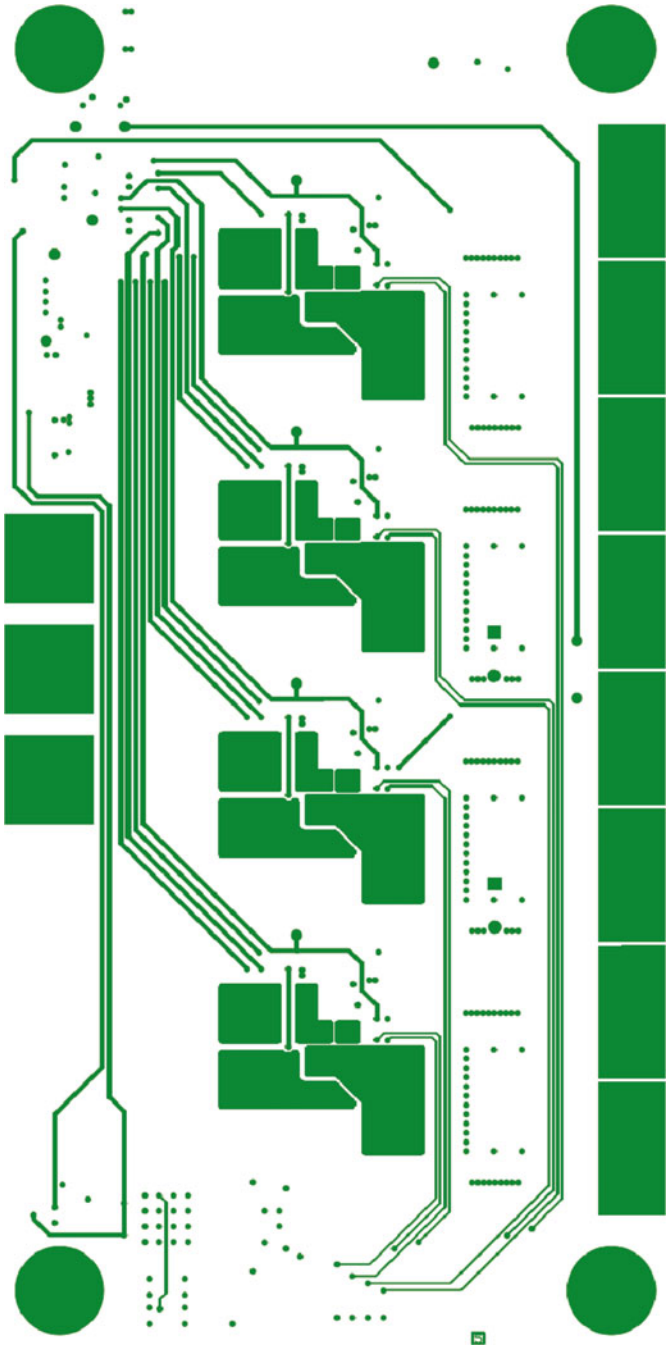

Fig. G.18 PCB design of inner layer 2 corresponding to the test board of Fig. G.12

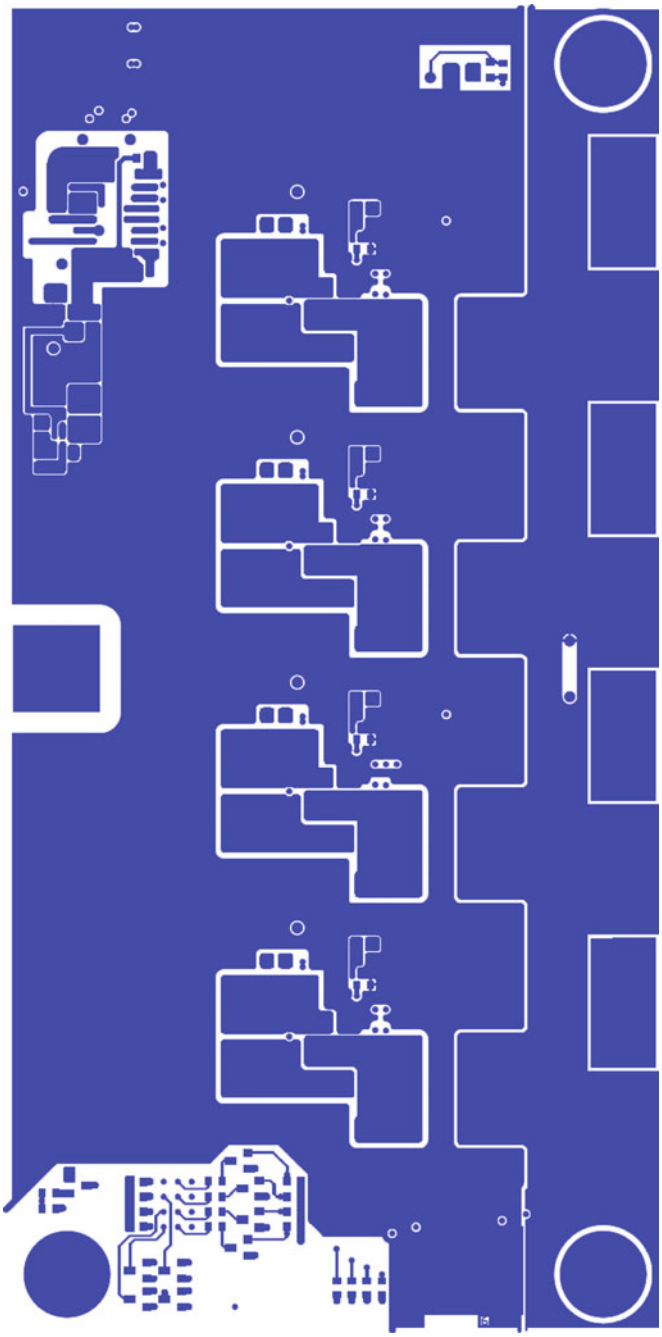

Fig. G.19 PCB design of bottom layer corresponding to the test board of Fig. G.12

Fig. G.20 PCB design of top overlay corresponding to the test board of Fig. G.12

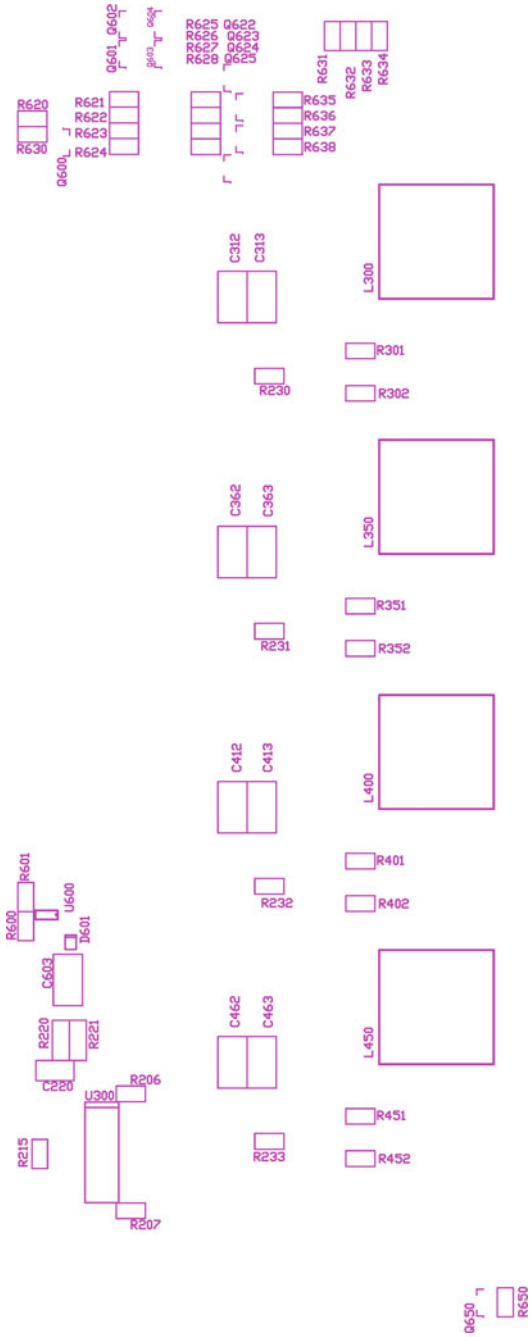

Fig. G.21 PCB design of bottom overlay corresponding to the test board of Fig. G.12

Index

A
Active droop control, 32, 33
Ambient temperature, 11, 12, 103, 111
Amorphous Fe-based, 28
Anhysteretic curve, 350
Anomalous, 351
Anti-series, 359, 362, 372
Avalanche breakdown, 68, 69, 71, 75, 80–82, 85, 104, 106, 112, 113, 118, 120, 122, 123, 126–128, 130, 136, 137, 147, 155, 159–166, 168, 173, 181, 182, 190, 192–194, 198, 204, 210, 231, 232, 256, 258, 264, 275, 281, 330, 333–334
Avalanche breakdown loss, 162, 225–256, 275, 330, 333
Average steady-state controller, 98–100

B
Behavioral modeling, 67–69, 88–90, 304, 306, 307, 359
Board temperature, 11, 12, 232
Body diode, 38, 67, 69–72, 75, 80, 82, 83, 85, 88–90, 97, 99, 115, 117, 121, 123, 124, 128, 137, 138, 161, 163, 166, 167, 176, 181, 184, 207, 210, 218, 231, 240, 280, 282, 285–287, 292–293, 296, 297, 301–311, 313, 316, 318, 320, 324, 330, 333, 358–359
Body diode reverse recovery, 68, 87, 139, 166, 307, 310, 313
Body-effect, 70, 82, 113, 122–128, 301–306
Bond wire, 40, 75, 128, 206, 264, 266
Bus voltage, 16, 17

C
Capacitive current, 73, 85, 203, 205, 301, 304, 306–307, 309, 311, 332
CCM. *See* Continuous conduction mode
Cell pitch, 18
Channel current, 69–70, 82, 85, 92, 125, 128, 137, 142, 144, 147, 148, 155, 156, 191, 203, 229, 285, 293, 295, 297, 301, 302, 304–308, 311, 315, 330, 331
Charging loss, 159–160, 165, 167, 184–188, 198–201, 203, 211, 257, 369
Circuit simulations, 21, 45–47, 52, 68–90, 123, 253, 286, 306–308, 313, 316, 317, 352
Clamped inductive switching, 24, 75, 141, 142, 191
Classical Eddy current loss, 27, 335, 347, 348, 351
Closed-form, 47, 51, 133, 134, 156, 159, 182, 210, 328, 357–358
Concentration of holes, 305–306, 315
Conduction loss, 14, 24, 37–39, 120, 122, 205, 206, 210, 211, 229–231, 233, 235, 250, 253, 255, 257, 259, 260, 266–268, 275, 280, 281, 385, 307, 310
Continuity equation, 198, 316, 319, 335
Continuous conduction mode (CCM), 15, 33, 37, 114
Contour plots, 151, 153, 233, 236, 240, 250, 252, 257, 355
Control signals, 10–12, 92, 97
Converter topology, 13, 14, 246
CoolMOS, 2, 3, 287
CPU fan, 11, 270
Crossover conduction, 23
Curie temperature, 27, 28
Current branch, 327–330
Current crowding, 267, 281, 345, 353
Current hard-switching, 115, 118, 120, 198, 201–205, 256, 331–332
Current loop, 118, 120, 327–334
Current sensing, 35, 36, 84, 96, 98, 103

Current sharing, 17, 30, 32, 33, 35, 128
Curve tracer, 75, 81, 286
Cut-off frequency, 14, 209, 339

D
Damping factors, 157, 170–171, 182, 204, 264
DCM. *See* Discontinuous conduction mode
DC output characteristics, 4, 68, 70, 75, 80–82, 92, 285–298, 301, 311
Dead time, 23, 32, 38, 40, 49, 68, 90, 97–99, 101, 104–106, 114, 115, 121, 123–125, 128, 130, 134, 193, 207, 231, 240, 253, 280, 282, 334, 359–361, 369, 373, 375–376
De-embedding, 82, 83, 301, 305, 311, 314, 324
Deep sleep, 13, 37
Demo board, 90–97, 101, 105–112, 192
Design guidelines, 9, 50, 54, 197, 198, 213, 231–232, 235, 283, 375–394
Design space, 50, 133, 236
Device characteristics, 47, 67–69, 75, 104, 113, 286–289, 307, 314
Device package, 18, 22, 39, 75, 307
Device physics modeling, 48, 53, 81
di/dt problem, 5, 24, 88, 116–118, 143–144
Diffusion current, 88, 301–304, 306, 315–317, 319–322, 324
Diffusion length, 315
Diffusion time, 320
Direct FET, 24, 39
Discontinuous conduction mode (DCM), 15, 33, 34, 38
Distributed power architecture (DPA), 15, 16
DMOS, 287
Domain moments, 208, 347, 349
Domain wall, 208, 347, 349, 351
DPA. *See* Distributed power architecture
D-Pak, 39, 41, 76–78
D^2-Pak, 39, 78
Drain current, 70, 71, 73, 82, 83, 85, 88, 102, 103, 109, 115–117, 124, 128, 134, 140, 142–144, 147, 148, 152, 156, 157, 166, 170, 173, 182–185, 190, 202, 203, 205, 264, 285–287, 290–292, 295–297, 301, 302, 304, 305, 307, 309, 315, 324, 332, 343, 359
Drain inductance, 76–78, 88, 102, 103, 116, 142, 148, 152, 170, 190, 264, 308
Drain-source voltage, 137, 138, 142–144, 147–150, 155–157, 164, 166, 168, 170–172, 174, 175, 181, 184, 190, 202, 203, 286, 290, 291, 304, 359
Drift region, 19–20, 304, 315–318, 320
DrMOS, 13, 23, 40, 44, 45, 113, 153, 235

E
Eddy current loss, 27–29, 208, 335, 347, 348, 351, 353, 355
Eddy currents, 77, 197, 206, 335, 345, 347, 351, 353, 355
  in conductors, 208, 345
Effective active chip area, 70
Effective die area, 229
Electrolytic capacitors, 31, 41, 44, 216, 219, 222, 225, 226, 236, 249, 267, 270, 274
Electron concentration, 292–298
Empirical model, 46–48, 68, 69, 71, 317, 320, 324
Environmental conditions, 10–12
Equivalent series inductance (ESL), 27, 30, 31, 34, 78, 94–96, 102, 109, 214, 216–227, 262, 263, 267, 268, 270, 274, 335–337, 340, 342, 345
Equivalent series resistance (ESR), 26, 30, 31, 33–36, 94, 95, 112, 208, 209, 214, 216, 217, 219, 221–227, 262, 267, 268, 335–337, 340, 342, 362, 365, 366, 369, 372
  frequency dependence, 78, 345
ESL. *See* Equivalent series inductance
ESR. *See* Equivalent series resistance
Excess Eddy current losses, 27, 335, 351–352, 355
Excess of holes, 316

F
Feedback, 32–35, 38, 116, 117, 137, 159, 170, 172, 177, 190, 264, 308
Ferrites, 27–30, 44, 208, 335, 347, 348, 350, 353
Ferromagnets, 345, 347, 351
Figure of merit (FoM), 20–22, 50, 51, 130, 197, 213, 228–231, 233, 247, 249–251, 254, 257, 258, 261, 283, 362, 369
First quadrant operation, 167
Forward body diode, 80, 116, 285, 287, 290–291, 296, 297, 304, 307
Forward recovery, 71
Fourier expansion, 206, 214–215

G
Gate bounce loss, 170, 176–179, 333
Gate bounce shoot-through, 106, 113, 135, 137, 155, 156, 169, 170, 172, 173, 176–179, 231, 282
Gate bounce susceptibility, 174, 175, 179, 180, 232, 251, 253, 254, 263, 280, 282

Gate busbar, 23, 74, 79
Gate charge loss, 24, 39, 122, 176, 199–201, 231, 332, 357, 360, 362, 369
Gate charging, 18, 22, 25, 39, 118–120, 198, 201, 251, 264, 302, 332, 357, 360, 362, 369
Gate current, 72, 79, 85, 86, 88, 91, 102, 126, 134, 142, 144, 145, 148–151, 153, 170, 191, 202–205, 211, 212, 229, 256, 263–265, 332, 333
Gate drive loss, 119, 129, 130, 144, 145, 149, 152, 153, 233, 259, 276, 332, 357, 360, 361, 369, 370, 372
Gate driver, 22–25, 32, 37, 54, 60, 90–94, 97, 109, 114, 122–124, 134, 136, 139, 145, 147, 152, 171, 190, 207, 210, 213, 228–235, 240, 246, 253, 256–260, 262–266, 275, 280, 357–373
Gate inductance, 23, 25, 114, 128, 170, 173, 178, 264, 266, 308, 357, 361
Gate-source voltage, 126, 137, 138, 140, 141, 171, 180, 190

H

Half-bridge charging (HBC), 118, 119, 198, 199, 227, 332
Half-bridge loop inductance, 22, 26, 40, 103, 117, 119, 121, 130, 134, 137, 141, 142, 144, 145, 148–150, 153, 163, 167, 198, 199, 209, 226, 232, 252, 262, 281
Hard-switching loss, 144, 145, 148, 149, 201–203, 211, 235, 252, 275, 276, 331
Hard-switching phenomena, 150
Harmonic composition, 214
Harmonic domain, 339
HBC. *See* Half-bridge charging
Heatsink, 10, 16, 26, 27, 41–46, 237, 239, 248–250, 269–270, 272–274, 279
Heavy load, 4, 231, 239, 246, 262, 267, 268, 276, 281
HEMT. *See* High electron mobility transistor
High electron mobility transistor (HEMT), 20, 261
High switching frequency, 17, 19, 22, 24, 25, 27, 28, 46–50, 75, 159, 208, 214, 217, 225, 227, 263, 275, 279, 335, 345, 348, 357, 375
High switching frequency operation, 20, 27, 29, 49, 166, 241, 257, 279, 281, 345, 348, 375
Hysteresis model, 208, 348–351
Hysteretic controller, 34
Hysteretic losses, 27, 29, 335, 347–351, 355

I

IBA. *See* Intermediate bus architecture
Idle losses, 94
Impedance analyzer, 75, 76, 83, 84, 86, 95
Induced voltage, 5, 102, 116–117, 119, 137–138, 144, 170, 176, 178, 180, 216, 217, 219, 220, 222, 332
Inductive reverse recovery, 75, 88, 90, 173, 180, 314, 316, 317, 321, 323
Input voltage, 10, 13, 14, 27, 101, 103, 104, 108, 109, 117, 119, 137, 156, 161, 227–229, 239, 275, 276, 281, 307, 359, 361
Integrated power module (IPM), 40, 192, 195, 198, 201, 213, 231–236, 239, 240, 246–248, 251, 252, 254, 255, 259, 260, 265, 266, 269, 270, 272, 279–282, 375, 376
Inter-electrode capacitance, 75, 82–87, 308
Interleaving, 16, 30, 37, 41, 44, 209, 213–216, 224, 225, 227, 241, 268, 269, 276, 279
Intermediate bus architecture (IBA), 16
IPM. *See* Integrated power module
Irreversable magnetization, 349, 350

J

Jiles-Atherton, 335, 348–350
Junction temperature, 81, 111, 246, 286

L

Langevin expression, 349, 350
Laptop, 7, 9, 10, 31, 44, 45, 113, 114, 123, 124, 213, 239–243, 246, 257, 263, 264, 275–277, 281
Lateral power MOSFET technology, 18
Lauritzen, 71, 87
Layout arrangement, 77, 240, 269–274, 307, 336
Layout design, 26, 74, 96, 111, 252, 259, 265, 336
Leadframe, 39, 78, 197, 206, 335, 343–347
LFPak, 21, 39, 43, 78, 101, 114, 122, 124, 240, 275, 277, 335, 343–347, 375
Light load, 4, 6, 11, 17, 30, 37, 38, 40, 218, 221, 232, 233, 239, 241, 268, 269, 280
Limit, 4, 5, 11, 14, 17, 19, 24, 26, 27, 29, 30, 39–41, 47, 310, 313, 314, 355, 360, 367, 373
Load current, 4, 5, 10, 14, 16, 17, 24, 33, 37,38, 48, 98, 100, 101, 103, 104, 107, 109, 112, 113, 118–120, 124, 149, 169, 182, 188, 192, 198,

201–208, 211, 212, 215–221, 224, 227, 232, 233, 239, 242, 254–256, 267–270, 281, 314, 331–332, 352, 354, 355, 375–376
Load line, 4, 5, 8, 9, 11, 12, 32–35, 215, 224, 225
Load line transient, 217–223
Look-up tables, 46, 47, 68, 70, 72, 73
Loop delays, 217
Loss breakdown, 54, 68, 112–123, 129, 131, 187, 212, 234, 248, 255–257, 275, 276, 281, 330, 333, 347, 355
Loss mechanism, 14, 45, 50, 51, 54, 68, 112–114, 117–121, 129, 130, 159, 162, 166, 169, 173, 192, 198, 208, 211, 231, 255, 279, 282, 283, 327, 331–334, 355
Loss model, 50–52, 188, 197–213, 226, 228, 234, 348–352, 359
Lumped elements, 47, 67, 69
Lumped model, 90, 96, 301, 313–324

M
Magnetic flux saturation, 27–29
Magnetic loss, 29, 75, 208, 281, 335–355
Magnetic materials, 27–29, 208, 237, 352, 355
Magnetization, 28, 348–351
Maximum voltage overshoot, 5–7, 9, 149, 162
MCM. *See* Multichip module
Measurement instrument, 83, 84
Mechanical guidelines, 11, 12
Microprocessor power supply, 9–48
Miller plateau, 115, 191, 201, 205, 263, 308
Minority carriers, 82, 292, 301
MLCC. *See* Multilayer ceramic capacitors
Model data, 75–90
Model parameters, 54, 67, 70, 75, 78, 81, 82, 88–90, 122, 324
Modulation techniques, 34, 35, 37
MOSFET, 13, 14, 17–27, 36, 39–43, 45–48, 52, 54, 67–131, 133–135, 137–141, 146, 147, 149, 150, 159–162, 165, 168, 169, 173, 175–181, 183, 189, 190, 198–207, 209, 210, 228–235, 240, 246–261, 263–266, 268, 269, 275–277, 279–282, 285–298, 301–311, 313–317, 320, 324, 330, 332–335, 343–345, 358–363, 366, 369, 372, 373, 375, 385
Motherboard, 10, 12, 31, 41–45, 269
Multichip module (MCM), 40, 44, 54, 113, 128–131, 262, 321
Multilayer ceramic capacitors (MLCC), 27, 31, 40, 44, 270
Multimode switching, 32, 37
Multiphase operation, 40, 376
Multiphase regulation, 35–37
Multiphysics, 21, 47

N
Nanocrystallines, 28
n-channel enhancement-mode, 17, 22
Nonlinear behavior, 281, 282, 335
Nonlinear capacitance, 71, 73, 138, 139, 146, 160–162, 174, 199, 201
Nonlinear functions, 73
Nonlinear hysteretic control, 34, 213, 217, 269, 280
Nonlinear impedance network, 94
Nonlinear networks, 133
Nonlinear parasitic elements, 281
Nonlinear transient, 191
Number of phases, 35, 41, 42, 48, 49, 54, 213, 215, 217, 225, 226, 232, 235, 236, 238–242, 247–249, 251, 256, 267, 268, 276, 283
Numerical methods, 21, 47, 133, 147, 184, 204, 224

O
Ohmic intervals, 116
Optimization guidelines, 245, 280
OS-CON, 31, 42, 44
Output capacitance, 37, 85, 87, 94, 112, 117–119, 122, 137, 141, 142, 148, 153, 160, 161, 167, 174, 183–185, 187, 198, 199, 208, 209, 218, 221, 257, 263, 281, 282, 304, 305, 315, 332, 362
Output capacitance current, 121, 144, 332
Output characteristics, 4, 82, 83, 138–141, 285–298, 301, 305, 311
Output charge, 92, 143, 251, 282
Output coil, 99–101, 103, 112, 213, 222, 225, 237, 238, 241, 242, 247, 256, 268, 330
Output current, 30, 32, 33, 35, 41, 99, 111, 112, 116, 118, 121, 194, 201, 215, 216, 219–220, 280, 307, 308, 321, 323, 330, 331, 334, 359
Output filter, 5–7, 14, 27–31, 34, 44, 48, 68, 94–95, 97, 114, 123, 124, 128, 208, 209, 213–226, 232, 236, 249–251, 262, 267–270, 274, 276, 280, 335, 343
Output indicators, 11
Output inductor, 27, 30, 33, 36, 77, 90, 95, 98, 100, 102, 103, 112, 118, 144,

189, 192, 197, 205, 208, 215–224, 227, 236, 238, 240, 248, 249, 266, 277
Output load, 119, 330
Output voltage, 1, 4, 9, 10, 14, 30–34, 102, 103, 195, 214–219, 221, 267, 268, 308, 359

P
Package impedance, 68, 75–80, 88, 348
Package inductance, 23, 78, 88, 280
Package resistance, 81, 128, 197, 198, 206, 229, 287, 343
Packaging technology, 240, 246
Parallel devices, 240, 275
Parasitic capacitance, 134, 159, 259, 360
Parasitic charge, 21, 23, 25, 207, 208, 251, 253, 254, 257, 357
Parasitic elements, 15, 23, 24, 30, 31, 39, 40, 68, 69, 74, 75, 78, 83, 86, 88, 90, 95, 96, 98, 118, 123, 147, 214, 220, 259, 281, 360, 362
Parasitic inductance, 5, 22, 23, 40, 50, 75, 77–79, 83, 91, 94, 95, 228, 240, 252, 263, 266, 280, 362, 375
Parasitic resistance, 25, 74, 119, 159, 266, 309, 357, 362, 366
PCB board arrangement, 44, 240, 269
PCB layout, 77, 78, 90, 95–98, 231, 240, 269, 283, 335–343, 375
PDN. *See* Power delivery network
Permalloys, 28
PFM. *See* Pulse frequency modulation
Phase shedding, 17, 30, 32, 37, 49, 239, 241, 242, 268–270, 276, 280
Piecewise linear analytical (PLA), 51, 133–195
Piecewise linear analytical (PLA) model, 50, 51, 143, 150, 158, 166, 181, 188, 191–195, 197, 201, 210–212, 232, 233
Pinning mechanism, 349
PIP212-12M, 128, 192, 212, 232–236, 247, 252–255, 259, 263, 265, 266, 270, 276, 375, 376
PLA. *See* Piecewise linear analytical
p-n junction, 166, 304
Point-of-load (PoL), 15–17, 32, 254, 321, 375–376, 382, 385
Power beads, 237
Power cube, 27, 29, 30, 42, 44, 237, 266
Power delivery guidelines, 12
Power delivery network (PDN), 4, 6
Power density, 1, 2, 9, 13, 14, 16, 17, 20, 27–31, 39, 44, 48, 49, 54, 213, 214, 226, 235, 238–242, 245, 247–251, 254–256, 269, 276, 277, 279, 336, 337, 339–342, 353, 354
Power inductors, 30, 345, 348, 352
Power loss, 15, 17, 21, 22, 29, 30, 37, 38, 48, 49, 51, 67, 101, 104, 109, 112, 113, 119, 120, 122, 124, 128–130, 137, 159, 162, 185, 194, 195, 197–212, 225, 234–236, 239, 248, 251, 253, 256, 258, 267, 268, 275, 281, 285, 307, 309–310, 327, 330–333, 335, 339–341, 351, 352, 355, 358, 360–362, 364, 369–373
Power MOSFET model, 45–48, 68–90, 102
Power-out, 10–12
Power supply-in-package (PSiP), 15, 40, 262
Power supply-on-chip (PwrSoC), 15, 40, 262
Prototype board, 90, 101, 375–377, 383
PSiP. *See* Power supply-in-package
Pulse frequency modulation
  adaptive constant ON time, 35
  constant OFF time, 35
  constant ON time, 34, 35
Pulse frequency modulation (PFM), 15, 17, 34, 35, 37, 239
Pulse width modulation (PWM), 15, 34–37, 68, 91, 97–100, 215
PwrSoC. *See* Power supply-on-chip

Q
QSW. *See* Quasi-square wave
Quality factor, 185, 357–373
Quasi-neutral, 85, 318, 320
Quasi-plateau, 308
Quasi-square wave (QSW), 15, 29
Quasi-static, 77, 320, 335–336, 349
Quasi-uniform, 339

R
Recombination, 301, 313, 318
Recovery charge, 168, 316, 323
Reduced surface field, 19–20, 260, 261, 263, 269, 270
Resistive reverse recovery, 88, 303, 306
Resonant frequency, 79, 95, 157, 170, 182
Resonant gate driver (RGD), 24, 25, 145, 260, 265, 280, 357–373
Reverse recovery (RR), 38, 68, 70, 71, 75, 87–90, 104, 105, 113, 115–126, 128–131, 134, 135, 137, 139, 155, 156, 159, 162, 166–170, 172–174, 176–180, 192, 198, 210, 231, 240, 282, 285, 301–311, 313–324, 330, 333, 375

Reverse recovery (RR) (*cont.*)
loss, 38, 167, 282, 285
time, 167–169, 172, 321, 323, 333
Reverse transfer capacitance, 126
RGD. *See* Resonant gate driver
Ringing transition, 155, 180–190
Ringing voltage, 124, 168, 227, 229, 264

S

Shoot-through, 38, 92, 104, 106, 112, 113, 117, 120, 125, 126, 129, 130, 135, 137, 155, 156, 169, 170, 172–174, 177–179, 231, 280, 282
Shunt resistor, 96, 102, 103, 109, 111
SiP. *See* System in package
Si Steels, 28
Skin depth, 197, 209, 335, 337, 338
Skin effect, 76–78, 208, 209, 266, 267, 336, 339–343
Slew rate (SR), 5, 6, 8–10, 12, 218–220, 224–228, 267, 268
SMT. *See* Surface-mount technology
Snubbed hard-switching (SHS), 118–121, 123, 131, 331
Snubber turn-off, 118, 122, 148, 257, 258
Snubber turn-on, 117, 145, 152, 153, 258
SoC. *See* System on chip
SOIC, 39
Source inductance, 24, 78, 88, 114, 116, 117, 123, 126, 128, 144, 147, 152, 159, 169, 170, 172, 177, 179, 190, 264, 266, 308, 343, 345
S-parameter, 75, 76, 78, 79
Specific ON resistance, 19, 251, 359
SPICE model, 50, 191, 194, 306, 307
Spurious turn-on, 23, 120, 125, 169, 172, 264, 280, 282, 310, 333
SR. *See* Slew rate
SRBC. *See* Synchronous rectifier buck converter
Steady-state output voltage, 4, 30, 214, 219
Storage node, 313, 317, 319
Substrate resistance, 69, 74, 75, 82
Subthreshold, 82, 125, 127, 282, 285, 287, 290, 292–298, 302, 307, 311
Subthreshold electron concentration, 293–298
Supply voltage, 2–4, 8, 9, 11, 13, 109, 114, 119, 159, 167, 280
Surface-mount technology (SMT), 27, 30, 31, 39, 83
Switched node falling edge transition, 103, 147–155, 194
Switched node leading edge transition, 143–147, 150–155, 166, 193
Switched-node voltage, 137, 167, 169, 215, 257
Switching behavior, 49, 54, 67–131, 135, 141, 146, 184, 283
Switching loss, 3, 14, 15, 22–24, 37, 38, 45, 49, 51, 80, 82, 92, 95, 114, 118–120, 122–128, 130, 145, 149–151, 153, 159, 163, 165, 167, 176, 190, 201, 202, 229, 233, 235, 239, 257, 258, 264, 275, 281–283, 285, 311
Synchronous rectification, 32, 218
Synchronous rectifier buck converter (SRBC), 13–17, 22, 26, 34, 37, 40, 41, 48, 50, 51, 54, 67, 90, 95, 97, 98, 105–111, 122–124, 134, 135, 144, 163, 192, 210, 279, 282
System architecture, 1, 15–17
System in package (SiP), 39, 40, 153
System on chip (SoC), 39, 40

T

Thermal management, 2, 39
Thermal stress, 35
Third quadrant, 68, 70, 81–83, 87, 117, 125, 138, 139, 141, 181, 285–289, 301–302, 305–307, 310, 311, 359
Third quadrant operation, 70, 128, 182, 285, 310
Threshold voltage, 23, 70, 117, 124, 126, 138, 140–142, 180, 286, 290–291, 301–302, 306, 310
Toroids, 27, 29, 30, 41
Transconductance, 134, 138, 140, 142, 146, 173, 174, 191, 203
Transient behavior, 122, 124, 190, 213, 233, 285
Transient skin effect, 76–78, 208, 209, 266, 267, 339, 340–343
Transient waveform, 218
Transmission coefficients, 76, 79, 80, 94, 95
Transmission line, 76, 317–319, 322, 324
Transport equation, 316
Trapezoidal current waveform, 123, 340
Trench cell, 18, 291–298, 302, 303, 305, 306, 321

U

Underdamped condition, 171, 172, 180, 182

V

V^2 control, 33, 34
Vector network analyzer (VNA), 75, 76, 78, 94–95
Vertical power MOSFET technology, 71

Vertical trench power MOSFET, 18
VID. *See* Voltage identification digital
Virtual design loop, 52, 245, 282
VNA. *See* Vector network analyzer
Voltage hard-switching, 115
Voltage identification digital (VID), 11–13
Voltage regulator down (VRD), 10, 11, 16, 31, 32, 41–45, 226
  guidelines, 226
Voltage regulator module (VRM), 10–12, 16, 31, 32, 44, 46, 226
Voltage regulators (VR), 9–13, 15, 17, 31–33, 38, 48, 50–54, 83, 84, 113, 153, 208, 213, 214, 218, 220, 225–227, 235–242, 245–251, 253–258, 260, 262, 267–274, 276, 279–283, 386
  guidelines, 12–13, 247
  layout arrangement, 269–274, 336
Voltage regulator specifications, 9–13
Voltage stress, 117, 118, 121, 149, 151, 152, 154, 155, 161, 162, 189, 204, 205, 276, 281
VR. *See* Voltage Regulator
VRD. *See* Voltage regulator down
VRM. *See* Voltage regulator module

W

Weight of loss contribution, 7, 327, 331, 332
Worst-case, 7, 126, 148, 154–155, 161, 163, 169, 174, 176, 180, 185, 188, 204, 214, 217, 218, 221, 225, 226, 232, 235, 239, 246, 268, 282, 322

Z

Zero current switching (ZCS), 14, 92
Zero voltage switching (ZVS), 14–15, 23, 118, 190, 241, 268–269, 281, 282, 358, 359, 361