Appendix A
Current State-of-the-Art in Literature

This appendix provides an overview of the current state-of-the-art in literature on ultra-low-voltage digital circuit design in CMOS technologies. A subset of papers will be discussed.

The criteria for selection are the following:

- It must consist of a substantial digital circuit which has been fabricated and measured. Very simple digital circuits, such as a single logic gate or a ring oscillator, have been discarded. The implementations of the papers are included in the table, and range from adders and multipliers to full DSPs and microcontrollers.
- The designs must be fabricated in bulk CMOS technologies.
- The designs must be able to operate at ultra-low supply voltages. The requirement which has been used for this appendix is that they should be able to function at supply voltages below 500 mV.

Table A.1 contains all relevant details of the 41 selected papers and their measured operating points at supply voltages equal to or below 500 mV:

- The year in which the paper was published.
- Paper reference.
- A short description of the design.
- In which CMOS technology the design has been fabricated.
- Whether body biasing was employed or not.
- The following measured operating points:
  - At the minimal functional supply voltage $V_{\mathrm{dd,min}}$.
  - At the MEP (if provided).
  - Any other operating points (if provided).

All reported operating points were measured at room temperatures, except for the ones of papers 12, 21 and 22 (indicated by *), which were measured at 50 °C.

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Table A.1 Overview of current state-of-the-art in literature on ultra-low-voltage digital circuit design

#	Year	Publication	What?	CMOS tech.	Body bias	Measured operating points		
						$V_{dd,min}$	MEP	Other
1	2002	[27, 45]	MAC	140 nm	✓	175 mV, 166 kHz	–	–
2	2003/2001	[31, 46]	8 × 8 array multiplier	0.35 µm	✓	300 mV	–	–
3	2004/2005	[54, 55]	16-bit 1024-pt FFT	0.18 µm	✗	180 mV, 164 Hz	350 mV, 9.6 kHz	–
4	2005	[56]	32-bit RISC core	0.25 µm	✓	400 mV, 2 MHz	–	500 mV, 5 MHz
5	2005/2006	[6, 7]	32-bit Kogge-Stone adder	90 nm	✗	250 mV, 7 kHz	330 mV, 50 kHz	500 mV, 2.4 MHz
6	2006/2009	[59, 60]	Sensor processor	130 nm	✗	200 mV	360 mV, 833 kHz	–
7	2007	[57]	32-bit RISC core	0.18 µm	✓	230 mV, 375 kHz	–	350 mV, 5 MHz /500 mV,16 MHz
8	2007	[53]	Baseband processor	90 nm	✗	400 mV, 25 MHz	400 mV, 25 MHz	–
9	2007/2008	[16, 17]	Sensor processor	130 nm	✓	160 mV, 710 Hz	350 mV, 354 kHz	–
10	2007	[21]	8 × 8 FIR	130 nm	✓	85 mV, 240 Hz	–	200 mV, 12 kHz / 270 mV, 98 kHz
11	2008	[22]	DSP	90 nm	✗	440 mV	450 mV, 4 MHz	500 mV, 5 MHz
12*	2008/2009	[28, 29]	Motion estimation accelerator	65 nm	✗	230 mV, 4.3 MHz	320 mV, 23 MHz	–
13	2008/2009	[35, 36]	Microcontroller	65 nm	✗	300 mV, 8.7 kHz	500 mV, 434 kHz	–
14	2008/2009	[18, 51]	Sensor processor	0.18 µm	✗	460 mV	500 mV, 106 kHz	–
15	2009	[26]	Microcontroller	130 nm	✗	240 mV	280 mV, 475 kHz	–
16	2009/2010	[47, 48]	JPEG encoder	65 nm	✓	400 mV, 2.5 MHz	400 mV, 2.5 MHz	450 mV, 4.5 MHz /500 mV, 10 MHz
17	2009/2010	[42, 43]	14-tap 8-bit FIR	130 nm	✗	160 mV, 5 MHz	270 mV, 20 MHz	300 mV, 80 MHz / 360 mV, 187 MHz
18	2010	[12]	Frame decoder	40 nm	✗	330 mV, 600 kHz	330 mV, 600 kHz	–
19	2010	[9]	8-tap FIR	90 nm	✗	200 mV	290 mV, 148 kHz	–
20	2010	[10]	Sensor platform	0.18 µm	✗	350 mV	400 mV, 73 kHz	500 mV, 1 MHz

Table A.1 (continued)

#	Year	Publication	What?	CMOS tech.	Body bias	Measured operating points		
						$V_{dd,min}$	MEP	Other
21*	2010	[1]	CLB array	32 nm	✗	260 mV, 27 MHz	340 mV	–
22*	2010	[30]	SIMD accelerator engine	45 nm	✗	230 mV, 8.8 MHz	300 mV, 33 MHz	–
23	2010	[8, 50]	FPGA	90 nm	✗	200 mV	–	–
24	2010/2012	[2, 49]	Cardiac event detector	65 nm	✗	250 mV, 1 kHz	320 mV, 20 kHz	–
25	2011/2012	[38, 39]	8 × 8 multiplier	130 nm	✗	84 mV, 15.2 kHz	260 mV, 544.8 kHz	–
26	2011	[13]	Frame decoder	40 nm	✓	240 mV, 1 MHz	340 mV, 10 MHz	–
27	2011	[3, 20]	Biomedical signal processor	90 nm	✗	400 mV, 1 MHz	400 mV, 1 MHz	–
28	2011	[19]	AES coprocessor	65 nm	✗	193 mV	300 mV, 80 kHz	400 mV, 890 kHz
29	2011/2012	[15, 23]	DSP SoC	28 nm	✗	340 mV, 3.6 MHz	500 mV, 43.4 MHz	–
30	2011/2012	[25, 52]	16-bit 1024-pt FFT	65nm	✗	260 mV	270 mV, 30 MHz	300 mV, 41 MHz
31	2012	[33]	30-tap FIR	130 nm	✗	300 mV, 8 kHz	350 mV, 29 kHz	–
32	2012	[58]	FFT	65nm	✗	200 mV	450 mV, 20 MHz	–
33	2012	[37]	Neural signal processor	65 nm	✗	250 mV, 20 kHz	–	–
34	2012	[44]	8-bit microprocessor	65 nm	✗	300 mV, 2.95 kHz	300 mV, 2.95 kHz	400 mV, 37.2 kHz
35	2012	[24]	IA-32 processor	32 nm	✗	280 mV, 3 MHz	450 mV	500 mV, 100 MHz
36	2012/2013	[4, 5]	Microcontroller	65 nm	✗	265 mV	400 mV, 25 MHz	–
37	2012/2013	[40, 41]	32-bit RISC processor	65 nm	✗	200 mV, 10 kHz	325 mV, 133 kHz	500 mV, 4.2 MHz
38	2013	[11]	32-bit RISC core	130 nm	✓	300 mV, 5 MHz	300 mV, 5 MHz	500 mV, 25 MHz
39	2013	[34]	SoC for ExG	40 nm	✓	400 mV, 1 MHz	400 mV, 1 MHz	–
40	2014	[14]	32-bit processor	90 nm	✗	250 mV	–	–
41	2014	[32]	16-bit microprocessor	65 nm	✗	303 mV, 10 MHz	–	412 mV, 49 MHz

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Index

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