

References

1. Evolution of cell phone to smartphone. <https://blog.lookout.com/blog/2011/02/03/evolution-of-cell-phone-to-smartphone/>. Accessed 20 Feb 2015.
2. Will LTE slap WiMAX and become the next-gen technology? <http://www.broadbandwatcher.co.uk/will-lte-slap-wimax-and-become-the-next-gen-technology-566/>. Accessed 15 Mar 2013.
3. Wirelesshd specifications. <http://www.wirelesshd.org>. Accessed 20 Feb 2015.
4. Namgoong W. A channelized digital ultrawideband receiver. *IEEE Trans Wireless Commun.* 2003;2(3):502–10.
5. Mitola J. The software radio architecture. *IEEE Commun Mag.* 1995; 33(5):26–38.
6. Bagheri R, Mirzaei A, Chehrazi S, Heidari ME, Lee M, Mikhemar M, Tang W, Abidi AA. A 800-MHz-6-GHz software-defined wireless receiver in 90-nm CMOS. *IEEE J Solid-State Circuits.* 2006;41(12):2860–76.
7. Razavi B. *RF microelectronics*. New Jersey: Prentice Hall; 2012.
8. Chen PW, Lin TY, Kei L-W, Yu R, Tsai M-D, Yeh C-W, Lee Y-B, Tzang B, Chen Y-H, Huang S-J, Lin Y-H, Dehng G-K. A 0.13 μm CMOS quad-band GSM/GPRS/EDGE RF transceiver using a low-noise fractional-N frequency synthesizer and direct-conversion architecture. *IEEE J Solid-State Circuits.* 2009;44(5):1454–63.
9. Siligaris A, Richard O, Martineau B, Mounet C, Chaix F, Ferragut R, Dehos C, Lanteri J, Dussot L, Yamamoto SD, Pilard R, Busson P, Catheline A, Belot D, Vincent P. A 65-nm CMOS fully integrated transceiver module for 60-GHz wireless HD applications. *IEEE J Solid-State Circuits.* 2011;46(12):3005–17.
10. Murmann B. ADC performance survey 1997–2011. <http://www.stanford.edu/~murmam/adcsurvey.html>. Accessed June 2011.
11. Medi A, Namgoong W. A high data-rate energy-efficient interference-tolerant fully integrated CMOS frequency channelized UWB transceiver for impulse radio. *IEEE J Solid-State Circuits.* 2008;43(4):974–80.
12. Andreani P, Bonfanti A, Romano L, Samori C. Analysis and design of a 1.8-GHz CMOS LC quadrature VCO. *IEEE J Solid-State Circuits.* 2002;37(12):1737–47.
13. Behbahani F, Kishigami Y, Leete J, Abidi AA. CMOS mixers and polyphase filters for large image rejection. *IEEE J Solid-State Circuits.* 2001;36(6):873–87.
14. Rofougaran A, Rael J, Rofougaran M, Abidi A. A 900MHz CMOS LC-oscillator with quadrature outputs. In: *International Solid-State Circuits Conference*, Feb. 1996, pp. 392–3.
15. Rofougaran A, Chang G, Rael JJ, Chang JYC, Rofougaran M, Chang PJ, Djafari M, Ku MK, Roth EW, Abidi AA, Samuelli H. A single chip 900-MHz spread-spectrum wireless transceivers in 1- μm CMOS —part I: architecture and transmitter design. *IEEE J Solid-State Circuits.* 1998;33(4):515–34.
16. Lanka NR, Patnaik SA, Harjani RA. Frequency-hopped quadrature frequency synthesizer in 0.13 μm technology. *IEEE J Solid-State Circuits.* 2011;46(9):2021–32.
17. Razavi B. Design of millimeter-wave CMOS radios: a tutorial. *IEEE J Solid-State Circuits.* 2009;56(1):4–16.

18. Hajimiri A, Lee TH. A general theory of phase noise in electrical oscillators. *IEEE J Solid-State Circuits*. 1998;33(2):179–94.
19. Razavi B. A study of injection locking and pulling in oscillators. *IEEE J Solid-State Circuits*. 2004;39(9):1415–24.
20. Huang D, Li W, Zhou J, Li N, Chen J. A frequency synthesizer with optimally coupled QVCO and harmonic-rejection SSBmixer for multi-standard wireless receiver. *IEEE J Solid-State Circuits*. 2011;46(6):1307–20.
21. Elbadry M, Harjani R. Quadrature frequency synthesis for Wideband wireless transceivers. PhD thesis, University of Minnesota, May 2014.
22. Valla M, Montagna G, Castello R, Tonietto R, Bietti I. A 72-mW CMOS 802.11a direct conversion front-end with 3.5-dB NF and 200-kHz $1/f$ noise corner. *IEEE J Solid-State Circuits*. 2005;40(4):970–7.
23. Vancorenland P, Steyaert MSJ. A 1.57-GHz fully integrated very low-phase-noise quadrature VCO. *IEEE J Solid-State Circuits*. 2002;37(5):653–6.
24. Yi X, Boon CC, Liu H, Lin JF, Lim WM. A 57.9-to-68.3 GHz 24.6 mW frequency synthesizer with in-phase injection-coupled QVCO in 65 nm CMOS technology. *IEEE J Solid-State Circuits*. 2014;49(2):347–59.
25. Gierkink SLJ, Laventino S, Frye RC, Samori C, Bocuzzi V. A low-phase-noise 5-GHz CMOS quadrature VCO using superharmonic coupling. *IEEE J Solid-State Circuits*. 2003;38(7):1148–54.
26. Chamas IR, Raman S. Analysis and design of a CMOS phase-tunable injection-coupled LC quadrature VCO. (PTIC-QVCO). *IEEE J Solid-State Circuits*. 2009;44(3):784–96.
27. Guermandi D, Tortori P, Franchi E, Gnudi A. A 0.83-2.5-GHz continuously tunable quadrature VCO. *IEEE J Solid-State Circuits*. 2005;40(12):2620–27.
28. Andreani P, Wang X. On the phase-noise and phase-error performances of multiphase LC CMOS VCOs. *IEEE J Solid-State Circuits*. 2004;39(11):1883–93.
29. Kim HR, C YC, S MOh, Yang MS, and SGLee. A very low-power quadrature VCO with back-gate coupling. *IEEE J Solid-State Circuits*. 2004;39(6):952–5.
30. Ng AWL, Luong HC. A 1-V 17-GHz 5-mW CMOS quadrature VCO based on transformer coupling. *IEEE J Solid-State Circuits*. 2007;42(9):1933–41.
31. Decanis U, Ghilioni A, Monaco E, Mazzanti A, Svelto F. A low-noise quadrature VCO based on magnetically coupled resonators and a wideband frequency divider at millimeter waves. *IEEE J Solid-State Circuits*. 2011;46(12):2943–55.
32. Hegazi E, Sjolund H, Abidi AA. A filtering technique to lower LC oscillator phase noise. *IEEE J Solid-State Circuits*. 2001;36(12):1921–30.
33. Ham D, Hajimiri A. Concepts and methods in optimization of integrated LC VCOs. *IEEE J Solid-State Circuits*. 2001;36(6):896–09.
34. Wu Q, Quach T, Mattamana A, Elabd S, Dooley SR, McCue JJ, Orlando PL, Creech GL, Khalil W. A 10 mW 37.8 GHz current-redistribution BiCMOS VCO with an average FOMT of -193.5 dBc/Hz. In *IEEE International Solid State Circuits Conference*, pp 150–51, Feb. 2013.
35. Cusmai G, Repossi M, Albasini G, Mazzanti A, Svelto F. A magnetically tuned quadrature oscillator. *IEEE J Solid-State Circuits*. 2007;42(12):2870–7.
36. Hong-Yeh C, Yuan-Ta C. K-band CMOS differential and quadrature voltage-controlled oscillators for low phase-noise and low-power applications. *IEEE Trans Microwave Theory Tech*. 2012;60(1):46–59.
37. Wireless LAN at 60 GHz - IEEE 802.11ad Explained. Technical report, Agilent Technologies.
38. Wells J. Faster than fiber: the future of multi-G/s wireless. *IEEE Microwave Mag*. 2009;10(3):104–12.
39. Hasch J, Topak E, Schnabel R, Zwick T, Weigel R, Waldschmidt C. Millimeter-wave technology for automotive radar sensors in the 77 GHz frequency band. *IEEE Trans Microwave Theory Tech*. 2012;60(3):845–60.

40. Tabesh M, Chen J, Marcu C, Kong L, Kang S, Niknejad AM, Alon E. A 65 nm CMOS 4-element sub-34 mw/element 60 GHz phased-array transceiver. *IEEE J of Solid State Circuits*. 2011;46(12):3018–32.
41. Vidojkovic V, Mangraviti G, Khalaf K, Szortyka V, Vaesen K, Thillo W Van, Parvais B, Libois M, Thijs S, Long JR, Soens C, Wambacq P. A low-power 57-to-66 GHz transceiver in 40 nm LP CMOS with -17 dB EVM at 7 Gb/s. In *IEEE International Solid State Circuits Conference*, pp. 268–70, Feb. 2012.
42. Okada K, Matsushita K, Bunsen K, Murakami R, Musa A, Sato T, Asada H, Takayama N, Li N, Ito S, Chaivipas W, Minami R, Matsuzawa A. A 60 GHz 16QAM/8PSK/QPSK/BPSK direct-conversion transceiver for IEEE 802.15.3c. In *IEEE International Solid-State Circuits Conference*, pp. 160–2, Feb. 2011.
43. Kim C, Park P, Kim D-Y, Park K-H, Park M, Cho M-K, Lee SJ, Kim J-G, Eo YS, Park J, Baek D, Oh J-T, Hong S, Yu H-K. A CMOS centric 77 GHz automotive radar architecture. In *IEEE Radio Frequency Integrated Circuits symposium*, pp. 131–4, Jun. 2012.
44. Marcu C, Chowdhury D, Thakkar C, Park J-D, Kong L-K, Tabesh M, Wang Y, Afshar B, Gupta A, Arbabian A, Gambini S, Zamani R, Alon E, Niknejad AM. A 90 nm CMOS low-power 60 GHz transceiver with integrated baseband circuitry. *IEEE J Solid State Circuits*. 2009;44(12):3434–47.
45. Chan WL, Long JR. A 60-GHz band 2×2 phased-array transmitter in 65-nm CMOS. *IEEE J Solid State Circuits*. 2010;45(12):2682–95.
46. Scheir K, Bronckers S, Borremans J, Wambacq P, Rolain Y. A 52 GHz phased-array receiver front-end in 90 nm digital CMOS. *IEEE J Solid State Circuits*. 2008;43(12):2651–59.
47. Scheir K, Vandersteen G, Rolain Y, Wambacq P. A 57-to-66 GHz quadrature PLL in 45 nm digital CMOS. In *IEEE International Solid State Circuits Conference*, pp 494–5, 2009.
48. Wu L, Luong HC. A 49-to-62 GHz CMOS quadrature VCO with bimodal enhanced magnetic tuning. In *IEEE European Solid State Circuits Conference*, pp. 297–300, Sep. 2012.
49. Mazzanti A, Andreani P. Class-C harmonic CMOS VCOs, with a general result on phase noise. *IEEE J Solid State Circuits*. 2008;43(12):2716–29.
50. Integrand Software, Inc. EMX user's manual, 2010.
51. Sadhu B, Harjani R. Capacitor bank design for wide tuning range LC VCOs: 850 MHz-7.1 GHz (157%). In *Proceedings of 2010 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1975–78, 2010.
52. Shannon CE. Communication in the presence of noise. *Proc IRE*. 1949;37(1):10–21.
53. Goldsmith A. *Wireless communications*. Cambridge University Press, 2005.
54. Sai-Wang T, Socher E, Wong A, Yu W, Lan DV, Chang M-CF. Simultaneous sub-harmonic injection-locked mm-wave frequency generators for multi-band communications in CMOS. In *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 131–4, Jun. 2008.
55. Chan WL, Long JR. A 60-GHz band 2×2 phased-array transmitter in 65-nm CMOS. *IEEE J Solid-State Circuits*. 2010;45(12):2682–95.
56. Abdul-Latif MM, Elsayed MM, Sanchez-Sinencio E. A wideband millimeter-wave frequency synthesis architecture using multi-order harmonic-synthesis and variable N-push frequency multiplication. *IEEE J Solid-State Circuits*. 2011;46(6):1265–83.
57. Elbadry M, Sadhu B, Qiu J, Harjani R. Dual channel injection-locked quadrature LO generation for a 4 GHz instantaneous bandwidth receiver at 21GHz center frequency. *IEEE Trans Microwave Theory Tech*. 2013;61(3):1186–99.
58. Dal Toso S, Bevilacqua A, Tiebout M, Marsili S, Sandner C, Gerosa A, Neviani A. UWB fast-hopping frequency generation based on sub-harmonic injection locking. *IEEE J Solid-State Circuits*. 2008;43(12):2844–52.
59. Izad MM, Heng CH. A pulse shapping technique for spur suppression in injection-locked synthesizers. *IEEE J Solid-State Circuits*. 2012;47(3):652–64.
60. Lathi BP, Ding Z. *Modern digital and analog communication systems*. Oxford University Press, 2009.

61. Kalia S, Elbadry M, Sadhu B, Patnaik S, Qiu J, Harjani R. A simple, unified phase noise model for injection-locked oscillators. In IEEE Radio Frequency Integrated Circuits Symposium, pp. 1–4, Jun. 2011.
62. Mazzanti A, Svelto F, Andreani P. On the amplitude and phase errors of quadrature LC-tank CMOS oscillators. *IEEE J Solid-State Circuits*. 2006;41(6):1305–13.
63. Kinget P, Melville R, Long D, Gopinathan V. An injection-locking scheme for precision quadrature generation. *IEEE J Solid-State Circuits*. 2002;37(7):845–51.
64. Chan WL, Long JR. A 56–65 GHz injection-locked frequency tripler with quadrature outputs in 90-nm CMOS. *IEEE J Solid-State Circuits*. 2008;43(12):2739–46.
65. Sadhu B, Ferriss MA, Natarajan AS, Yaldez S, Plouchart JO, Rylyakov AV, Garcia AV, Parker BD, Babakhani A, Reynolds S, Xin L, Pileggi L, Harjani R, Tierno J, Friedman D. A linearized, low phase noise VCO based 25 GHz PLL with automatic biasing. *IEEE J Solid-State Circuits*, 2012.
66. Mazzanti A, Uggetti P, Svelto F. Analysis and design of injection-locked LC dividers for quadrature generation. *IEEE J Solid-State Circuits*. 2004;39(9):1425–33.
67. Tiebout M. A CMOS direct injection-locked oscillator topology as high-frequency low-power frequency divider. *IEEE J Solid-State Circuits*. 2004;39(7):1170–74.
68. Andreani P. A 2 GHz, 17 % tuning range quadrature CMOS VCO with high figure-of-merit and 0.6° phase error. In IEEE European Solid-State Circuits Conference, pp. 815–8, 2002.
69. Craninckx J, Staeyart MSJ. A 1.8-GHz low-phase-noise CMOS VCO using optimized hollow spiral inductors. *IEEE J Solid-State Circuits*. 1997;32(5):736–44.
70. Kuhn WB, Ibrahim NM. Analysis of current crowding effects in multiturn spiral inductors. *IEEE Trans Microwave Theory Tech*. Jan. 2001.;49(1):31–38.
71. R&S FSP spectrum analyzer—data sheet.