

Bibliography

- [1.1] L. Selmi, F. Venturi, E. Sangiorgi, and B. Ricco, "Three Dimensional Distribution of Latch-Up Current in Scaled CMOS Structures", Proc. ESSDERC (1987) 783.
- [1.2] P. Ciampolini, A. Gnudi, R. Guerrieri, M. Rudan and G. Baccarani, "Three-Dimensional Simulation of a Narrow-Width MOSFET", Proc. ESSDERC (1988) 413.
- [1.3] E.M. Buturla, P.E. Cottrell, B.M. Grossman and K.A. Salsburg, "Finite-Element Analysis of Semiconductor Devices: The FIELDAY Program", IBM J. Res. Develop. 25 (1981) 218.
- [1.4] K.A. Salsburg, P.E. Cottrell and E.M. Buturla, "FIELDAY - Finite Element Device Analysis", NATO Advanced Study Institute on Process and Device Simulation for MOS-VLSI Circuits, Sogesta-Urbino, Italy 1982.
- [1.5] W.P. Nobel and P.E. Cottrell, "Narrow Channel Effects in Insulated Gate Field Effect Transistors", IEDM Tech. Dig. (1976).
- [1.6] F.H. Gaensslen, "Geometry Effects of Small MOSFET Devices", IBM J. Res. Develop. 23 (1979) 682.
- [1.7] N. Shigyo and R. Dang, "Analysis of an Anomalous Sub-threshold Current in a Fully Recessed Oxide MOSFET Using a Three-Dimensional Device Simulator", IEEE ED-32 (1985) 441.

- [1.8] H. Masuda, T. Toyabe, T. Haguwara and Y. Ushiro, "High-Speed Three-Dimensional Device Simulator on a Supercomputer: CADDETH", Proc. IEEE Int. Symp. on Circuits and Systems (1984) 1163.
- [1.9] T. Toyabe, H. Masuda, Y. Aoki, H. Shukuri and T. Hagiwara, "Three-Dimensional Device Simulator CADDETH with Highly Convergent Matrix Solution Algorithms", IEEE ED-32 (1985) 2038.
- [1.10] H. Masuda, T. Toyabe, H. Shukuri, K. Ohshima and K. Itoh, "A Full Three-Dimensional Simulation on Alpha-Particle Induced DRAM Soft-Errors", IEDM Tech. Dig. (1985) 496.
- [1.11] M. Thurner P. Lindorfer and S. Selberherr, "Numerical Treatment of Nonrectangular Field-Oxide for 3-D MOS-FET Simulation", Proc. SISDEP Vol.3 (1988) 375.
- [1.12] M. Thurner P. Lindorfer and S. Selberherr, "Numerical Treatment of Nonrectangular Field-Oxide for 3-D MOS-FET Simulation", IEEE CAD-9 (1990) 1189.
- [1.13] S. Selberherr, "The Status of MINIMOS", Proc. SISDEP Vol.2 (1986) 2.
- [1.14] P. Conti, "Manual for the tensor grid generator gen", ETH Zürich, Zurich, Swiss, 1989.
- [1.15] G. Heiser, "MEDES User's Guide" and "MEDES Program Documentation", ETH Zürich, Zurich, Swiss, 1989.
- [1.16] G. Heiser, "SIMBAD A Hard- and Software Independent Binary I/O Interface", Technical Report 24, Integrated Systems Laboratory ETH Zurich, Zurich, Swiss, 1988.
- [1.17] P. Conti, N. Hitschfeld and W. Fichtner, " Ω - an octree-based mixed element grid allocator for adaptive 3d device simulation", IEEE CAD-9 (1991) in press.

- [1.18] P. Conti, G. Heiser and W. Fichtner, "Three-dimensional transient simulation of complex silicon devices", *Jap. J. Appl. Phys. Letters* 29 (1990) 12.
- [1.19] M. Westermann, "PICASSO: Ein Programm zur Visualisierung von zwei- und dreidimensionalen Simulationsergebnissen", master's thesis, ETH Zürich, Zurich, Swiss, 1990.
- [1.20] G. Baccarani, R. Guerrieri, P. Ciampolini and M. Rudan, "HFIELDS: a Highly-Flexible 2-D Semiconductor-Device Analysis Program", *Proc. NASECODE IV* (1985) 3.
- [1.21] TCAD, Technology Modeling Associates Inc., Newsletter July 1990.
- [1.22] TCAD, Technology Modeling Associates Inc., Newsletter January 1990.
- [1.23] W. Bergner and R. Kircher, "SITAR - An Efficient 3D Simulator for Optimization of Non-Planar Trench Structures", *Proc. SISDEP Vol.3* (1988) 165.
- [1.24] W. Bergner and R. Kircher, "SITAR - An Efficient 3-D Simulator for Optimization of Nonplanar Trench Structures", *IEEE CAD-11* (1990) 1184.
- [2.1] J.W. Slotboom and H.C. deGraaff, "Measurements of the Band Gap Narrowing in Si Bipolar Transistors", *Solid State Electr.* 19 (1976) 857.
- [2.2] J.W. Slotboom and H.C. deGraaff, "Band Gap Narrowing in Si Bipolar Transistors", *IEEE ED-24* (1977) 1123.
- [2.3] S.M. Sze, "Physics of Semiconductor Devices", John Wiley & Sons, New York, 1981.
- [2.4] D.M. Caughey and R.E. Thomas, "Carrier Mobility in Silicon Empirically Related to Doping and Field", *Proc. IEEE* 55 (1967) 2192.

- [2.5] N.D. Arora, J.R. Hauser and D.J. Roulston, "Electron and Hole Mobilities in Silicon as a Function of Concentration and Temperature", *IEEE ED-29* (1982) 292.
- [2.6] K.K. Thornber, "Relation of drift velocity to low-field mobility and high-field saturation velocity", *J. Appl. Phys.* 51 (1980) 2127-2136.
- [2.7] K. Yamaguchi, "A Mobility Model for Carriers in the MOS Inversion Layer", *IEEE ED-30* (1983) 658.
- [2.8] R.N. Hall, "Electron-Hole Recombination in Germanium", *Phys. Rev.* 87 (1952) 387.
- [2.9] W. Shockley and W.T. Read, "Statistics of Recombination of Holes and Electrons", *Phys. Rev.* 87 (1952) 835.
- [2.10] A.S. Chynoweth, *Phys. Rev.* 109 (1958) 1537.
- [2.11] A.F. Franz and G.A. Franz, "BAMBI - A Device Model for Power MOSFET's", *IEEE CAD-4* (1985) 177.
- [2.12] O.E. Akcasu, J.L. Bouknight, T. Luich, R. Jerome and S. Leibiger, "Three Dimensional Transient Simulation of Electro-Thermal Behavior in Semiconductor Devices and It's Applications", *IEDM Tech. Dig.* (1987) 514.
- [3.1] "GALENE II Version 1.3 User's Guide", RWTH Aachen, Aachen, Germany 1990.
- [3.2] G. Nanz, "Numerische Methoden in der zweidimensionalen Halbleiterbauelementesimulation", TU Wien, Vienna, Austria 1989.
- [3.3] M.R. Pinto, C.S. Rafferty and R.W. Dutton, "PISCES II: Poisson and Continuity Equation Solver", Stanford University, Stanford 1984.
- [3.4] G.E. Forsythe and W.R. Wasaw, "Finite Difference Methods for Partial Differential Equations", Wiley & Sons, New York, 1960.

- [3.5] R. Kircher and W. Bergner, "Modeling of Charge Conservation in Isolated Silicon Regions", *Jap. J. Appl. Phys.* 28 (1989) 2454.
- [4.1] R.E. Bank and D.J. Rose, "Global Approximate Newton Method", *Numer. Math.* 37 (1981) 279.
- [4.2] K.H. Gummel, "A Self-Consistent Iteration Scheme for One-Dimensional Steady State Transistor Calculations", *IEEE ED-16* (1964) 455.
- [4.3] W.H. Press, B.P. Flannery, S.A. Teukolsky and W.T. Vetterling, "Numerical Recipes", Cambridge University Press, Cambridge 1988.
- [4.4] A.C. Aitken, "Studies in Practical Mathematics V. On the Iterative Solution of a System of Linear Equations", *Proc. Roy. Soc. Edinburgh Sec. A*63 (1950) 52.
- [4.5] J.W. Sheldon "On the Numerical Solution of Elliptic Difference Equations", *Math. Tables Aids Comput.* 9 (1955) 101.
- [4.6] M.R. Hestenes and E. Stiefel, "Methods of Conjugate Gradients for Solving Linear Systems", *J. Research of NBS* 49 (1952) 409.
- [4.7] P. Sonneveld, "CGS, a Fast Lanczos-Type Solver for Non-symmetric Linear Systems", Delft University, Dept. of Math., Delft, The Netherlands, Rept. 84-16 (1984).
- [4.8] R. Fletcher, "Conjugate Gradient Methods for Indefinite Systems", *Proc. of the 1974 Dundee Biennial Conf. on Numerical Analysis*, Springer-Verlag, Berlin (1975) 73.
- [4.9] Y. Saad, "The Lanczos Biorthogonalization Algorithm and Other Oblique Projection Methods for Solving Large Unsymmetric Systems", *SIAM J. Numer. Anal.* 19 (1982) 470.

- [4.10] T. Wada and R.L.M. Dang, "Modification of ICCG method for application to semiconductor device simulators", *Electron. Lett.* 18 (1982) 265.
- [5.1] H. Sunami, T. Kure, N. Hashimoto, K. Itoh, T. Toyabe and S. Asai, *IEDM Tech. Dig.* (1982) 806.
- [5.2] S. Nakajima, K. Minegishi, K. Miura, T. Morie, M. Kimizuka and T. Mano, "A Submicrometer Megabit DRAM Process Technology Using Trench Capacitors", *IEEE ED-32* (1985) 210.
- [5.3] H. Sunami, T. Kure, K. Yagi, Y. Wada, K. Yamaguchi, H. Miyazawa and S. Shimizu, "Scaling Considerations and Dielectric Breakdown Improvement of a Corrugated Capacitor Cell for a Future DRAM", *IEEE SC-20* (1985) 216.
- [5.4] K. Yamaguchi, R. Nishimura, T. Hagiwara and H. Sunami, "Two-Dimensional Numerical Model of Memory Devices with a Corrugated Capacitor Cell Structure", *IEEE SC-20* (1985) 202.
- [5.5] H. Sunami, "Cell Structures for Future DRAM's", *IEDM Tech. Dig.* (1985) 694.
- [5.6] K. Yamada, K. Yamabe, Y. Tsunashima, K. Imai, T. Kashio and H. Tango, "A Deep-Trenched Capacitor Technology for 4 Mega Bit Dynamic RAM", *IEDM Tech. Dig.* (1985) 702.
- [5.7] H. Ishiuchi, T. Watanabe, K. Kishi, M. Ishikawa, N. Goto, T. Tanaka, T. Mochizuki and O. Ozawa, "Submicron CMOS Technologies for Four Mega Bit Dynamic RAM", *IEDM Tech. Dig.* (1985) 706.
- [5.8] N.C.-C. Lu, "Advanced Cell Structures for Dynamic RAMs", *Proc. Int. Symp. on VLSI Technology, Systems and Applications* (1987) 163.
- [5.9] P.A. Murkin, H.-M. Mühlhoff, S. Röhl, Meyberg, W. Müller, W. Bergner and R. Kircher, "Isolation-Related

- Leakage in a 4 Mb DRAM Cell”, Proc. ESSDERC (1987) 761.
- [5.10] M. Elahy, H. Shichijo, P.K. Chatterjee, A.H. Shah, S.K. Banerjee and R.H. Womack, “Trench Capacitor Leakage in High-Density DRAM’s”, IEEE ED-5 (1984) 527.
- [5.11] K. Yamaguchi, R. Nishimura, T. Hagiwara and H. Sunami, “Two-Dimensional Numerical Model of Memory Devices with a Corrugated Capacitor Cell Structure”, IEEE ED-32 (1985) 282.
- [5.12] E. Takeda, K. Takeuchi, H. Hiraiwa, T. Toyabe, H. Sunami and K. Itoh, “Three Dimensional Leakage Current in Corrugated Capacitor Cells”, Proc. SSDM (1985) 37.
- [5.13] T. Hamamoto, N. Shigyo, K. Hieda and M. Wada, “Current Leakage Analysis of Folded Capacitor Cell (FCC) for Future Megabit DRAMs”, Proc. SSDM (1985) 41.
- [5.14] W. Bergner, “Physikalische Simulation von 3D Punch Through Effekten in der Trenchzelle”, master’s thesis, TU München, Munich, Germany 1988.
- [5.15] N.C.-C. Lu, P.E. Cottrell, W.J. Craig, S. Dash, D.L. Critchlow, R.L. Mohler, B.J. Machesney, T.H. Ning, W.P. Noble, R.M. Parent, R.E. Scheuerlein, E.J. Sprogis and L.M. Terman, “A Substrate-Plate Trench Capacitor (SPT) Memory Cell for Dynamic RAM’s”, IEEE SC-21 (1986) 627.
- [5.16] M. Tamaguchi, S. Ando, N. Higaki, G. Goto, T. Ema, K. Hashimoto, T. Yabu and T. Nakano, “Dielectrically Encapsulated Trench Capacitor Cell”, IEDM Tech. Dig. (1986) 136.
- [5.17] S. Yoshikawa, S. Sawada, T. Mizuno, J. Kumagai, T. Hamamoto, H. Aochi, K. Toita, S. Kaki, Y. Saito and S. Shinozaki, “Process Technologies for a High Speed 16M DRAM with Trench Type Cell”, Proc. Int. Symp. on VLSI Technology, Systems and Applications (1989) 67.

- [5.18] K. Tsukamoto, M. Shimizu, M. Inuishi, Y. Matsuda, H. Oda, H. Morita, M. Nakajima, K. Kobayashi, Y. Mashiko and Y. Akasaka, "Double Stacked Capacitor with Self-Aligned Poly Source/Drain Transistor(DSP) Cell for Megabit DRAM", IEDM Tech. Dig. (1987) 328.
- [5.19] T. Kaga, Y. Kawamoto, T. Kure, Y. Nakagome, M. Aoki, H. Sunami and K. Itoh, "A 4.2 fm Half-Vcc Sheath-Plate Capacitor DRAM Cell with Self-Aligned Buried Plate-Wiring", IEDM Tech. Dig. (1987) 332.
- [5.20] S. Nakajima, K. Miura, K. Minegishi and T. Morie, "An Isolation-Merged Vertical Capacitor Cell for Large Capacity DRAM", IEDM Tech. Dig. (1984) 240.