

References

1. Al A, Rao BP, Kudva S, Babu S, Suman D, Rao A (2004) Quality and complexity comparison of H.264 intra mode with JPEG2000 and JPEG. In: Proceedings of IEEE international conference on image processing, Singapore, October 2004, pp 525–528
2. Bojnordi MN, Fatemi O, Hashemi MR (2006) An efficient deblocking filter with self-transposing memory architecture for H.264/AVC. In: Proceedings of IEEE international conference on acoustics, speech and signal processing, Toulouse, France, May 2006, pp II–II
3. Chen T-C, Chien S-Y, Huang Y-W, Tsai C-H, Chen C-Y, Chen T-W, Chen L-G (2006) Analysis and architecture design of an HDTV720p 30 frames/s H.264/AVC encoder. *IEEE Trans Circuits Syst Video Technol* 16(6):673–688
4. Chang C-R, Chen J-W, Lo T-J, Chiu C-L, Chang Y-H, Tzeng H-C, Shih S-Y, Kao Y-C, Kao C-Y, Lin Y-L (2006) An H.264/AVC main profile hardwired decoder. In: Proceedings of the 2006 picture coding symposium, Beijing, China, April 2006
5. Chang H-C, Chen J-W, Su C-L, Yang Y-C, Li Y, Chang C-H, Chen Z-M, Yang W-S, Lin C-C, Chen C-W, Wang J-S, Quo J-I (2007) A 7 mW-to-183 mW dynamic quality-scalable H.264 video encoder chip. In: IEEE international solid-state circuits conference, Digest of technical papers, San Francisco, USA, February 2007, pp 280–603
6. Chen K-H, Guo J-I, Chao K-C, Wang J-S, Chu Y-S (2005) A high-performance low power direct 2-D transform coding IP design for MPEG-4 AVC/H.264 with a switching power suppression technique. In: Proceedings of IEEE international symposium on VLSI design, automation and test, Hsinchu, Taiwan, April 2005, pp 291–294
7. Cheng C-C, Chang T-S (2005) Fast three step intra prediction algorithm for 4×4 blocks in H.264. In: Proceedings of IEEE international symposium on circuits and systems, Kobe, Japan, May 2005, pp 1509–1512
8. Chen J-W, Chang C-R, Lin Y-L (2005) A hardware accelerator for context-based adaptive binary arithmetic decoding in H.264/AVC. In: Proceedings of IEEE international symposium on circuits and systems, Kobe, Japan, May 2005, pp 4525–4528
9. Chen K-H, Guo J-I, Wang J-S (2006) A high-performance direct 2-D transform coding IP design for MPEG-4 AVC/H.264. *IEEE Trans Circuits Syst Video Technol* 16(4):472–483
10. Chen T-C, Huang Y-W, Chen L-G (2004) Fully utilized and reusable architecture for fractional motion estimation of H.264/AVC. In: Proceedings of IEEE international conference on acoustics, speech, and signal processing, Montreal, Canada, May 2004, pp 9–12
11. Chen J-L, Lin Y-K, Chang T-S (2007) A low cost context adaptive arithmetic coder for H.264/MPEG-4 AVC video coding. In: Proceedings of IEEE international conference on acoustics, speech and signal processing, Hawaii, USA, April 2007, pp 105–108
12. Chen J-W, Lin Y-L (2007) A high-performance hardwired CABAC decoder. In: Proceedings of IEEE international conference on acoustics, speech, and signal processing, Hawaii, USA, April 2007, pp 37–40
13. Chao P, Lin Y-L (2008) A motion compensation system with a high efficiency reference frame pre-fetch scheme for QFHD H.264/AVC decoder. In: Proceedings of IEEE international symposium on circuits and systems, Seattle, USA, May 2008, pp 256–259

14. Chao P, Lin Y-L (2008) Reference frame access optimization for ultra high resolution H.264/AVC decoding. In: Proceedings of IEEE international conference on multimedia and expo, Hanover, Germany, June 2008, pp 1441–1444
15. Chen Y-J, Tsai C-H, Chen L-G (2007) Novel configurable architecture of ML-decomposed binary arithmetic encoder for multimedia applications. In: Proceedings of IEEE international symposium on VLSI design, automation, and test, Hsinchu, Taiwan, April 2007, pp 1–4
16. Chao YC, Lin JK, Yang JF, Liu BD (2006) A high throughput and data reuse architecture for H.264/AVC deblocking filter. In: Proceedings of Asia Pacific conference on circuits and systems, Singapore, December 2006, pp 1260–1263
17. Chang SC, Peng WH, Wang SH, Chiang T (2005) A platform based bus-interleaved architecture for deblocking filter in H.264/MPEG-4 AVC. *IEEE Trans Consumer Electron* 51(1):249–255
18. Yang C, Goto S, Ikenaga T (2006) High performance VLSI architecture of fractional motion estimation in H.264 for HDTV. In: Proceedings of IEEE international symposium on circuits and systems, Island of Kos, Greece, May 2006, pp 2605–2608
19. Huang YW, Chen TW, Hsieh BY, Wang TC, Chang TH, Chen, LG (2003) Architecture design for deblocking filter in H.264/JVT/AVC. In: Proceedings of IEEE international conference on multimedia and expo, Baltimore, USA, July 2003, pp I-693-6
20. He Z, Liou M-I (1997) Reducing hardware complexity of motion estimation algorithms using truncated pixels. In: Proceedings of IEEE international symposium on circuits and systems, Hong Kong, China, June 1997, pp 2809–2812
21. Huang Y-W, Hsieh B-Y, Chen T-C, Chen L-G (2005) Analysis, fast algorithm, and VLSI architecture design for H.264/AVC intra frame coder. *IEEE Trans Circuits Syst Video Technol* 15(3):378–401
22. Huang Y-W, Wang T-C, Hsieh B-Y, Chen L-G (2003) Hardware architecture design for variable block size motion estimation in MPEG-4 AVC/JVT/ITU-T H.264. In: Proceedings of IEEE international symposium on circuits and systems, Bangkok, Thailand, May 2003, pp II796–II799
23. Hou K-C, Wang S-Z, Huang Y-H, Liu T-M, Lee C-Y (2006) A bandwidth-efficient motion compensation architecture for H.264/AVC HDTV decoder. In: Proceedings of 17th VLSI design/CAD symposium, Hualian, Taiwan, August 2006
24. Joch A, Kossentini F, Schwarz H, Wiegand T, Sullivan G (2002) Performance comparison of video coding standards using Lagrangian coder control. In: Proceedings of IEEE international conference on image processing, New York, USA, September 2002, pp 501–504
25. Kao C-Y, Kuo H-C, Lin Y-L (2006) High performance fractional motion estimation and mode decision for H.264/AVC. In: Proceedings of IEEE international conference on multimedia and expo, Toronto, Canada, July 2006, pp 1241–1244
26. Kao C-Y, Lin Y-L (2008) A high-performance and memory-efficient architecture for H.264/AVC motion estimation. In: Proceedings of IEEE international conference on multimedia and expo, Hanover, Germany, June 2008, pp 141–144
27. Kao C-Y, Lin Y-L (in press) A memory-efficient and highly parallel architecture for variable block size integer motion estimation in H264/AVC. *IEEE Trans Very Large Scale Integr Syst*
28. Kao C-Y, Wu C-L, Lin Y-L (in press) A high performance three-engine architecture for H.264/AVC fractional motion estimation. *IEEE Trans Very Large Scale Integr Syst*
29. Ku C-W, Cheng C-C, Yu G-S, Tsai M-C, Chang T-S (2006) A high-definition H.264/AVC intra-frame codec IP for digital video and still camera applications. *IEEE Trans Circuits Syst Video Technol* 16(8):917–928
30. Kim M, Hwang I, Chae S-I (2005) A fast VLSI architecture for full-search variable block size motion estimation in MPEG-4 AVC/H.264. In: Proceedings of Asia and South Pacific design automation conference, Shanghai, China, January 2005, pp 631–634
31. Koga T, Iinuma K, Hirano A, Iijima Y, Ishiguro T (1981) Motion compensated interframe coding for video conferencing. In: Proceedings of national telecommunication conference, New Orleans, USA, November 1981, pp C9.6.1–C9.6.5

32. Kao Y-C, Kuo H-C, Lin Y-T, Hou C-W, Li Y-H, Huang H-T, Lin Y-L (2006) A high-performance VLSI architecture for intra prediction and mode decision in H.264/AVC video encoding. In: Proceedings of IEEE Asia-Pacific conference on circuits and systems, Singapore, December 2006, pp 562–565
33. Khurana G, Kassim AA, Ping CT, Mi MB (2006) A pipelined hardware implementation of in-loop deblocking filter in H.264/AVC. *IEEE Trans Consum Electron* 52(2):536–540
34. Komerek T, Pirsch P (1989) Array architectures for block matching algorithms. *IEEE Trans Circuits Syst Video Technol* 36(10):1301–1308
35. Kuo T-Y, Lin Y-K, Chang T-S (2007) SIFME: a single iteration fractional-pel motion estimation algorithm and architecture for HDTV sized H.264 video coding. In: Proceedings of IEEE international conference on acoustics, speech, and signal processing, Hawaii, USA, April 2007, pp 1185–1188
36. Kuo H-C, Lin Y-L (2008) An H.264/AVC full-mode intra-frame encoder for 1080HD video. In: Proceedings of IEEE international conference on multimedia and expo, Hanover, Germany, June 2008, pp 1037–1040
37. Lappalainen V, Hallapuro A, Hamalainen T (2003) Complexity of optimized H.26L video decoder implementation. *IEEE Trans Circuits Syst Video Technol* 13(7):717–725
38. Lin H-Y, Chao Y-C, Chen C-H, Liu B-D, Yang J-F (2005) Combined 2-D transform and quantization architectures for H.264 video coders. In: Proceedings of IEEE international symposium on circuits and systems, Kobe, Japan, May 2005, pp 1802–1805
39. Lin Y-C, Chao P, Hung W-C, Peng H-K, Lee C-H, Chen J-W, Lo T-J, Chang Y-H, Hsu S-T, Jan K-Y (2006) A pure hardwired H.264/AVC video decoder on an SOC platform. In: International SOC conference, Seoul, Korea, October 2006
40. Liu P-S, Chen J-W, Lin Y-L (2007) A hardwired context-based adaptive binary arithmetic encoder for H.264 advanced video coding. In: Proceedings of IEEE international symposium on VLSI design, automation, and test, Hsinchu, Taiwan, April 2007, pp 1–4
41. Li L, Goto S, Ikenaga T (2005) An efficient deblocking filter architecture with 2-dimensional parallel memory for H.264/AVC. In: Proceedings of Asia South Pacific design automation conference, Shanghai, China, January 2005, pp 623–626
42. Lin C-C, Lin Y-K, Chang T-S (2007) PMRME: a parallel multi-resolution motion estimation algorithm and architecture for HDTV sized H.264 video coding. In: Proceedings of IEEE international conference on acoustics, speech, and signal processing, Hawaii, USA, April 2007, pp 285–288
43. Lin YC, Lin YL (2009) A two-result-per-cycle deblocking filter architecture for QFHD H.264/AVC decoder. *IEEE transactions on very large scale integration systems* 17(6):838–843
44. Li Y, Qu Y, He Y (2007) Memory cache based motion compensation architecture for HDTV H.264/AVC decoder. In: Proceedings of IEEE international symposium on circuits and systems, New Orleans, USA, May 2007, pp 2906–2909
45. List P, Joch A, Lainema J, Bjntegarrd G, Karczewicz M (2003) Adaptive deblocking filter. *IEEE Trans Circuits Syst Video Technol* 13(7):614–619
46. Li D-W, Ku C-W, Cheng C-C, Lin Y-K, Chang T-S (2007) A 61 MHz 72k gates 1,280 × 720 30 fps H.264 intra encoder. In: Proceedings of IEEE international conference on acoustics, speech and signal processing, Hawaii, USA, April 2007, pp (II) 801–804
47. Lin Y-K, Li D-W, Lin C-C, Kuo T-Y, Wu S-J, Tai W-C, Chang W-C, Chang T-S (2008) A 242-mW 10-mm² 1080p H.264/AVC high-profile encoder chip. In: IEEE international solid-state circuits conference, Digest of technical papers, San Francisco, USA, February 2008, pp 314–615
48. Liu TM, Lee WP, Lin TA, Lee CY (2005) A memory-efficient deblocking filter for H.264/AVC video coding. In: Proceedings of IEEE international symposium on circuits and systems, Kobe, Japan, May 2005, pp 2140–2143
49. Lo C-C, Zeng Y-J, Shieh M-D (2007) Design and test of a high-throughput CABAC encoder. In: Proceedings of IEEE international technical conference of IEEE region 10, Taipei, Taiwan, October 2007, pp 1–4

50. Li L, Song Y, Ikenaga T, Goto S (2006) A CABAC encoding core with dynamic pipeline for H.264/AVC main profile. In: Proceedings of Asia Pacific conference on circuits and system, Singapore, December 2006, pp 760–763
51. Liu Z, Song Y, Shao M, Li S, Li L, Ishiwata S, Nakagawa M, Goto S, Ikenaga T (2007) A 1.41-W H.264/AVC real-time encoder SOC for HDTV1080P. In: Proceedings of IEEE symposium on VLSI circuits, Kyoto, Japan, June 2007, pp 12–13
52. Lin HY, Yang JJ, Liu BD, Yang JF (2006) Efficient deblocking filter architecture for H.264 video coders. In: Proceedings of IEEE international symposium on circuits and systems, Island of Kos, Greece, May 2006, p 4
53. Marpe D, Schwarz H, Wiegand T (2003) Context-based adaptive binary arithmetic coding in the H.264/AVC video compression standard. *IEEE Trans Circuits Syst Video Technol* 17(7):620–636
54. Meng B, Au O-C (2003) Fast intra-prediction mode selection for 4A blocks in H.264. In: Proceedings of IEEE international conference on acoustics, speech, and signal processing, Hong Kong, China, April 2003, pp (III) 389–392
55. Osorio R, Bruguera J (2006) High-throughput architecture for H.264/AVC CABAC compression system. *IEEE Trans Circuits Syst Video Technol* 16(11):1376–1384
56. Peng H-K, Lee C-H, Chen J-W, Lo T-J, Chang Y-H, Hsu S-T, Lin Y-C, Chao P, Hung W-C, Jan K-Y (2007) A highly integrated 8-mW H.264/AVC main profile real-time CIF video decoder on a 16-MHz SoC platform. In: Proceedings of Asia and South Pacific design automation conference, Yokohama, Japan, January 2007, pp 112–113
57. Sayood K (2006) Introduction to data compression. Morgan-Kaufmann, San Francisco, CA
58. Shih SY, Chang CR, Lin YL (2005) An AMBA-compliant deblocking filter IP for H.264/AVC. In: Proceedings of IEEE international symposium on circuits and systems, Kobe, Japan, May 2005, pp 4529–4532
59. Shih SY, Chang CR, Lin YL (2006) A near optimal deblocking filter for H.264 advanced video coding. In: Proceedings of Asia South Pacific design automation conference, Yokohama, Japan, January 2006, p 6
60. Shojania H, Sudharsanan S (2005) A high performance CABAC encoder. In: Proceedings of IEEE international Northeast workshop on circuits and systems, Ville de Quebec, Canada, June 2005, pp 315–318
61. Suh K, Park S, Cho H (2005) An efficient hardware architecture of intra prediction and TQ/IQIT module for H.264 encoder. *Electron Telecommun Res Inst J* 27(5):511–524
62. Sullivan G, Wiegand T (1998) Rate-distortion optimization for video compression. *IEEE Signal Process Mag* 15(6):74–90
63. Su C-L, Yang W-S, Chen Y-L, Li Y, Chen C-W, Guo J-I, Tseng S-Y (2006) Low complexity high quality fractional motion estimation algorithm and architecture design for H.264/AVC. In: Proceedings of IEEE Asia Pacific symposium on circuits and systems, Singapore, December 2006, pp 578–581
64. Su C-L, Yang W-S, Chen Y-L, Yang Y-C, Chen C-W, Guo J-I, Tseng S-Y (2006) A low complexity high quality interger motion estimation architecture design for H.264/AVC. Proceedings of IEEE Asia Pacific conference on circuits and systems, Singapore, December 2006, pp 398–401
65. Takizawa T, Hirasawa M (2001) An efficient memory arbitration algorithm for a single chip MPEG2 AV decoder. *IEEE Trans Consum Electron* 47(3):660–665
66. Takizawa T, Tajime J, Harasaki H (1999) High performance and cost effective memory architecture for an HDTV decoder LSI. In: Proceedings of IEEE international conference on acoustics, speech, and signal processing, Phoenix, USA, March 1999, pp 1981–1984
67. Tsai C-Y, Chen T-C, Chen T-W, Chen L-G (2005) Bandwidth optimized motion compensation hardware design for H.264/AVC HDTV decoder. In: Proceedings of 48th midwest symposium on circuits and systems, Cincinnati, USA, August 2005, pp 1199–1202
68. Tham J, Ranganath S, Ranganath M, Kassim A (1998) A novel unrestricted center-biased diamond search algorithm for block motion estimation. *IEEE Trans Circuits Syst Video Technol* 8(4):369–377

69. Tseng H-C, Chang C-R, Lin Y-L (2005) A motion compensator with parallel memory for H.264 advance video coding. In: Proceedings of 16th VLSI design/CAD symposium, Hualian, Taiwan, August 2005
70. Tseng H-C, Chang C-R, Lin Y-L (2005) A hardware accelerator for H.264/AVC motion compensation. Proceedings of IEEE workshop on signal processing systems, Athens, Greece, November 2005, pp 214–219
71. Tuan J-C, Chang T-S, Jen C-W (2002) On the data reuse and memory bandwidth analysis for full-search block-matching VLSI architecture. *IEEE Trans Circuits Syst Video Technol* 12(1):61–72
72. Vos L, Stegherr M (1989) Parameterizable VLSI architectures for the full-search block-matching algorithm. *IEEE Trans Circuits Syst* 36(10):1309–1316
73. Wang Y-J, Cheng C-C, Chang T-S (2007) A fAST aLGORITHM AND iTS VLSI architecture for fractional motion estimation for H.264/MPEG-4 AVC video coding. *IEEE Trans Circuits Syst Video Technol* 17(5):578–583
74. Wang T-C, Huang Y-W, Fang H-C, Chen L-G (2003) Parallel 4×4 2D transform and inverse transform architecture for MPEG-4 AVC/H.264. In: Proceedings of IEEE international symposium on circuits and systems, Bangkok, Thailand, May 2003, pp (II)800–803
75. Wang S-Z, Lin T-A, Liu T-M, Lee C-Y (2005) A new motion compensation design for H.264/AVC decoder. In: Proceedings of IEEE international symposium on circuits and systems, Kobe, Japan, May 2005, pp 4558–4561
76. Wang S-H, Peng W-H, He Y, Lin G-Y, Lin C-Y, Chang S-C, Wang C-N, Chiang T (2003) A platform-based MPEG-4 advanced video coding (AVC) decoder with block level pipelining. In: Proceedings of the 2003 joint conference of the fourth international conference on information, communications and signal processing and the Fourth Pacific rim conference on multimedia, Singapore, December 2003, pp 51–55
77. Wu C-L, Kao C-Y, Lin YL (2008) A high performance three-engine architecture for H.264/AVC fractional motion estimation. In: Proceedings of IEEE international conference on multimedia and expo, Hanover, Germany, June 2008, pp 133–136
78. Wang J-C, Wang J-F, Yang J-F, Chen J-T (2007) A fast mode decision algorithm and its VLSI design for H.264/AVC intra-prediction. *IEEE Trans Circuits Syst Video Technol* 17(10):1414–1422
79. Yap S, McCanny J (2004) A VLSI architecture for variable block size video motion estimation. *IEEE Trans Circuits Syst II, Express Briefs* 51(7):384–389
80. Yang K-M, Sun M-T, Wu L (1989) A family of VLSI designs for the motion compensation block-matching algorithm. *IEEE Trans Circuits Syst Video Technol* 36(10):1317–1325
81. Yeo H, Hu Y-H (1995) A novel modular systolic array architecture for full-search block matching motion estimation. *IEEE Trans Circuits Syst Video Technol* 5(5):407–416
82. Zhang P, Gao W, Wu D, Xie D (2006) An efficient reference frame storage scheme for H.264 HDTV decoder. In: Proceedings of IEEE international conference on multimedia and expo, Toronto, Canada, July 2006, pp 361–364
83. Zhang N-R, Li M, Wu W-C (2006) High performance and efficient bandwidth motion compensation VLSI design for H.264/AVC decoder. In: Proceedings of 8th international conference on solid-state and integrated circuit technology, Shanghai, China, October 2006, pp 1896–1898
84. Zhu S, Ma K (1997) A new diamond search algorithm for fast block matching motion estimation. In: Proceedings of international conference on information, communications and signal processing, Singapore, September 1997, pp 292–296

Index

k^{th} Order Exp–Golomb Code Method, 128
1-D array architecture, 37
1080pHD, 16, 97
2-D array architecture, 37, 39
4Kx2K, 30
720pHD, 155

A

adaptive macroblock transmission scheme, 115
AMBA, 159, 162
 master, 163
 slave, 163
arbitration policy, 76
ASIC, 156

B

BAE architecture
 ML–decomposed, 137
 Multi–Bin, 137
 One–Bin, 136
 Two–Bin, 137
bank conflict, 76
basic pattern, 89
BCMODS, 140
bi prediction, 75
binarization, 125, 126, 141
Binarization and Context Modeler (BCM),
 140
binary arithmetic encoder (BAE), 125, 130,
 140
 bypass, 126, 131
 regular, 126, 130
 terminal, 126, 131
bit-stream
 H.264/AVC, 153, 158
 MB-level, 153
bitOutstanding, 131, 144, 146
block

 AC, 86
 DC, 86
blocking artifact, 6, 8, 107, 111
boundary strength (BS), 108, 109, 115, 117

C

CABAC, 125, 155
CAVLC, 8, 125, 155
Cb, 2, 12, 86
chroma_pre_mode SE, 132
chromaEdgeflag, 112
chrominance (chroma), 2
CIF, 13
coded block flag (CBF), 94, 96, 133
coded block pattern (CBP), 94
coeff_level SE, 129, 133
coefficient, 5, 86, 89, 133
Concatenation Method, 128
context index (CtxIdx), 129
context modeler, 125, 129
context table, 126
Cr, 2, 12, 86
CtxBlkCatOffset, 129
CtxIdx Left–Inc, 129
CtxIdx Top–Inc, 129
CtxIdxInc, 129
CtxIdxOffset, 129

D

Data-Reuse Scheme, 43
 Level A, 43
 Level B, 43
 Level C, 43, 45, 52
 Level D, 43
deblocking filter (DF), 8, 107, 108, 116
down-sampling, 36, 49, 53
DRAM, 83, 156
 access penalty, 75, 76, 159

E

edge filter, 108, 112
 strong edge filter, 108, 112
 weak edge filter, 108, 112
 entropy encoder, 86
 Exp–Golomb code method, 128

F

filtering strength, 108
 FilterOffsetA, 111
 FilterOffsetB, 111
 filterSampleflag, 108, 109, 111
 Fixed–Length Code Method, 128
 frame
 B-type, 152
 I-type, 152
 P-type, 152
 frames per second (fps), 1, 31
 full high definition (FullHD), 1

G

group-of-picture (GOP), 163

H

H.263, 85, 151
 half refinement, 58, 70
 HDTV, 31
 Huffman, 126

I

in–loop filter, 108
 indexA, 111
 indexB, 111
 inter–stage register bypass scheme, 137
 interpolation, 64, 75, 76, 79
 2-tap filter, 59
 6-tap filter, 59
 half-pixels, 79
 quarter-pixels, 79
 interpolation engine
 1-D based, 76
 2-D based, 76
 dual, 79
 separate 1-D based, 76
 interprediction, 4
 intra encoding, 11
 intra mode
 DC, 13
 DDL, 22
 DDR, 22
 HD, 22
 horizontal, 13

HU, 22

plane, 13
 vertical, 13
 VL, 22
 VR, 22

intra prediction, 4, 8, 11, 85, 107
 intra4x4_pre_mode SE, 132
 InvLevelScale, 92
 ISO/IEC, 73, 151
 ITU-T, 73, 151

J

Joint Model (JM), 19, 53, 135, 155
 JPEG2000, 11

L

L-C correlated mapping, 76
 Lagrangian parameter, 60, 152
 last significant coefficient flag, 93, 133
 Least Probable Symbol (LPS), 130
 least-significant-bits (LSB), 5
 LevelScale, 91
 list0, 75
 list1, 75
 luminance (luma), 2

M

macroblock, 2
 B-type, 151
 I-type, 86, 151
 intra 16x16, 86
 non-intra 16x16, 86
 P-type, 151
 mb_type SE, 128
 Media embedded Processor, 156
 memory access unit (MAU), 158, 163
 mode
 non-reconstruction-loop (Non-RL), 20
 reconstruction-loop (RL), 20
 mode decision
 all-mode, 19
 inter, 151
 intra, 13, 19, 151
 macroblock, 152
 partial-mode, 19
 rate-distortion optimized (RDO), 155
 mono prediction, 75
 Most Probable Symbol (MPS), 130
 Most Significant Bit (MSB), 147
 motion compensation, 7, 8, 73, 77, 107

motion estimation, 4, 31, 85
 block-based, 31, 33
 Diamond Search, 34
 fixed block size, 32, 57
 fractional, 32, 58
 Full Search, 33, 36, 153
 integer, 32, 58
 Three Step Search, 34
 variable block size, 32, 57
 motion vector (MV), 4, 33, 58, 151
 difference, 4, 73, 77
 predictor, 32, 65, 74, 77
 motion_vector_difference (MVD) SE, 133
 motion_vector_difference SE
 horizontal, 143
 vertical, 143
 Moving Picture Experts Group (MPEG), 73
 MPEG-1, 2
 MPEG-2, 2, 151
 MPEG-4, 85, 151
 multiple-candidate data reuse, 41, 44, 46, 52
 multiple-candidate parallel architecture, 41, 42
 multiple-macroblock data reuse, 44–46, 52
 MV-bit-rate estimation, 58, 59

N

Non-skip-all mode, 122

P

Parallel-In-Parallel-Out (PIPO), 140
 partial-search algorithm, 43
 ping-pong fashion, 102, 158
 pipeline hazard, 121
 pixel duplication, 76
 pixel truncation, 49, 53
 pixel-level parallelism (PLP), 19, 21, 22
 post-scaling factor, 90
 pre-scaling factor, 91, 93
 prediction mode capability (PMC), 19
 Probability State Index (pStateIdx), 126
 processing element (PE), 22, 37, 39
 profile
 baseline, 11, 85
 extended, 11, 85
 high, 11
 main, 11, 85
 PSNR, 156
 PutBit function, 130, 144

Q

QFHD, 8, 107, 125
 quantization, 86

quantization parameter (QP), 90, 152
 quantization step (Qstep), 5, 90
 quarter pixel accuracy, 74
 quarter refinement, 58, 70
 queue, 163

R

RangeLPS (rLps), 130
 RangeMPS (rMps), 130
 rangeTabLPS table, 130
 read-after-write hazard, 144
 reconfigurable architecture, 19
 reference frame, 31, 47, 49, 159
 Reference Frame Interlaced Processing (RFIP),
 50
 reference index, 73
 Reference Pixel Register Array, 47
 rem_intra_pre_mode SE, 132
 renormalization, 130
 residual, 4, 86, 89
 row-of-pixels (ROP), 119
 row-miss, 76
 run level coding (RLC), 86, 93

S

scalar multiplication, 90
 scalar quantizer, 90
 SDTV, 62
 search range, 33, 159
 search window, 31–33, 41
 seed pixel, 26
 significant coefficient flag, 93, 133
 Skip-all mode, 115, 122
 Skip-top mode, 115
 snake scan, 49
 SOC, 156
 standard definition (SD), 1, 155
 sum of absolute differences (SAD), 33,
 155
 sum of absolute transformed differences
 (SATD), 58, 59, 155, 156
 generation, 63, 68
 sum of square difference (SSD), 33
 switching FIFO, 82
 syntax element (SE), 125

T

Table Mapping Code Method, 128
 threshold, 108, 109, 111

transform

- discrete cosine (DCT), [85](#), [89](#)
 - Hadamard (HT), [89](#), [90](#)
 - inverse discrete cosine (IDCT), [92](#)
 - inverse Hadamard (IHT), [92](#)
- transIdxLPS table, [143](#)
- Truncated Unary Code Method, [127](#)
- Two-Result-Per-Cycle Edge Filter, [118](#)

U

- Unary Code Method, [127](#)

V

- variable-length coding, [125](#)
- Video Coding Experts Group (VCEG), [73](#)

W

- weighted prediction, [75](#), [82](#)

Z

- zig-zag scan, [93](#), [101](#)