RF, system and building block specifications

Performance of a front-end is determined by linearity, selectivity, noise and gain. Linearity is characterized by the input second intercept point (IIP2), input third intercept point (IIP3) and 1-dB compression point (A_{1dB}). Noise performance of a front-end is described by the noise figure (NF). IIP2, IIP3, A_{1dB} and NF are called RF specifications. In the process of front-end design, RF specifications are calculated based on system specifications. The following system specifications are used in front-end design: sensitivity at a certain bit error rate (BER), inter-modulation performance, interference performance, blocking signals and maximum input signal level.

Considering the linearity of a front-end, the third order inter-modulation products are of a particular interest. Figure A.1 shows a case when a weak wanted signal is accompanied by two strong interferers. The frequencies of the interferers $(f_1 \text{ and } f_2)$ are very close to the frequency of the wanted signal. Due to the third order inter-modulation distortion, two new components at the frequencies $2f_1 - f_2$ and $2f_2 - f_1$ are generated at the output of a front-end. They are called third-order inter-modulation (IM3) products . Since the frequencies f_1 and f_2 are very close to the frequency of the wanted signal, there is possibility that one of the IM3 products falls in the band of the wanted signal. As a consequence, the SNR will be degraded. The third-order inter-modulation distortion is described by the IIP3 [1]. A typical IIP3 plot is presented in Fig. A.2. Assuming that the amplitude of the wanted signal is denoted with A, then the amplitude of fundamental signal at the output increases in proportion to A while the amplitude of the third-order inter-modulation products at the output is proportional to the A^3 [1]. Therefore, there is an intersection point of these two curves. The x-coordinate of that point is called input third intercept point (IIP3). Specifications related to inter-modulation performance are used to calculate the IIP3 of a front-end.



Figure A.1 Degradation of a wanted signal by IM3 products



Figure A.2 Input third intercept point (*IIP*3)

The second-order inter-modulation products can also influence reception quality. Assuming that the frequencies f_1 and f_2 are very close to each other (see Fig. A.1), then due to the second-order nonlinearity a low frequency components will appear at the frequencies $f_1 - f_2$ and $f_2 - f_1$. Before conversion to the digital domain, a high frequency wanted signal has to be down-converted to a low IF. There is possibility that the second-order inter-modulation products fall in the band of the down-converted wanted signal. If that happens the SNR will be deteriorated. The second-order inter-modulation distortion is described by the input second intercept point (IIP2), which is defined in the same way as IIP3.

Inter-modulation performance can be characterized by two-tone test. The levels of both signals in the two-tone test are equal and denoted with P_s . The level of third-order

inter-modulation components, which is referred to the front-end input, is denoted with $P_{\text{IM3,in}}$. The front-end IIP3 can be calculated if P_{s} and $P_{\text{IM3,in}}$ are known [1]:

IIP3 =
$$P_{\rm s} + \frac{1}{2} (P_{\rm s} - P_{\rm IM3,in})$$
 (A.1)

In the similar way IIP2 can be expressed as a function of P_s and the level of second-order inter-modulation components referred to the front-end input ($P_{IM2,in}$):

$$IIP2 = 2P_s - P_{IM2,in} \tag{A.2}$$

Due to the nonlinearity of a front-end transfer function, the front-end gain depends on the level of an input signal. In the case of a small signal gain, harmonics are small and they can be neglected. When an input signal increases, harmonics become stronger. Due to their influence, the front-end gain starts to drop and at a certain level of an input signal it becomes equal to zero. In order to characterize this effect, RF engineers use 1 dB compression point (A_{1dB}). This is the level of an input signal at which the front-end gain drops for 1 dB compared to its small signal gain.

Specifications related to interference performance define levels of in-band interferers, while blocking performance specify levels of out-of-band interfering signals. Front-ends have to be designed in a way to handle these in-band and out-of-band interferers. Actually, specifications related to interference and blocking performance are used to determine front-end selectivity.

NF is a quantity that describes the noise added by a front-end during the signal processing. Hence, NF is defined as a ratio between SNR at the front-end input (SNR_{in}) and SNR at the front-end output (SNR_{out}).

$$NF = 10 \log \left(\frac{SNR_{in}}{SNR_{out}}\right)$$
(A.3)

The NF shows a degradation of SNR_{in} due to the additional noise added by a front-end. The linear denotation of NF is noise factor *F*.

$$F = \frac{\text{SNR}_{\text{in}}}{\text{SNR}_{\text{out}}}$$
(A.4)

In general, front-end gain is defined as a ratio between signal levels at the front-end output and front-end input. Depending which quantities are used to characterize the signals at the front-end input and output, various gain definitions can be obtained. Usually, voltage and power gain are most often used in the front-end design.

Quality of received signals at the output of the demodulator is evaluated by means of BER. The BER has to be equal or better than a maximal allowed BER (BER_{max}). BER is a function of a signal-to-noise ratio (SNR) at the input of the demodulator. Typical BER dependence on SNR is presented in Fig. A.3. So, for a required quality of reception (BER \leq BER_{max}), it is necessary to provide a SNR, which is equal or greater than the SNR that corresponds to BER_{max} (SNR_{min}).



Figure A.3 BER as a function of SNR

Sensitivity of a front-end represents a minimum signal level (P_{sens}) that can be received and demodulated with BER_{max}. This means that a front-end has to process a received signal in such way that at least SNR_{min} is provided at the input of the demodulator. Starting from (A.3) and assuming power matching between the antenna and front-end, P_{sens} can be expressed as [1]

$$P_{\text{sens}} = -174 \text{ dBm/Hz} + \text{NF} + \text{SNR}_{\text{min}} + 10 \log B$$
(A.5)

Using front-end sensitivity from system specifications and if SNR_{min} , and bandwidth (*B*) are known, then the required front-end NF can be determined.

The distance between a receiver and a base station varies. P_{sens} defines a maximal distance on which communication between a receiver and the corresponding base station can be established. When a receiver is very close to the corresponding base station, the received wanted signal is strong. P_{max} specifies a maximal level of the wanted signal at the front-end input, which a front-end has to handle. In principle, the strength of a received wanted signal is in the range from P_{sens} up to P_{max} .

Front-ends are subdivided into different building blocks (see Fig. 1.6). Building blocks in a front-end are characterized with its own NF, IIP3 and power or voltage gain. These quantities are called building block specifications. On top of that, each building block has a power budget and chip area target. According to the multi-standard front-end design flow (see Fig. 1.7), calculation of building block specifications is the last step in the system level design. When building block specifications are calculated, two important formulas are used. Noise factor of a front-end that consists of *m* cascaded stages can be expressed as [1]

$$F = F_1 + \frac{F_2 - 1}{A_{p1}} + \dots + \frac{F_m - 1}{A_{p1} \cdots A_{p(m-1)}}$$
(A.6)

 F_i and A_{pi} are the noise factor and available power gain of stage *i*. The equation (A.6) is also known as Friis formula [1]. The most important implication from Friis formula is that a noise contribution from each stage is reduced by the gain of a preceding stage. Therefore, if each stage in a front-end has a gain greater than unity, then the first few stages contribute the most to the overall noise factor of a front-end. Similarly the IIP3 of a front-end that consist of *m* cascaded stages can be approximated as [1]

$$\frac{1}{\text{IIP3}^2} \approx \frac{1}{\text{IIP3}_1^2} + \sum_{i=2}^{i=m} \frac{\prod_{n=1}^{n=i-1} A_n^2}{\text{IIP3}_i^2}$$
(A.7)

 A_n and IIP3_i are the voltage gain and input third intercept point of stage *i*. IIP3_i is expressed in V instead of dBm. Compared to Friis formula, (A.7) has an opposite implication. If each stage in a front-end has a gain greater than unity, then the linearity of last few stages in a front-end determines the overall front-end linearity.

Noise factor of a two-port network

A two-port network is presented in Fig. B.1. It is driven by a voltage source V_{in} with resistance R_s . The total noise from a two-port network is transfered to the input. It is represented by an equivalent voltage noise source $\overline{V_{in}^2}$ and an equivalent current noise source $\overline{I_{in}^2}$ [46]. The noise factor of a two-port network, with respect to the source resistance R_s , can be expressed as [1]

$$F = 1 + \frac{(V_{\rm in} + I_{\rm in}R_{\rm s})^2}{4kTR_{\rm s}}$$
(B.1)

k is the Boltzmann constant ($k = 1.38 \times 10^{-23} \text{ J/K}$) and *T* is the absolute temperature in kelvins.

The noise factor of a two-port network can be also expressed in an alternative way. The total noise voltage per unit bandwidth at the output of a two-port network is equal to

$$\overline{V_{\text{out}}^2} = \left(4kTR_{\text{s}} + \overline{(V_{\text{in}} + I_{\text{in}}R_{\text{s}})^2}\right)|G|^2 \tag{B.2}$$

G is the voltage gain, which is defined as

$$G = \frac{V_{\text{out}}}{V_{\text{in}}} \tag{B.3}$$

Multiplying both, numerator and denumerator of (B.1) with $|G|^2$ and taking into account (B.2), the noise factor of a two port network can be expressed as

$$F = \frac{\overline{V_{\text{out}}^2}}{|G|^2 4kTR_{\text{s}}} \tag{B.4}$$



Figure B.1 Two-port network

If the output referred noise voltage from the two port network is denoted with $\overline{V_{tp,out}^2} = \overline{(V_{in} + I_{in}R_s)^2} |G|^2$) then the noise factor of a two port network can be written in an another way:

$$F = 1 + \frac{V_{\rm tp,out}^2}{\left|G\right|^2 4kTR_{\rm s}} \tag{B.5}$$

С

Noise factor of a passive RF block

A passive RF block (PRFB), which is driven by the voltage source V_{in} with resistance R_s , can be represented by the Thevenin equivalent circuit (see Fig C.1). R_t is equal to the output resistance of the PRFB:

$$R_{\rm t} = R_{\rm PRFB,out} \tag{C.1}$$

 V_t is the voltage at the ouput of the PRFB (at reference point *B*) when it is unloaded:

$$V_{\rm t} = \frac{R_{\rm PRFB,in}}{R_{\rm s} + R_{\rm PRFB,in}} G_{\rm PRFB} V_{\rm in} \tag{C.2}$$

 $R_{\text{PRFB,in}}$ is the input impedance and G_{PRFF} is the voltage gain of the PRFB.

Insertion loss (L) of the PRFB is defined as the ratio between the available source power and the available power at the output of the PRFB [1]. Based on this definition L can be expressed as

$$L = \frac{V_{\rm in}^2}{V_{\rm t}^2} \frac{R_{\rm PRFB,out}}{R_{\rm s}}$$
(C.3)

Taking into account (C.2), L can be written as

$$L = \frac{1}{\left(\frac{R_{\text{PRFB,in}}}{R_{\text{s}} + R_{\text{PRFB,in}}} G_{\text{PRFB}}\right)^2} \frac{R_{\text{PRFB,out}}}{R_{\text{s}}}$$
(C.4)

In appendix B (see (B.4)) it has been shown that the noise factor of a PRFB can be calculated as

$$F_{\text{PRFB}} = \frac{V_{\text{PRFB,out}}^2}{|G|^2 4kTR_{\text{s}}} \tag{C.5}$$



Figure C.1 A passive RF block (a) Thevenin equivalent circuit for a passive RF block (b)

 $\overline{V_{\text{PRFB,out}}^2}$ is the noise voltage at the output of the PRFB. It can be expressed as

$$\overline{V_{\text{PRFB,out}}^2} = 4kTR_{\text{PRFB,out}} \left(\frac{R_{\text{d}}}{R_{\text{d}} + R_{\text{PRFB,out}}}\right)^2 \tag{C.6}$$

G is the voltage gain $(G = \frac{V_{\text{out}}}{V_{\text{in}}})$, which can be expressed as

$$G = \frac{R_{\text{PRFB,in}}}{R_{\text{s}} + R_{\text{PRFB,in}}} G_{\text{PRFB}} \frac{R_{\text{d}}}{R_{\text{d}} + R_{\text{PRFB,out}}}$$
(C.7)

Combining (C.2), (C.6), (C.7) and (C.5), the final expression for F_{PRFB} is obtained:

$$F_{\rm PRFB} = \frac{1}{\left(\frac{R_{\rm PRFB,in}}{R_{\rm s} + R_{\rm PRFB,in}} G_{\rm PRFB}\right)^2} \frac{R_{\rm PRFB,out}}{R_{\rm s}}$$
(C.8)

Comparing (C.8) with (C.4) it can be seen that

$$F_{PRFB} = L \tag{C.9}$$

Equation (C.9) shows that the noise factor of a passive RF block is equal to its insertion loss.

References

- [1] B. Razavi, RF Microelectronics, Prentice Hall, Upper Saddle River, NJ, 1998.
- [2] H. Darabi et al., "A Dual Mode 802.11b/Bluetooth Radio in 0.35 mu CMOS," IEEE International Solid State Circuits Conference (ISSCC), 2003, pp. 86–87.
- [3] M. Kuo et al., "A CMOS WLAN/GPRS Dual-Mode RF Front-End Receiver," IEEE Radio Frequency Integrated Circuit Symposium (RFIC), 2004, pp. 153–156.
- [4] Y. Kim et al., "A GSM/EGSM/DCS/PCS Direct Conversion Receiver With Integrated Synthesizer," *IEEE Radio Frequency Integrated Circuit Symposium (RFIC)*, 2004, pp. 53–56.
- [5] S. Cipriani *et al.*, "Fully Integrated Zero IF Transceiver for GPRS/GSM/DCS/PCS Application," *IEEE European Solid-State Circuits (ESSCIRC)*, 2002, pp. 439–442.
- [6] R. Magoon *et al.*, "A Single-Chip Quad-Band (850/900/1800/1900 MHz) Direct Conversion GSM/GPRS RF Transceiver with Integrated VCOs and Fractional-N Synthesizer," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 12, pp. 1710–1720, December 2002.
- [7] K. Muhammad *et al.*, "The First Fully Integrated Quad-Band GSM/GPRS Receiver in a 90-nm Digital CMOS Process," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 8, pp. 1772–1783, August 2006.
- [8] E. Song *et al.*, "A 0.25 um CMOS Quad-Band GSM RF Transceiver Using an Efficient LO Frequency Plan," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 5, pp. 1094–1106, May 2005.
- [9] K. Vavelidis *et al.*, "Dual-Band 5.15-5.35-GHz, 2.4-2.5-GHz 0.18-um CMOS Transceiver for 802.11a/b/g Wireless LAN," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 7, pp. 1180–1184, July 2004.

- [10] Z. Xu et al., "A Compact Dual-Band Direct Conversion CMOS Transceiver for 802.11a/b/g WLAN," IEEE International Solid-State Circuits Conference (ISSCC), 2005, pp. 98–586.
- [11] T. Maeda *et al.*, "A Low-Power Dual-Band Triple-Mode WLAN CMOS Transceiver," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 11, pp. 2481–2490, November 2006.
- [12] T. Manku *et al.*, "A Single Chip Direct Conversion CMOSD Transceiver for Quad-band GSM/GPRS/EDGE and WLAN with Integrated VCO's and Fractional-N Synthesizer," *IEEE Radio Frequency Integrated Circuit Symposium (RFIC)*, 2004, pp. 423–426.
- [13] A. Baschirotto *et al.*, "Baseband Analog Front-End and Digital Back-End for Reconfigurable Multi-Standard Terminals," *IEEE Circuits and Systems Magazine*, vol. 6, no. 1, pp. 8–28, 2006.
- [14] Source: http://www.3g.co.uk/PR/June2003/5493.htm.
- [15] N. Darbanian et al., "Tri-Mode Integrated Receiver for GPS, GSM 1800, and WCDMA," IEEE Radio Frequency Integrated Circuit Symposium (RFIC), 2006.
- [16] R. Castello *et al.*, "Multimode Reconfigurable Wireless Terminals: A First Step Toward Software Defined Radio," *IEEE European Solid-State Circuits (ESSCIRC)*, 2006, pp. 42–49.
- [17] A. Loke *et al.*, "Direct Conversion Radio for Digital Mobile Phones-Design Issues, Status, and Trends," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 11, pp. 2422–2435, November 2002.
- [18] A. Smolders et al., "RF SiP: The Next Wave for Wireless System Integration," IEEE Radio Frequency Integrated Circuit Symposium (RFIC), 2004, pp. 233–236.
- [19] L. Lecheminoux et al., "Advanced Design, Technology & Manufacturing for High Volume and Low Cost Production," *IEEE Electronics Manufacturing Technology* (*IEMT*) Symposium, 2003, pp. 255–260.
- [20] V. Vidojkovic *et al.*, "Receiver Planning for a 1.8-2.5 GHz Multi-Standard Front-End," *IEEE European Conference on Circuit Theory and Design (ECCTD)*, 2003, vol. 2, pp. 189–192.
- [21] F. Vessal *et al.*, "An 8-Bit 2-Gsamples/s Folding-Interpolating Analog-to-Digital Converter in SiGE Technology," *IEEE Journal of Solid State Circuits*, vol. 39, no. 1, pp. 238–241, January 2004.
- [22] W. An et al., "An 8-Bit 1-Gsamples/s Folding-Interpolating Analog-to-Digital Converter," European Solid-State Circuit Conference (ESSCIRC), 2000, pp. 200–203.

- [23] O. Eynde *et al.*, "A Fully-Integrated Zero-IF DECT Transceiver," *IEEE International Solid State Circuits Conference (ISSCC)*, 2000, pp. 138–139.
- [24] G. Dehng *et al.*, "A Single-Chip RF Transceiver for Quad-Band GSM/GPRS Applications," *IEEE Radio Frequency Integrated Circuit Symposium (RFIC)*, 2004, pp. 427–430.
- [25] A. Leeuwenburgh et al., "A 1.9 GHz Fully Integrated CMOS DECT Transceiver," IEEE International Solid-State Circuits Conference (ISSCC), 2003, pp. 450–451.
- [26] R. van de Plassche, *Integrated Analog to Digital and Digital to Analog Converters*, Kluwer Academic Publishers, Boston/Dordrecht/London, 1994.
- [27] R. Walden *et al.*, "Analog-to-Digital Converter Survey and Analysis," *IEEE Journal of Solid State Circuits*, vol. 17, no. 4, pp. 539–550, April 1999.
- [28] J. Crols et al., CMOS Wireless Transceiver Design, Kluwer, Boston/Dordrecht/ London, 1997.
- [29] M. Valkama *et al.*, "Advanced Methods for I/Q Imbalance Compensation in Communications Receivers," *IEEE Transactions on Signal Processing*, vol. 49, no. 10, pp. 2335–2344, October 2001.
- [30] L. Der et al., "A 2-GHz CMOS Image-Reject Receiver With LMS Calibration," IEEE Journal of Solid State Circuits, vol. 38, no. 2, pp. 167–175, February 2003.
- [31] ETSI DECT Standard, TBR6-Technical Basis for Regulation, 1999.
- [32] T. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, Cambridge CB2 2RU, UK, 1998.
- [33] J. Crols, et al., "Low-IF Topologies for High performance Analog Front Ends of Fully Integrated Receivers," *IEEE Transactions on Circuit and Systems-II: Analog* and Digital Signal Processing, vol. 45, no. 3, pp. 269–282, 1998.
- [34] J. Tang, *High-Frequency Oscillator Design for Integrated Transceivers*, Ph.D. thesis, Eindhoven University of Technology, 2002.
- [35] A. Zjajo et al., "A 1.8V 100mW 12bits 80Msamples/s Two-step ADC in 0.18-μm CMOS," European Solid-State Circuit Conference (ESSCIRC), 2003, pp. 241–244.
- [36] A. Loloee *et al.*, "A 12bits 80MSs Pipelined ADC Core with 190mW Consumption from 3 V in 0.18-μm CMOS," *European Solid-State Circuit Conference (ESSCIRC)*, 2002, pp. 467–469.
- [37] P. Baltus, *Minimum Power Design of RF Front Ends*, Ph.D. thesis, Eindhoven University of Technology, 2004.

- [38] J. Crols *et al.*, "An Analog Integrated Polyphase Filter for a High Performance Low-IF Receiver," *Symposium on VLSI Circuits*, 1995, pp. 87–89.
- [39] H. Darabi et al., "Noise in RF-CMOS Mixers: A Simple Physical Model," IEEE Journal of Solid State Circuits, vol. 35, no. 1, pp. 15–25, 2000.
- [40] F. Behbahani *et al.*, "CMOS Mixers and Polyphase Filters for Large Image Rejection," *IEEE Journal of Solid State Circuits*, vol. 36, no. 6, pp. 873–887, 2001.
- [41] B. Shi et al., "A 57-dB Band Rejection CMOS Gm-C Polyphase Filter with Automatic Frequency Tuning for Bluetooth," *International Symposium on Circuits and Systems (ISCAS)*, 2002, vol 5, pp. 169–172.
- [42] H. Bergveld *et al.*, "A Low-Power Highly-Digitized Receiver for 2.4-GHz-Band GFSK Applications," *IEEE Radio Frequency Integrated Circuit Symposium (RFIC)*, New York, NY 10020, 2004, pp. 347–350.
- [43] J. Chabloz et al., "A Novel I/Q Mismatch Compensation Scheme for a Low-IF Receiver Front-End," International Symposium on Circuits and Systems (ISCAS), 2004, vol 4, pp. 453–456.
- [44] S. Galal *et al.*, "RC Sequence Asymmetric Networks for RF Integrated Transceivers," *IEEE Transactions on Circuits and Systems-II:Analog and Digital Signal Processing*, vol. 47, no. 1, pp. 18–27, 2000.
- [45] M. Gingell *et al.*, "Single Sideband Modulation Using Sequence Asymmetric Polyphase Networks," *Electrical Communications*, vol. 48, pp. 21–25, 1973.
- [46] P. Gray et al., Analysis and Design of Analog Integrated Circuits, John Wiley & Sons, New York, 2001.
- [47] B. Razavi, "CMOS RF Receiver Design for Wireless LAN Applications," *Radio and Wireless Conference (RAWCON)*, 1999, pp. 275–280.
- [48] TBR6-Technical Basis for Regulation, ETSI DECT Standard, 1999.
- [49] Specifications for the Bluetooth System (version 1.1), www.bluetooth.com, 2001.
- [50] S. Samadin *et al.*, "Demodulators for a Zero-IF Bluetooth receiver," *IEEE Journal of Solid State Circuits*, vol. 38, no. 8, pp. 1393–1396, August 2003.
- [51] Min-Jung Kim et al., "An 11b 70 MHz 1.2 mm2 49mW 0.18 um CMOS ADC with on.chip Current/Voltage References," European Solid-State Circuits Conference (ESSCIRC), 2002 pp. 463–466.
- [52] C. Debono et al., "A 900 MHz, 0.9 V Low-Power CMOS Down-conversion Mixer," IEEE Custom Integrated Circuit Conference (CICC), 2001, pp. 527–530.
- [53] P. Sullivan *et al.*, "Low Voltage Performance of a Microwave CMOS Gilbert Cell Mixer," *IEEE Journal of Solid State Circuits*, vol. 32, no. 7, pp. 1151–1155, July 1997.

- [54] V. Vidojkovic *et al.*, "Mixer Topology Selection for a 1.8-2.5 GHz Multi-Standard Front-End in 0.18 um CMOS," *International Symposium on Circuits and Systems* (ISCAS), 2003, vol 2, pp. 300–303.
- [55] J. Rudell *et al.*, "1.9-GHz Wide-Band IF Double Conversion CMOS Receiver for Cordless Telephone Applications," *IEEE Journal of Solid State Circuits*, vol. 32, no. 12, pp. 2071–2087, December 1997.
- [56] B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, New York, NY 10020, 2001.
- [57] A. Karanicolas, et al., "A 2.7-V 900-MHz CMOS LNA and Mixer," IEEE Journal of Solid State Circuits, vol. 31, no. 12, pp. 1939–1944, December 1996.
- [58] C. Hermann et al., "A 0.6V 1.6mW Transformer based 2.5GHz Downconversion Mixer with 5.4dB Gain and -2.8dBm IIP3 in 0.13 um CMOS," Radio Frequency Integrated Circuit Symposium (RFIC), 2004, pp. 35–38.
- [59] E. Klumperink, et al., "A CMOS Switched Transconductor Mixer," IEEE Journal of Solid State Circuits, vol. 39, no. 8, pp. 1231–1240, August 2004.
- [60] F. Behbahani, *et al.*, "CMOS Mixers and Polyphase Filters for Large Image Rejection," *IEEE Journal of Solid State Circuits*, vol. 36, no. 6, pp. 873–887, 2001.
- [61] D. Shaeffer, et al., "A 1.5-V, 1.5 GHz CMOS Low Noise Amplifier," IEEE Journal of Solid State Circuits, vol. 32, no. 5, pp. 745–759, 1997.
- [62] F. Bruccoleri, et al., "Generating All Two-MOS-Transistors Amplifiers Leads to New Wide-Band LNAs," *IEEE Journal of Solid State Circuits*, vol. 36, no. 7, pp. 1032–1040, 2001.
- [63] H. Hashemi, *et al.*, "Concurrent Multiband Low-Noise Amplifiers-Theory, Design and Applications," IEEE Transactions on Microwave Theory and Techniques, vol. 50, no. 1, pp. 288–301, 2002.
- [64] G. Gramegna, et al., "A Sub-1-dB NF ±-kV ESD-Protected 900-MHz CMOS LNA," *IEEE Journal of Solid State Circuits*, vol. 36, no. 7, pp. 1010–1017, 2001.
- [65] J. Rudell, et al., "1.9-GHz Wide-Band IF Double Conversion CMOS Receiver for Cordless Telephone Applications," *IEEE Journal of Solid State Circuits*, vol. 32, no. 12, pp. 2071–2087, 1997.
- [66] S. Kim, et al., "Novel High-Q Bondwire Inductors for RF and Microwave Monolithic Integrated Circuits," *Microwave Symposium Digest*, vol. 4, pp. 1621–1624, 1999.
- [67] W. Hioe, et al., "0.18-μm CMOS Bluetooth Analog Receiver With -88-dBm Sensitivity," *IEEE Journal of Solid State Circuits*, vol. 39, no. 2, pp. 374–377, 2004.

ANALOG CIRCUITS AND SIGNAL PROCESSING SERIES

Consulting Editor: Mohammed Ismail. Ohio State University

Titles in Series: Continued from page ii CALIBRATION TECHNIQUES IN NYQUIST A/D CONVERTERS van der Ploeg, H., Nauta, B. Vol. 873, ISBN 1-4020-4634-0 ADAPTIVE TECHNIQUES FOR MIXED SIGNAL SYSTEM ON CHIP Fayed, A., Ismail, M. Vol. 872, ISBN 0-387-32154-3 WIDE-BANDWIDTH HIGH-DYNAMIC RANGE D/A CONVERTERS Doris, Konstantinos, van Roermund, Arthur, Leenaerts, Domine Vol. 871 ISBN: 0-387-30415-0 METHODOLOGY FOR THE DIGITAL CALIBRATION OF ANALOG CIRCUITS AND SYSTEMS: WITH CASE STUDIES Pastre, Marc, Kayal, Maher Vol. 870, ISBN: 1-4020-4252-3 HIGH-SPEED PHOTODIODES IN STANDARD CMOS TECHNOLOGY Radovanovic, Sasa, Annema, Anne-Johan, Nauta, Bram Vol. 869, ISBN: 0-387-28591-1