CHAPTER 9 *Conclusions*

Short-distance fiber-optic chip-to-chip links provide next-generation processors with the I/O bandwidth required to fully exploit their immense data processing throughput. Economic viability however asks for a low-cost and low-overhead implementation, which can be optimally satisfied by fully integrated silicon receivers. Throughout this book, the reader has been shown how to address the upcoming challenges and trade-offs in the design of such CMOS-integrated receivers.

Knowing the substantial bandwidth available in the optical domain and remembering that the electrical properties of the transmitter and receiver ultimately limit the data rates of optical communication links, it is tempting to push the electro-optical interfaces as far as possible inside the computing parts of the processors. While optical computing seems destined to remain a far-out technology for some time to come, optical networking has become an immovable cornerstone of the connected world. As a result, it makes perfect sense to think about integration of optical links on silicon processors to replace global connections in the large multicore arrangements currently planned by the major manufacturers. Of course, miniaturization and CMOS process compatibility of optical add-drop multiplexers, waveguides and silicon transmitters and receivers represent major challenges to the engineering community, but the computing power leveraged by such reconfigurable on-chip optical networks combined with large-scale multiprocessor arrays would represent a quantum leap in manufacturable processing power.

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