

Index

- Adaptive body-bias, 25, 45, 77
- Adaptive voltage scaling, 25
- Aging, 87, 151
 - negative bias temperature instability (NBTI), 11
- Asynchronous design, 230
 - bundled data, 230
 - dual-rail, 231
- Asynchronous latch controller, 240
- Body-bias, 2, 12, 20
 - adaptive, 4, 25, 45, 77
 - controller, 88
 - forward, 27, 60
 - reverse, 27, 55
- Canary circuits, 179
- Clock generation, 138
- Clocking
 - jitter, 150
 - skew, 150, 274
- Control loop, 199
- Critical path, 145, 210
- DC-DC, 108
 - inductor-based, 109
 - switched-cap, 110
- Device sizing, 98
- Drain induced barrier lowering (DIBL), 17, 50
- Dynamic voltage scaling (DVS), 26, 50, 95, 123, 126, 176
- Error correction coding, 106, 277
- Error detection, 182
- Frequency island, 207–208
- Frequency optimization, 33
- Globally asynchronous, locally synchronous (GALS), 208
- Guardbands, 299
- Hardware and software control, 68
- In-situ monitor, 181
- Leakage current
 - gate, 2, 17, 50
 - gate edge diode leakage (GEDL), 18
 - gate induced diode leakage (GIDL), 20, 39
 - subthreshold, 2, 17, 50
- Leakage current monitor, 56
- Low-dropout (LDO), 109
- Manufacturing test, 272, 279
 - ATPG, 280
 - clock de-skew, 288
 - power management, 289
 - wafer sort, 280
- Microprocessor, 121
- Minimum energy tracking, 112
- Negative bias temperature instability (NBTI), 11
- Noise, 145
- Operating system control (OS), 70
- Performance monitor, 128
- PLL, 87, 138
- Power monitor, 279
- Power optimization, 33
- Process variation, 41, 79, 145, 149, 175, 207, 210, 267
 - die-to-die, 79

Random dopant fluctuations, 11
Ring oscillator, 33

Shadow latch, 187
Short-channel effect, 59

SRAM, 101, 134, 249
 active sleep, 260
 bias generator, 262
 passive sleep, 261
 read assist, 257
 reliability, 267
 replica path, 258
 soft errors, 267
 subthreshold, 107
 timing, 257
 write assist, 253

Static noise margin (SNM), 134
 flip-flops, 97
 read, 104, 250
 SRAM, 104
 write, 250

Sub-threshold CMOS, 97
Supply voltage variation, 150, 177

Technology scaling, 1, 26, 75, 175
Temperature variation, 7, 57, 150,
 177, 207, 217
Threshold-voltage variation, 13

Ultra dynamic voltage scaling, 95

Variable channel-length, 5
Variable frequency scaling, 207
Variable threshold CMOS
 (VTCMOS), 55

Voltage/frequency hopping, 51
Voltage controlled oscillator
 (VCO), 280

Voltage regulator, 278
Voltage scaling, 2
 adaptive, 25

Continued from page ii

Abstraction Refinement for Large Scale Model Checking
Chao Wang, Gary D. Hachtel, and Fabio Somenzi
ISBN 978-0-387-28594-2, 2006

A Practical Introduction to PSL
Cindy Eisner and Dana Fisman
ISBN 978-0-387-35313-5, 2006

Thermal and Power Management of Integrated Systems
Arman Vassighi and Manoj Sachdev
ISBN 978-0-387-25762-4, 2006

Leakage in Nanometer CMOS Technologies
Siva G. Narendra and Anantha Chandrakasan
ISBN 978-0-387-25737-2, 2005

Statistical Analysis and Optimization for VLSI: Timing and Power
Ashish Srivastava, Dennis Sylvester, and David Blaauw
ISBN 978-0-387-26049-9, 2005