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Another inexpensive, efficient, solid state shock scrambler

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This paper describes an inexpensive, solid state shock scrambler. The circuit employs TTL logic and mercury-wetted relays for quiet, reliable operation. The unit can control shock presentation to 16 grids and operates with an efficiency of 50%; for example, on any given clock pulse, 50% of the grids are positive and the other 50%, negative.

When shock of any significant duration or frequency of presentation is employed in animal experiments, it is necessary to change the polarity of shock to the grid floor. Brush (1967) advocated the use of two criteria of efficiency in the design of shock scramblers: "1) Each pair of grid bars should be of opposite polarity equally often, and 2) the frequency of opposite polarity in each pair should be maximized; i.e., approach a limit of 50% of the time" (p. 393). This paper presents a simple modification of the shock scrambler described by Graefe and Pisacreta (1977). Their design is inefficient, since only one grid is "hot" with respect to the others on any given clock pulse. Specifically, since the circuit switches shock to one grid at a time while the others are off, the efficiency for 16 grids is 6.25%. Efficiency can be increased by decreasing the number of grids, but in most situations that is not a practical solution. The primary advantage of the modification is an increase from 6.25% to the optimal level of 50%, since half of the grids are always on while the others remain off. Regardless of the number of grids employed, the efficiency remains at the optimal 50%.

As in the Graefe and Pisacreta (1977) design, a clock pulse drives a 4-bit counter (SN7493), which drives a 4-to-16-line decoder (SN74154). The increase in efficiency comes from having each bit of the SN74154 operate inputs to eight different gates (SN7430), with one gate required for each grid. The eight input lines of the gate are tied to a selected set of 8 of the 16 bits of the 74154, and the output line of each gate drives a peripheral driver, thus switching the relay to the normally open position. As the 16-line decoder switches through Bits 0-15, the individual bits go to ground. When the decoder produces a ground tied to an input of a gate, the output of the gate will go to 5 V, thereby switching the relay to the normally closed position. Since each bit of the 16-line decoder is tied to inputs of eight different gates, the activation of each bit provides ground to eight of the peripheral drivers; the other eight, which are not tied to that particular bit, will be at 5 V. Thus, on each clock pulse to the 74154, the relay is in the normally closed position for the other half. Rather than each of the 16 bits of the 74154 driving an individual relay, each of the 16 bits activates a pattern of shock with half of the grids on and half off. On each clock pulse, another set of half of the grids are on while the other half are off. With this arrangement, it is possible to present a repeating set of 16 different patterns of shock.

Figure 1 presents a schematic of the suggested modification. Only the wiring diagram for Grid 1 is shown, to simplify the figure. The wiring connections for the other grids can be determined from Table 1. Several additional points about Figure 1 are in order. First, the clock pulse input has not been given more detail because TTL-compatible clock pulse units are fairly common in laboratories and can be utilized to provide a clock pulse for the scrambler. If one is not available, the pulse-generating circuit described by Graefe and Pisacreta (1977) can be utilized. Second, the reset pins (18 and 19) of the 74154 should be grounded. In this diagram they are permanently grounded, which means that the scrambler will operate whenever power is applied to the unit. Alternatively, the clock pulse can be gated with a 7476 flip-flop, as described by Graefe and Pisacreta, in order to switch on the unit. Third, the eight inputs of the 7430 were drawn to Bits 2, 3, 6, 7, 8, 9, 10, and 14 in a fashion to make the figure as simple as possible. As long as the eight inputs are wired to those 8 bits of the 74154, the order is irrelevant, since the grounding of any of the eight inputs will cause the output of the gate to go to 5 V, thereby turning off the peripheral relay driver. Fourth, in Figure 1, the shock-supply voltage is connected with the normally open contact to positive and the normally closed contact of the minus side of the shocker. Since the sequence given in Table 1 is symmetrical, the polarity of wiring on the relay contacts is not critical.

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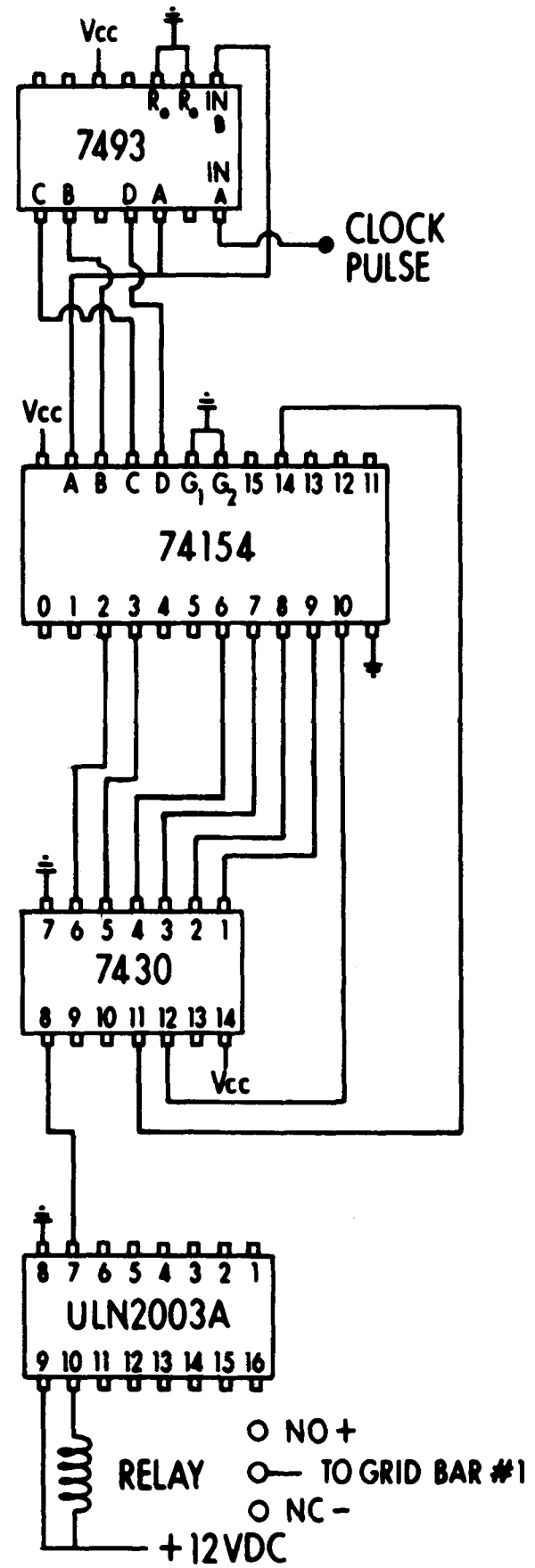

Figure 1. A schematic of the basic drive circuit. Complete wiring is shown for only the first grid bar.

Table 1
Wiring List for the 74154 to the Individual Grids to Yield the Pattern Specified in Table 2

74154 Bit	Grid Number
0	2, 4, 5, 6, 7, 10, 13, 14
1	2, 5, 10, 11, 12, 14, 15, 16
2	1, 3, 4, 6, 8, 10, 11, 15
3	1, 2, 4, 5, 7, 9, 13, 16
4	3, 6, 7, 9, 10, 11, 13, 15
5	2, 3, 6, 8, 9, 10, 12, 14
6	1, 4, 6, 11, 12, 13, 14, 16
7	1, 3, 5, 7, 10, 12, 14, 16
8	1, 2, 3, 6, 9, 14, 15, 16
9	1, 4, 7, 8, 9, 10, 12, 13
10	1, 2, 5, 8, 10, 12, 13, 15
11	2, 4, 6, 7, 8, 11, 13, 14
12	3, 5, 8, 9, 11, 13, 14, 16
13	3, 4, 6, 9, 11, 12, 15, 16
14	1, 2, 5, 7, 8, 9, 12, 15
15	3, 4, 5, 7, 8, 11, 15, 16

Since bits of the 74154 activate patterns of shock, rather than individual grids, any number of grids up to 16 can be employed and wired to give 50% efficiency. Table 1 was devised for 16 grids with the following criteria: First, on each clock pulse, eight grids are on and eight are off. Second, during the 16-bit cycle of the 74154, each grid is on eight times and off eight times. Third, an effort is made to maximize each combination of grid pairs at approximately 50% efficiency (and pair of grids being of opposite polarity for eight of the 16 patterns). The wiring connections given in Table 1 satisfy the first criteria. Table 2 presents the half-matrix for the combination of each grid with every other grid and the average efficiency for each grid. From the view of efficiency expressed by Brush (1967) (any combination of grids operating at 50% efficiency), the ideal matrix would consist of eight in each cell. While each grid has an efficiency of 50% (8.5 out of 16), there is some variability, ranging from 6 to 14 of 16. Thus, the minimum efficiency for any given combination is 6 of 16, or 37.5%, which occurs for 21 combinations (17.5%). In 99 cases (82.5%), the pairs operate at an efficiency of 50% or greater. Of course, alternative patterns can be formulated with any number of grids and criteria and the gates wired accordingly. Since the bits represent the presentation of a pattern of shock, any number of grids can be employed. However, without the use of additional components, the use of the 16-line decoder and eight input gates dictate a maximum of 16 grids with the eight inputs on each gate tied to a selected set of eight of the 16 bits of the 74154. Beyond 16 grids, it is easier to have some relays control shock to more than one grid.

Using the components described by Graefe and Pisacreta (1977), the modification requires only the addition of 16 gates (SN7430), which cost approximately 15 cents each from surplus outlets. A substantial reduction in cost can be achieved by employing a peripheral driver (Texas Instrument ULN2003A) that has seven

Table 2
Frequency of Opposite Polarity for All Possible Pairs of Grids During 16-Bit Cycle

Grid	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Mean Efficiency
1		8	10	8	8	10	8	8	8	8	12	6	8	10	8	8	8.53
2			12	10	6	8	8	8	8	8	12	8	8	6	8	10	8.53
3				10	10	6	10	8	6	8	6	10	12	8	6	6	8.53
4					10	6	6	8	10	10	6	10	6	10	10	8	8.53
5						14	6	8	10	8	10	8	8	8	8	6	8.53
6							10	10	8	8	6	10	8	6	8	10	8.53
7								8	8	8	10	10	6	10	10	10	8.53
8									8	8	8	8	8	10	8	12	8.53
9										10	10	8	8	10	8	8	8.53
10											10	6	8	8	8	12	8.53
11												10	8	8	6	6	8.53
12													10	8	8	8	8.53
13														8	12	10	8.53
14															12	6	8.53
15																8	8.53
16																	8.53

drivers per package at a cost of 85 cents each. Thus, instead of $15-$20 for individual transistor driver networks, the cost is reduced to less than $3, since only three integrated circuits are required per scrambler. In addition, a 12-V mercury-wetted relay (Walach 5504-11011) can be purchased from Poly Paks[1] for $2 each, which reduces the cost of the 16 relays to $32. The total cost of the unit can be reduced to less than $40 minus power supplies and packaging.

As in the Graefe and Pisacreta (1977) design, an independent relay is employed between the shock source and the scrambler in order to control the presentation of shock to the grids. If multiple boxes are to be run, the most economical approach involves the basic circuit driving several sets of relays that scramble shock in separate boxes. With the scrambler continuously running for all chambers, shock can be independently activated to each chamber by means of the shock relay to each set of grid relays. One advantage of the increased efficiency is the ability to run the scrambler with a relatively slow clock pulse, thus prolonging the life of the relays.

REFERENCES

BRUSH, F. R. An efficient, inexpensive relay grid scrambler for multiple boxes. *Journal of the Experimental Analysis of Behavior*, 1967, **10**, 393-394.

GRAEFE, J., & PISACRETA, R. An integrated circuit shock scrambler. *Behavior Research Methods & Instrumentation*, 1977, **9**, 499-500.

NOTE

1. Poly Paks, P.O. Box 942, South Lynnfield, Massachusetts 01941.

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