Behavior Research Methods & Instrumentation
1976, Vol. 8 (3), 299-301

A computer-compatible multichannel event counting and digital recording system

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An inexpensive multichannel event counting digital recording system has been designed for compatibility with automated data analysis equipment. For as many as 16 channels, events are simultaneously summed over preselected repetitive time intervals and recorded. Each data entry is marked with the time of day and a code identifying each channel's data. The data is formated to be computer compatible and is logged on inexpensive readily available digital magnetic tape cassettes.

There are various types of event recorders ranging in complexity from simple manual counters to sophisticated digital computers dedicated to logging information associated with specific functions. Between these extremes are single-channel electromechanical counters and multichannel electronic counters with illuminescent or printed paper tape readout. The event counting and digital recording system described in this report is intended to fill the gap between these latter devices and dedicated computer systems. It does so at a modest cost (approximately $1,500) and retains compatibility with digital computers for further data reduction.

This system can accommodate up to 16 event counters. The output, in serial digital format, is recorded on a magnetic tape cassette. Events are summed over a switch selectable time interval that can range between 1 and 99 min. Operation is continuous, that is, at the end of the specified interval, the counters are automatically reset and a new summation interval begins. Every channel can record up to 9,999 events during each interval, at the end of which, the time of day, in 24-h format, the channel identifiers and their respective data are recorded.

To facilitate playback and transfer of data, two transistor-transistor-logic (TTL) compatible output buses are provided. One bus is in parallel with the tape recorder's input, it is for on-line monitoring of recorded data. The other bus originating at the recorder's output allows playback of data to a teletype, computer, or other device. A numeric light-emitting diode (LED) visual display is incorporated to display the time of day. The system is housed in a metal cabinet measuring 44 x 27 x 14 cm and weighing 1.5 kg. It is powered by 115 V ac at 60 Hz.

SYSTEM DESCRIPTION

Most of the electronic circuitry is constructed with complementary-metal-oxide-semiconductor (CMOS) integrated circuits (IC), much of this being of the large-scale-integrated (LSI) type (Note 1). The cassette recorder is an original equipment manufacture (OEM) unit (Note 2). This recorder registers incrementally on standard Phillips certified tape cassettes using complementary NRZI encoding. The recording density is 40 characters per inch (8-bit characters), and the storage capacity of one cassette is 144,000 characters. A pushbutton switch initiates cassette rewind which is automatically terminated when the cassette is completely rewound.

In addition to the cassette recorder, cabinet, and clock display, the unit consists of two power supplies (12 and 5 V dc), printed circuit boards, and a wire-wrapped backplane to interconnect the printed circuit boards (Note 3). Figure 1 is a block diagram delineating functional blocks of the circuitry and outlining their interconnection. The heavier lines indicate the flow of information logged on the cassette recorder. This information consists of the sum of events for each channel, the channel identifying Letters A through P, and the time of day. The slashes on the lines and the numbers above them indicate the actual number of connections each line represents. Lines which have no slash indicate a single connection.

Each counter printed circuit board contains two event counters. Comprising each counter is an accumulator, latch-buffer, binary-coded-decimal (BCD) decoder, and multiplexing circuitry for sequentially outputting 4 BCD digits (10^0, 10^1, 10^2, 10^3) presented on a four-line data bus (one line for each bit: 2^0, 2^1, 2^2, 2^3). There are four digit-strobe output lines identifying which BCD digit is available at the counter's output at any given time.

When recording data, the contents of each counter are sequentially selected (from Event Counter A through Event Counter P) and forwarded to the "data or time-identifier selector" (DTIS). The time of day and channel identifier travel towards the DTIS along a different route.

The real-time clock uses the line frequency (60 Hz) as a time base. It also has a 4-decimal-digit

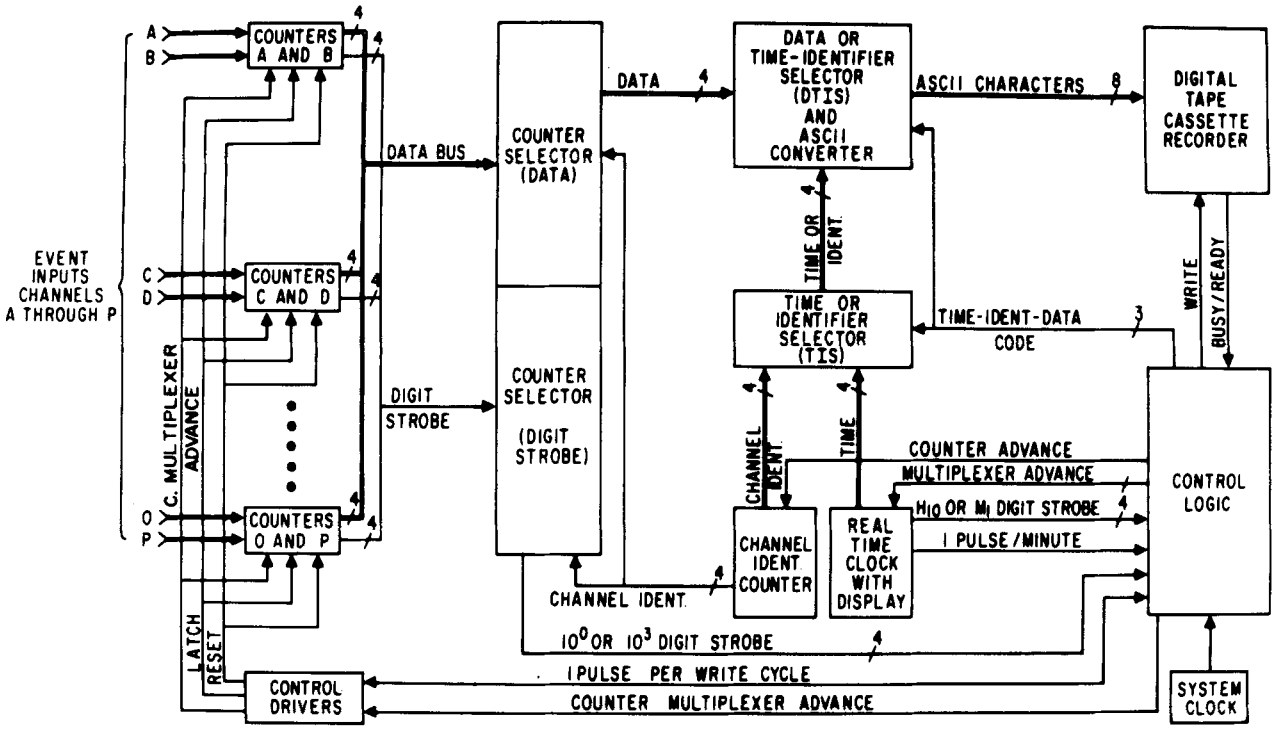

Figure 1. Functional block diagram.

multiplexed BCD output. The channel identifying counter counts from 1 to 20 in octal. This provides the five low-order bits of the ASCII code for the Letters A through P, respectively. For example, the binary code for the number 07 is 00111 which is the same as the five low-order bits of the ASCII code for the Letter G (1000111). These numbers ($1\text{-}20_8$) and their corresponding letters (A-P) each identifying one of the 16 event counters.

The multiplexed output of the real-time clock and the output of the channel identifying counter proceed to the "time or identifier selector" (TIS). From this the time or the channel identifier are available to the DTIS.

The control logic supervises a sequence of events which causes information for each write cycle to be logged by the recorder in the proper order. At the commencement of a write cycle, the sums of the events for each channel are transferred into latch-buffers and the counters are cleared. This is done by the control logic via the control drivers. The control logic contains two 10-position thumbwheel switches with BCD outputs. The user sets these switches to represent the number of minutes in the event-summating interval. The setting of these switches are read by an up-counter in the control logic. This counter is incremented once for each pulse received along the one pulse/min line from the real-time clock. When the contents of this counter are equal to the switch value, a write cycle begins.

The order in which information is recorded is as follows:

Time of day
A
Channel A's event summation
B
Channel B's event summation
.
.
.
.
P
Channel P's event summation.

At the beginning of a write cycle, the control logic determines if the multiplexed output of the real-time clock is the hours_{10} (H_{10}) digit. If not, it gates pulses from the system clock to the real-time clock multiplexer's circuitry until the H_{10} digit is present at the real-time clock's output. Under supervision of the control logic, the TIS gates the four BCD lines from the real-time clock to the DTIS. This selector, again via the control logic, gates the time signal to the ASCII converter which converts the BCD H_{10} information into 8-bit ASCII code with parity and forwards this, in 8-bit parallel format, to the input of the cassette recorder. At this time the control logic gates one system clock pulse along the write line to the recorder which writes the H_{10} character and then informs the control logic via the busy/ready line that it is through writing this character

and is ready for the next. The control logic will now gate one system clock pulse to the real-time clock's multiplexer, instructing it to output the $hours_1$ (H_1) digit. This digit and the remaining two time digits ($minutes_{10}$ and $minutes_1$) are recorded in a manner similar to that for recording the H_{10} digit.

At this time, the control logic switches the time-ident-data code from time to ident, indicating that an identifier will be written. This instructs the TIS to gate the output lines from the channel identifying counter, set to indicate "A," to the DTIS. The identifier information (A) passing through this selector is then converted to ASCII code and is recorded.

The control logic switches the time-ident-data code from ident to data. This gates event summation data from Channel A through the DTIS and ASCII converter to the recorder where it is logged. This data consists of four multiplexed decimal digits and is recorded in a fashion analogous to that for recording the time; that is, the 10^3 digit is recorded first followed by the 10^2, 10^1, and 10^0 digits. The multiplexer advance line from the control logic causes these characters to be presented in this order.

The time-ident-data code is switched back to ident. The channel identifying counter is incremented via the counter advance line to indicate "B." This character (B) is now recorded followed by the recording of Channel B's event summation data. The remaining channel identifiers and their respective data are then recorded in the same manner. At this point, the write cycle is terminated. Data is recorded incrementally at the rate of 40 char/sec; thus, a write cycle for 16 event counters is slightly longer than 2 sec.

APPLICATION

This system can be used to record occurrences of various events that are suitably detected. The input required to signal the occurrence of an event is a square wave of step levels 0 V dc and 8 to 12 V dc. Frequency response of the counters is 0 to 250 kHz. The tape cassette serves the function of communicating to data analysis equipment and also provides a viable data storage media.

The event counting and digital recording system is presently being used in conjunction with human motor activity monitoring instrumentation (McPartland, Foster, Kupfer, & Weiss, in press) and a Digital Equipment Corporation PDP-11/40 computer. The input of each channel is a series of square waves, each square wave corresponding to a physical movement of the subject monitored by that channel. Connections are made from the two 10-line parallel data output buses to DR11-C interfaces on the PDP-11/40 computer (Note 4). Assembly language (Macro-11) software has been written for this computer which enables data to be displayed by the computer while it is being recorded, and also allows the cassette tape to be played back by the recorder under computer control. The cassette can also be replayed by any other Phillips-type digital tape cassette playback transport using NRZI encoding.

REFERENCE NOTES

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2. Memodyne Corporation, *Technical Manual 100 Series Tape Transports and Recording Systems*, Memodyne Corporation, Newton Upper Falls, Massachusetts, 1974.

3. The circuit diagram is too extensive for inclusion. Arrangements for obtaining the diagram may be made with the authors.

4. Digital Equipment Corporation, *PDP-11 Peripherals Handbook*. Digital Equipment Corporation, Maynard, Massachusetts, 1975.

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(Received for publication September 19, 1975; revision received November 18, 1975.)