# A strain-gauge conditioner/analog-to-digital converter for acquisition of multiple analog signals

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Circuitry is described that allows the interfacing of a strain-gauge transducer with a laboratory microprocessor system. The analog processing system includes a high-stability, low-noise strain-gauge conditioning amplifier, monolithic active filtering, and high-speed analog-to-digital (A/D) conversion circuitry with 8-bit resolution and 10-microsec conversion period. A self-test circuit that allows off-line calibration and on-line monitoring of ongoing A/D conversion is included. Tristate converter outputs allow paralleled channel sampling without analog multiplexing or I/O port redundancy. Usage of the standard configuration in assessment of operant response dynamics in behavioral pharmacology is discussed, as well as modification of the proposed circuitry for generalized processing of psychophysiological and other analog signals found in psychological experimentation.

Following the lead of Notterman and Mintz (1965), Fowler (1974) and Fowler and Leberer (1977) have described a minicomputer system for recording the "dynamic" properties of operant responses. These intensitive response measures are peak force of response, response duration, response effort (the time integral of force), and interresponse time; these measures are recorded in addition to the usual measure of operant response rate. Such multiple measures have been useful in characterizing the effects of both pharmacological agents (Ford, Fowler, & Nail, 1979; Fowler, Filewich, & Leberer, 1977; Fowler & Price, 1978) and some types of brain damage (Price & Fowler, in press). However, one limitation of the system as described by Fowler and his colleagues is the cost of the circuitry required to computer interface the force transducers that are used as the operant manipulanda. Interfacing of each transducer necessitates the use of a strain-gauge amplifier (or equivalent) and an analog-to-digital (A/D) converter. The strain-gauge amplifier and A/D converter circuitry proposed in this paper considerably reduce the interfacing cost per transducer.<sup>1</sup> Additionally, the present circuitry was designed to provide flexibility, so that all or parts of the system may be customized for computer processing of other types of analog signals commonly measured in psychophysiological experimentation (e.g., Fridlund, Fowler, & Pritchard, 1980).

A block diagram of the proposed circuitry is shown in Figure 1. The transducer is used as a silent, nearly isometric, force-sensing manipulandum. The low-level force-proportional voltage from the transducer is amplified to a -10- to +10-V signal by the amplifier module. The active filter module contains a 60-Hz notch filter and a 180-Hz low-pass filter. The notch filter excludes line interference, and the low-pass filter reduces noise due to the resonant frequency of the transducer. The A/D converter module digitizes the force-proportional analog voltage for use by the host computer; the selftest module permits off-line calibration and/or on- or off-line monitoring of the A/D output of any specified converter channel.

## PRINCIPLES OF OPERATION

## Force Transducer

The LVDT force transducer employed in the system described by Fowler and his colleagues is no longer commercially available. The Grass Model FT.03 forcedisplacement transducer was chosen as a substitute. This transducer uses four bonded strain gauges that form a bridge circuit that measures the strain on a cantilever beam induced by an applied force. Although the FT.03 transducer was originally developed to measure contractions of muscle fibers of cats, it offers several advantages that make it suitable for many other applications. The transducer provides four working-force ranges (selectable by interchanging sets of springs provided), each capable of measuring positive and negative forces. It has a high natural resonance. It is rugged and resistant to damage, and its physical configuration permits ease of mounting using a standard clamp. Furthermore, eye lugs that accept 4-42 screws are provided on each side of the cantilever; these facilitate adaptation of the transducer for application in recording forces generated by a variety of animals and preparations. In our application, for example, the transducer is used to measure downward forces

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Figure 1. Block diagram of the proposed strain-gauge amplifier/analog processing circuitry, shown interfaced to microprocessor I/O ports.

exerted by the forepaws of rats. Thus, a threaded rod is attached to the center of an 18-mm-diam aluminum disk and simply screwed into one eye lug.

#### Amplifier

Processing of the small potentials produced by a force-induced imbalance in the strain-gauge bridge requires both low-noise circuitry and techniques of differential amplification (Faulkenberry, 1977). A configuration known as the instrumentation amplifier (Ott, Note 1) allows such amplification in the presence of even large common-mode transients such as those found in typical laboratory settings (e.g., relay switching, solenoid operation, computer-clock radiation). The circuit shown in Figure 2 permits interference-free and linear amplification of the strain-gauge signal.

Integrated Circuits A1-A3 are precision low-offset devices that form an instrumentation amplifier with a fixed gain of 210 (Precision Monolithics, Inc., 1980). These precision circuits, although more expensive than 741-type devices, allow a degree of gain and offsetvoltage stability necessary in critical applications and present high intrinsic common-mode rejection ratios (CMRR; see Faulkenberry, 1977). An LM741 forms an output buffer with both coarse- and fine-gain adjustments provided by the 10-kohm and 20-kohm 15-turn potentiometers, respectively (see Figure 2). Maximization of CMRR is provided by suitable adjustment of the 5-kohm pot that (through the 18-kohm resistor) grounds the noninverting input (Pin 5) of Differential Amplifier A3. The balance-resistor network, shown at the instrumentation amplifier inputs, nulls the straingauge output to the amplifier when no force is exerted upon the gauge. This network should be mounted in close proximity to the strain gauge, so that the high instrumentation amplifier CMRR figure can be preserved over long signal cables.

Instructions for adjustments of the balance network, CMRR, and gain potentiometers are included in the Calibration section of this paper.

#### **Active Filter**

Active filtering in this design employs National Semiconductor AF100-1CJ universal active filters that



## STRAIN GAUGE AMPLIFIER

Figure 2. Schematic diagram of the precision strain-gauge instrumentation amplifier. Stable, low-noise design is employed throughout. The 10-kohm balance potentiometer and 50-kohm wiper shunt resistor should be mounted in close proximity to the strain gauge to optimize common-mode rejection (see text).



ACTIVE FILTER

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Figure 3. Schematic diagram of the active filter section, showing (from left to right) the 60-Hz notch filter, 100-Hz low-pass filter, and half-wave precision rectifier sections.

are externally programmed for requisite filter functions. Specifications for the AF100-1CJ may be obtained from the National Semiconductor Corporation (1976). Figure 3 contains the schematic diagram for the active filter circuitry.

Stage 1 is a 60-Hz notch filter that supresses stray 60-Hz noise due to imperfect shielding and/or incomplete common-mode rejection in the strain-gauge amplifier. This filter accomplishes 60-Hz attenuation of at least 25 dB, leaving 57- and 63-Hz signals unattenuated. The 20-kohm potentiometer is used to null the filter at 60.0 Hz. (Instructions for nulling the filter are included in the Calibration section.)

Stage 2 is a two-pole Butterworth-type low-pass filter that provides a 12-dB/octave attenuation above a selected cutoff frequency (180 Hz in this application). Investigators who desire to modify the low-pass characteristics of this filter to suit particular applications should consult the formulas and nomographs for Butterworth "T" tuning in the National Semiconductor Corporation (1976) publication. The band-pass curves for the active filter module are shown in Figure 4.

The LM318 operational amplifier with diode output network forms a half-wave precision rectifier that allows linear rectification of low-level signals in accordance with the constraints of the A/D converter. The A/D converter circuitry in the configuration shown in Figure 5 will not tolerate negative input signals. Investigators wishing to digitize dual-polarity signals may do so by eliminating the precision rectifier and modifying the A/D converter circuitry as indicated in the A/D Converter section.

## A/D Converter

The A/D converter module shown in Figure 5 employs the ZN427E-8 integrated circuit (Ferranti Electronics Limited<sup>2</sup>). The ZN427 is a low-cost, high-

speed, 8-bit successive approximation counter. It offers unipolar and bipolar analog input ranges, as well as three-state, TTL-compatible digital outputs. Its only serious limitation is that the Start Convert (SC) pulse must be appropriately synchronized with the clock input to the ZN427.

Synchronization of the SC pulse is accomplished by the 7474 (dual-edge triggered flip-flop) circuit shown in Figure 5. The net result of this circuit at Pin 9 of the 7474 is a positive-going pulse that coincides with, and is of the same duration as, the negative clock cycle (Lancaster, 1977). This pulse is inverted by the 7404. Thus a negative-going SC pulse from external circuitry delivered to the R-C network at Pin 4 of the 7474 yields a suitably synchronized negative-going SC pulse of proper duration to Pin 4 of the ZN427.



Figure 4. System band-pass curve for the analog processing system. "0" dB is 1.00 V (average) applied to the input of the active filter module (instrumentation amplifier-frequency constraints are negligible). Passband characteristics are modifiable for custom application (see text).



Figure 5. Schematic diagram of the A/D conversion circuit. A/D converter outputs are tristate logic, allowing sampling of paralleled A/D channels without analog multiplexing (see text).

The output at Pin 4 of the CD4001 is a crystalcontrolled 1-MHz<sup>3</sup> square wave that provides clocking for both the ZN427 and the 7474 synchronizer circuit. The 7404 provides increased drive capability for the clock pulse. Consequently, a single clock circuit can provide clocking of up to four additional A/D converter modules.

The analog input-voltage range of the ZN427 is 0-2.5 V. Other input ranges may be obtained by connecting a resistor network to Pin 6 of the ZN427, as shown in the application notes provided in the ZN427 specification sheet. The input range of the circuit in Figure 5 is 0-10 V. (Instructions for adjustment of the 10-kohm gain and 1-megohm zero potentiometers are given in the Calibration section.)

In operation, conversion is initiated by the SC pulse. The digital output is valid when the end-of-conversion (EOC) output goes "high" (10-microsec worst-case, assuming a 1-MHz clock; 9 microsec minimum). Since the 8 digital-output bits of the ZN427 are three-state, these outputs remain essentially as open circuits until the Output Enable (OE) Pin 2 is brought to TTL "1." When OE is at TTL "1" (either under computer control or by connecting EOC to OE), the result of the conversion is available at the digital-output pins of the ZN427. The EOC and the digital outputs remain latched until receipt of the succeeding SC pulse.

## Self-Test Module

Although optional, the self-test circuit shown in Figure 6 is very useful in off-line testing and calibration of the amplifier and A/D converter circuitry and in online monitoring of A/D output. The module consists of two circuits, a square-wave generator and an LED digital-display circuit.

The LM555 integrated circuit is configured as an astable multivibrator whose output at Pin 3 is a 100-Hz square wave. This portion of the self-test module can be used in off-line operation to provide SC pulses to the input of the synchronizer circuit (Figure 5).

The digital-display circuit permits continuous monitoring of the state of each of the 8 output bits of the A/D converter. Each of these 8 bits is connected to an input of one of the 7404 inverters. The inverter outputs are each connected through a 330-ohm series resistor to the negative lead of an LED. The positive lead of each LED is tied to the 5-V source. When an output bit of the A/D converter is a logic "1," output of its corresponding inverter is a logic "0," allowing the inverter to sink current and thereby illuminate its LED. Conversely, a logic "0" at an A/D output turns off the LED.

## **Power Supply**

The power supplies for the strain-gauge signal processing circuitry must meet stringent criteria for precision

## SELF TEST



Figure 6. Schematic diagram of A/D self-test circuit, which allows both off-line calibration and on-line monitoring of ongoing A/D conversion using the integral LED display.

and stability. The use of the power supply configuration supplied by Fridlund and Fowler (1978) is highly recommended. This design provides the  $\pm 15$  V and  $\pm 5$  V needed for proper operation of the strain-gauge circuitry. The  $\pm 5$ -V supply supplies power for the TTL gating the strain-gauge circuitry; the  $\pm 15$  V is supplied using a dual-tracking configuration, wherein the negative rail "tracks" momentary fluctuations at the positive rail such that symmetrical amplitudes are maintained. The tracking configuration is essential for maintaining a stable offset voltage in the analog circuitry and consequent accuracy in A/D conversion. The power supply in Fridlund and Fowler (1978) provides precision and zero-point stability to within 1% and enables linear processing of signals with amplitudes up to 10 V.

#### Calibration

Calibration of the strain-gauge amplifier and the A/D converter circuitry requires a sine-wave generator, an oscilloscope, a digital voltmeter with 1% accuracy, a frequency counter, and a set of standard weights to be used as force standards. With the strain-gauge cable disconnected from the amplifier, a 10-kohm resistor is attached across the inputs of the amplifier (Pin 5 on A1 and A2, Figure 2). A 30-Hz 1-V (peak-to-peak) sine wave (referenced to ground) is applied to Pin 5 of A1. The 5-kohm CMRR potentiometer is then adjusted for the minimal voltage observed with the oscilloscope connected to the output (Pin 10) of Amplifier A3.

The 10-kohm resistor at the instrumentation ampli-

fier inputs is then removed, and the strain-gauge output cable is restored. With zero force on the transducer, the 10-kohm balance potentiometer (Figure 2) is adjusted for a null (.00 V dc) output at Amplifier A3 Pin 10.

Calibration of the 60-Hz notch filter is accomplished by setting the sine-wave generator for a 60.0-Hz, 1.0-V (peak-to-peak) signal that is input to the 100-kohm resistor at Pin 1 of the Stage 1 AF100-1CJ (Figure 3). The 20-kohm potentiometer is then adjusted for minimal output on an oscilloscope connected at AF100-1CJ Pin 11.

Adjustment of the gain potentiometers depends upon the range of forces to be measured and the resolution desired. For our purposes, forces between 0 and 200 g are measured with a resolution of 1.0 g. With .0-g force on the transducer, both gain potentiometers are set at midrange. The voltage output at Pin 5 of the Stage 2 AF100-1CJ is measured. The coarse-gain potentiometer is then adjusted until the voltage output is .00 V dc. With 200 g on the transducer, the coarse-gain potentiometer is then readjusted so that the voltage output is approximately 4 V dc. The fine-gain potentiometer may then be used for precise setting of the output voltage. Again, with .0-g force on the transducer, the output should be less than 20 mV dc. Further adjustment of these gain potentiometers for circuit linearity proceeds by applying the weights shown in Table 1 and adjusting for the corresponding voltage outputs.

Final adjustment of the strain-gauge amplifier gain potentiometer and the A/D converter zero and gain potentiometers is most easily accomplished using the self-test module. The digital-display circuit is attached to the A/D converter outputs, and the square-wave generator output is connected to the SC circuitry. Then the EOC (Pin 1) is connected to the OE (Pin 2) of the A/Dconverter. With weights removed from the transducer. the zero-adjust potentiometer of the A/D converter is adjusted so that the LSB of the digital display flickers; the potentiometer should then be reset slightly so that the LSB remains in a low state. Weights are then applied to the transducer, and the A/D gain potentiometer is adjusted so that the digital display for each weight corresponds to the value shown in Table 1. This may require some readjustment of the strain-gauge amplifier gain potentiometer.

Table 1 Calibration Table		
Weight in Grams	Voltage	Digital Display
1	.02	0000001
5	.10	00000101
10	.20	00001010
20	.40	00010100
100	2.00	01100100
200	4.00	11001000

Note-Shown are the voltage outputs at Pin 5 of the Stage 2 AF100-1CJ (Figure 3) and digital display corresponding to weights applied to FTO3 force transducer.

## **Computer Interfacing**

Interfacing of the A/D converter circuitry requires at least one parallel input port and one parallel output port. This minimal requirement permits control of and sampling from as many as seven A/D converter channels (assuming an 8-bit output port). The digital output of each A/D converter is connected to the computer parallel input port. One parallel output bit is connected to all A/D converter SC inputs, and each of the remaining output bits is connected to an OE (Pin 2) of an A/D converter channel (OE and EOC are not connected). Using this configuration, the bit controlling the SC of the A/D converters is held "high" until an SC pulse is desired. Bringing the SC bit "low" initiates simultaneous conversion in all A/D converter channels. It is held low for 10 microsec to allow adequate conversion time. The output of any A/D converter channel may be received at the input port by bringing its OE "high" while all other bits controlling OEs are "low."

For daily recalibration adjustments, it is convenient to interface a self-test module with the A/D converters. The digital outputs of each A/D converter are connected to the digital-display circuit. In order to monitor an A/D converter output off-line, the square-wave generator output is input to each A/D converter SC input by closing a switch between the generator output and the paralleled SC inputs to the A/D converters. Any A/D conversion, then, can be monitored by closing the circuit between EOC and OE of the A/D converters while all other A/D EOC-OE connections are open.

## CONCLUSION

The proposed circuitry offers several advantages over commercially available components. The described system is relatively low in cost and sacrifices no speed of conversion. Its flexibility permits use in a wide variety of laboratory applications.

In some applications, it may be desirable to obtain multiple analog measures simultaneously. Since this circuitry provides for interfacing of several A/D converters, all of which are initialized by a single SC pulse, simultaneous sampling from all channels is possible. The design and performance of this circuitry render it optimal for the present generation of microprocessor-based laboratory systems.

#### **REFERENCE NOTE**

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#### NOTES

1. The proposed circuitry can be constructed for less than \$75. The cost of the circuitry described by Fowler and his colleagues is approximately \$450.

2. Ferranti Electric, Inc., 87 Modular Avenue, Commack, New York 11725.

3. The choice of the 1-MHz clock frequency optimizes conversion speed and circuit simplicity. Slower frequencies increase conversion time and require either more expensive crystals or additional frequency-divider circuitry; higher frequencies require more complex synchronization circuitry without appreciable decrease in conversion time.

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