# Autoranging amplifier expands computer's A/D sensitivity by two decades

C. F. RICHMOND and T. H. NILSSON University of Alberta, Edmonton, Alberta, Canada

This device accepts an analog signal from 0 to  $\pm$ 14 V, automatically changes gain to condition the analog output to the limits of a  $\pm$ 1 V A/D converter, and transmits the gain mode as two digital bits. A computer with a 10-bit A/D converter and two sense lines uses this device to obtain the dynamic range of a 16-bit A/D converter. The relatively simple principle of the circuit may be of interest to expand the voltage sensitivity range of other analog devices for slowly changing signals.

Current technology offers ample opportunities for measurement to high degrees of precision at corresponding cost; but in the behavioral sciences, measurements are often made over a wide range of conditions with less demand on accuracy. For example, to discern 1% changes at both 10 V and 10 mV, a device with an accuracy of .1 mV at 10 V (.0001%) is not necessary. On the other hand, the 1 part in 512<sub>10</sub> acurracy of the 10-bit A/D converters commonly used on 12-bit minicomputers may often be insufficient to track psychophysical data over a wide stimulus range. While logarithmic transformation can handle analog voltages from observer response settings under some conditions, the inevitable loss of resolution at the high end may be a problem, particularly if the psychometric data do not correspond to a power function. To solve such problems, we built an autoranging amplifier which transmits 0 to +14 V signal levels at either unity, X10, or X.1 gain, depending on the signal level. The gain is indicated to the computer by a 2-bit code on two sense lines, and to the experimenter by three indicator lights. The autoranger is made with 5 general-purpose 741 operational amplifiers, 4 field effect transistors, 4 small signal diodes, 3 lightemitting diodes, 30 5% 4-W resistors, and 9 miniature potentiometers, for a total cost of less than \$30, including a circuit board and a case.

# **OPERATION**

Operational Amplifier 1  $(OA_1)$  is a voltage follower which provides input buffering of the signal voltage. Its output is fed to the programmable gain amplifier,  $OA_2$ , and two voltage comparators  $OA_3$  and  $OA_4$ .

 $OA_2$  inverts the input signal and operates in one of three possible gain modes, depending on the signal level: for low-level signals, it operates at a nominal (see below) gain of X10 through the  $R_1$  feedback loop; when the signal level exceeds .19 or 1.9 V, the gain is reduced to X1 or X.1, respectively, by opening of the

field effect transistor gates (JFETs) in feedback loops  $R_2$  or  $R_3$ . (Since the JFET source terminal is at the summing point of  $OA_2$ , which remains at virtual ground as referenced at the noninverting input of  $OA_2$ , gate-source voltage is at zero during the JFET on state, thus obviating need for bootstrapping the JFET gate.)

OA<sub>3</sub> and OA<sub>4</sub> serve as summing mode voltage comparators. Their outputs drive the JFET gates in the feedback loops of OA2, drive JFET gates on the computer sense lines, and drive the three indicator lightemitting diodes. OA<sub>3</sub> outputs +15 V unless the input signal exceeds its comparison voltage of 1.9 V (adjustable by  $P_5$ ), whence it outputs -15 V. The +15 V output state closes the JFET gate in Feedback Loop R<sub>3</sub> of  $OA_2$ . The -15 V state opens that JFET gate as Diode D<sub>1</sub> and Resistor R<sub>4</sub> clamp the gate voltage at zero. OA<sub>3</sub> controls the JFET gate on Sense Line B in the same manner to transmit or sink a positive logic output. (For negative logic, D<sub>2</sub> should be reversed; and the roles of Sense Lines B and A become reversed.) Light-emitting Diode L<sub>1</sub> connected to OA<sub>3</sub> indicates when OA<sub>2</sub> is operating at X.1 gain. OA<sub>4</sub> operates similarly for X1 gain, having a .19 V comparison threshold. When OA<sub>4</sub> is outputting +15 V, L<sub>3</sub> is turned on, indicating OA2 is at X10 gain.

 $OA_5$  reinverts the signal to its original polarity, permits adding an offset voltage, and produces a final corrective gain for the signal output. Adding an offset voltage permits single-polarity signals to maximally utilize bipolar A/D converters.  $OA_5$  operates at a gain of X.2 in order that the Feedback Resistance  $R_3$  can be made large with respect to the JFET on-resistance to avoid nonlinearities while  $R_1$ , larger by a factor of 100, must remain within practical limits. (A sixth operational amplifier in the voltage follower configuration of  $OA_1$  may be added at the output of  $OA_5$  to provide output buffering if necessary.)

## **ADJUSTMENTS**

Adjustments of the three gain modes, the two gain breakpoints, hysteresis of the breakpoints, and offset

Development was supported by the National Research Council of Canada under Grant APA-145.

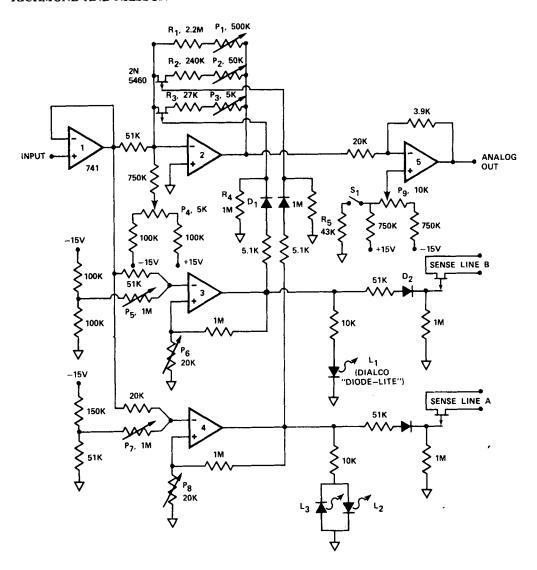


Figure 1. Circuit schematic of the autoranging amplifier.

is accomplished with nine 20-turn miniature potentiometers. Mounting all the potentiometers along the front edge of the circuit card facilitates trimming through labeled holes in the case.

 $P_1$ ,  $P_2$ , and  $P_3$  adjust the X10, X1, and X.1 gain modes of  $OA_2$ . For some users, it may be more convenient to use binary gain modes such as X8, X1, and X1/8, also adjusting  $P_5$  and  $P_7$  accordingly.

P<sub>4</sub> provides current offset to the input of OA<sub>2</sub> to compensate for voltage offsets resulting from any previous signal processing and from the non-negligible gate to source current of the JFET gates in the feedback loop (Graeme, 1973; Todd, 1968).

 $P_5$  and  $P_7$  control the approximate (see below) reference voltage at which comparators  $OA_3$  and  $OA_4$  alter the gain modes of  $OA_2$ . The required reference voltages are determined by the existing range of the A/D converter, the desired expansion, and whether output offset is used.

To eliminate chatter when the signal is near the comparator's switching thresholds, hysteresis is provided through positive feedback. P<sub>6</sub> and P<sub>8</sub> control the magnitude of hysteresis, which should be set greater than the magnitude of signal noise (Tobey, Graeme, & Huelsman, 1971). (For a threshold voltage of 1.9 V, a .1 V hysteresis prevents imposed transients of less than .1 V from switching the comparator; an increasing signal switches the comparator at 1.95 V, while a decreasing signal switches it at 1.85 V). If desired, P<sub>6</sub> and P<sub>8</sub> may be replaced with fixed resistors (a 10K resistor provides approximately .15 V hysteresis).

In addition to providing adjustment of output offset voltage,  $P_9$  is used in the zero offset mode to correct for any unwanted offset voltage introduced by the circuit. Zero offset is useful in calibrating the gain modes of the circuit even when it is to be used with output offset. Switch  $S_1$  selects  $R_5$  for an output of -1.0 V,  $P_9$  trims offset to this value after the gain is calibrated.

For other offsets, select an R<sub>5</sub> value to minimize the adjustment of P<sub>9</sub> from the zero offset state.

# **CALIBRATION**

Since certain adjustments interact, calibration is most easily achieved by the following iterative sequence. If a variable voltage reference and a digital voltmeter or two matched meters are available, it should only take about 10 min. The stated calibration values are for using the circuit with 0 to +10 V signal levels at decade gains to a  $\pm 1$  V A/D converter. To calibrate:

- (1) Throw the output offset switch to the zero position.
- (2) Set the comparator reference voltages: (a) Adjust  $P_5$  so that  $L_1$  comes on when the input signal rises to about 1.9 V. (b) Adjust  $P_6$  so that  $L_1$  goes off when the input falls to about 1.8 V. (c) Adjust  $P_7$  so that  $L_2$  comes on when the input rises to about .19 V. (d) Adjust  $P_8$  so the  $L_2$  goes off when the input falls to about .18 V.
- (3) Set the X.1 gain: (a) Set the input signal to 9.0 V. (b) Adjust  $P_3$  for a .9 V output signal. (c) Set the input to 2.0 V. (d) Adjust  $P_9$  for a .2 V output. (e) Repeat steps a-d.
- (4) Set the X10 gain: (a) Set input to .175 V. (b) Adjust P<sub>1</sub> for a 1.75 V output. (c) Set the input to .020 V. (d) Adjust P<sub>4</sub> for a .2 V output. (e) Repeat steps a-d.
- (5) Set the X1.0 gain: (a) Set the input to 1.75 V.(b) Adjust P<sub>2</sub> for a 1.75 V output.
  - (6) Repeat Steps 3, 4, and 5.
- (7) Set the output offset: (a) Throw the offset switch to the -1.0 V position. (b) Adjust  $P_9$  for a -.100 V output.
- (8) Repeat Step 2, though normally no adjustment will be necessary.

### **USE**

The circuit should be calibrated, allowed to "burn in" by being left on for a week, and then calibrated again. Our autoranger has operated flawlessly and continuously for over 1 year. The only time it required

Table 1
Summary of Autoranger Functions With -1 V Offset and Required Calculation

Input Voltage	_	Indicator Lights L1 L2 L3			Output Voltage	Lir		Computer Should
0 to .2	X10	Off	Off	On	- 1 to 1	+	+	+1;÷10
.2 to 2	X1	Off	On	Off	8 to 1	0	+	+1
2 to 14	X.1	On	On	Off	8 to +.4	0	0	+1; × 10

recalibration was after we had changed power supplies. A good quality  $\pm 15 \text{ V} \ge 50 \text{ mA}$  supply is essential for stable operation. The modular power supplies offered by several manufacturers of operational amplifiers such as Analog Devices, Burr-Brown, etc., or the  $\pm 15 \text{ V}$  supply in most computers is adequate.

Table 1 summarizes the function of the autoranger and the corrective calculation which the computer should perform to obtain the original signal value. To be certain the signal has not changed across a gain mode between sampling the A/D and testing the sense lines, it may be advisable to test sense line status before and after an A/D sample and resample if the status has changed.

Our device was designed for and has been used to monitor voltage levels changing at less than 1 Hz. With inexpensive 741 amplifiers, its inherent frequency response extends accurately to a few kilohertz. When the device is used with a computer, however, the maximal useful frequency will generally be much less than 1 kHz due to the rate at which sense lines and A D converter can be interpreted together with allowance for a repetition of readings when the gain changes.

### REFERENCES

Graeme, J. G. Applications of operational amplifiers. New York: McGraw-Hill, 1973. Pp. 99-100.

Tobey, G. E., Graeme, J. G., & Huelsman, L. P. Operational amplifiers. New York: McGraw-Hill, 1971. Pp. 361-364. Todd. C. D. Junction field effect transistors. New York: Wiley, 1968. Pp. 160-166.

(Revision received July 7, 1975.)