A computer-compatible technique for the recording of successive events as in a one-way alley*

BRIAN M. KRUGER
Wright State University, Dayton, Ohio 45431

Platt and Senkowski (1968) describe a system for recording interevent times (IETs) on eight-channel paper tape that could be adapted for use with other computer-compatible media. The system was designed for monitoring several operant chambers concurrently. Since an event in one chamber may occur during the recording cycle initiated by an event in another, the time unit of measurement (Δt) must be slightly greater than the data recording cycle (DRC); the same limitation exists when using their design for recording IETs for successive events. However, with only minor modifications of the design, it is possible to employ Δts much smaller than the DRC for recording successive events that are separated by time intervals greater than the recording cycle (IET > DRC). For example, recording of running times in successive 2-ft segments of an alley with Δt equal to 0.01 or 0.001 sec can be accomplished.

The Platt and Senkowski (1968) technique involves checking at the end of each Δt for events occurring during the immediately preceding Δt. A successful check immediately initiates a DRC. For either the simultaneous (Platt & Senkowski, 1968) or successive (modified design) event recording systems, each data set consists of two subsets of 8 bits of information. One subset is recorded on eight-channel paper tape with each of two punch cycles. One bit in each subset is assigned to subset identification, leaving a total of 14 bits for event and IET coding. Each punch cycle consists of three phases: preparation of the data for punching culminating with entry of the information into the punch buffer, punching one row on the tape, and clearing the buffer.

*Construction of the system described and computer time for analysis of tapes generated by the system were supported by the College of Science and Engineering, Wright State University. The assistance of J. Michael Lucas in constructing the system is gratefully acknowledged.

When simultaneous events are recorded, the event coding bits are included in the first subset in order to minimize error in assignment of events to Δts. Errors of assignment occur when an event occurs during the data preparation phase of the first punch cycle of a DRC initiated by another event or events: such an event is incorrectly assigned to the preceding Δt along with the initiating events.

When IETs for successive events are recorded, the seven least significant IET bits are included in the first data subset. Immediately following entry of the first data subset into the punch buffer, the seven least significant flip-flops in the IET binary counter are reset; these flip-flops are thus ready to register Δt counts during the remainder of the DRC. In order to prevent errors of omission in counting Δts, Δt must exceed the data preparation time for the first subset. For the example BRS/Foringer system employed by Platt and Senkowski (1968), this limitation is 800 microsec.

A second consideration is that, since additional flip-flops in the binary counter are not available for registering Δt counts until they are reset following entry of the second subset into the punch buffer, the maximum count of 127 Δts by the seven least significant flip-flops in the IET binary counter must exceed the punch cycle time. With the BRS/Foringer system, the flip-flops associated with the most significant IET bits in the second data subset are reset as required in less than 127 Δts when Δt is equal to 0.01 or 0.001 sec.

In summary, there are no errors in assignment of events to Δts or omissions of Δt counts when IETs exceed the DRC and Δt is equal to or greater than 0.001 sec. The number and type of logic modules required for the two logic circuits are virtually identical.[1]

REFERENCE

Platt, J. R., & Senkowski, P. C. A computer-compatible technique for recording binary events in real time. Behavior Research Methods & Instrumentation, 1968, 1, 79-81.

NOTE

1. A detailed description including a logic module schematic will be sent by the author upon request.

(Received for publication July 21, 1973;
revision received October 20, 1973.)