A linear interval to voltage device for oscilloscope display

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A linear interval to voltage device is described for oscilloscope displays. A schematic diagram is included.

The simple device described here will produce a voltage linear with the time elapsed since some event. It has been used to display single-unit interspike intervals on an oscilloscope screen so that patterning of firing might be seen during data collection. It has been successful in allowing experimenters to discover changes in firing rate patterns which were not discernible on the basis of auditory feedback.

The display appears on the oscilloscope screen as a dot for each event occurrence; the height of the dot above a baseline is proportional to the time elapsed between that event and the preceding one. The horizontal sweep speed may be set very slow so that events over a considerable period of time may be observed in one sweep.

FUNCTIONAL DESCRIPTION

The schematic diagram for the device is shown in Fig. 1. The device has four basic stages. The first stage is a one-shot, OS-1, which intensifies the oscilloscope trace. The second stage resets the ramp generator after trace intensification. It consists of OS-2, Q_1, R_1, and D_1. The third stage is the linear ramp generator and consists of Q_2, R_2, and C_5. The final stage is a source follower output stage consisting of Q_3, and R_3.

The event to be timed must produce a trigger pulse with a 0- to +15-V edge and a duration of at least 100 msec. The trigger pulse is fed into Pin 1 of IC-1. The output pulse width, PW_1, of OS-1, the first stage, is approximately:

$$PW_1 = 0.7(20{,}000 \times C_1). \quad (1)$$

The "1" output of OS-1, V_b, is a 0- to +15-V 1.4-msec pulse taken from Pin 2 of IC-1 and fed to the Z-axis input of an oscilloscope.

The "0" output of OS-1 is a +15- to 0-V 1.4-msec pulse taken from Pin 6 of IC-1 which acts as a delayed trigger for OS-2, the second stage, and is fed to Pin 13 of IC-1. The output pulse width, PW_2, of OS-2 is approximately:

$$PW_2 = 0.7(20{,}000 \times C_3). \quad (2)$$

The "0" output pulse (+15 to 0 V, 1.4 msec) from Pin 8 of IC-1 is fed to the base of Transistor Switch Q_1. Between events, Q_1 is kept at cutoff by the +15 V from the "0" output from OS-2. This causes the emitter of Q_1 to maintain +15 V. Consequently, Diode D_1 is reverse biased, since its anode cannot attain a voltage more positive than +15 V. When an event causes OS-2 to be triggered, the "0" output goes to 0 V for the duration of the pulse, thus applying 0 V to the base of Q_1. The emitter of Q_1 also goes to 0 V, thus forward biasing Diode D_1 for any anode voltage more positive than 0 V.

The third stage, the linear ramp generator, is formed by R_2, Q_2, and C_5. Components R_2 and Q_2 form a constant current source which applies a constant positive current to C_5 independent of the charge across C_5. Since in a capacitor $dv/dt = I/C$, if I and C are held constant, the rate of change of voltage across the capacitor must be constant. Any resistance in parallel with the capacitor will reduce the linearity of the system, because it produces an RC discharge path resulting in an exponential charge rate. In this circuit, three such possible paths exist. The first is through the capacitor, but the use of a low-leakage capacitor for C_5 will block that path. Another path leads to the reverse biased junction at the gate of a junction field effect transistor, Q_3. The remaining path is through the diode, D_1. Between events, D_1 is reverse biased and the charge across C_5 will increase linearly over time. However, 1.4 msec after an event, D_1 will be forward biased for a 1.4-msec duration, thus providing a discharge path for C_5 through D_1 and Q_1. During this period, the charge across C_5 will be reduced to 0 V, resetting the ramp generator to 0 V.

The final source follower stage consists of Q_3 and R_3. Its function is to block a discharge path for C_5, which would be present if the voltage across C_5 were fed directly into an oscilloscope vertical amplifier. The input impedance of vertical amplifiers is typically no greater than 1 megohm. Such a resistance in parallel with C_5 would substantially detract from the linearity of the ramp generator. Since the gate of a source follower is always reverse biased, the interpolation of the source follower, Q_3, as an interface between the ramp generator the oscilloscope vertical amplifier prevents such a discharge path and the resulting nonlinearity. The voltage from the source of Q_3, V_a, is fed to the vertical amplifier of an oscilloscope.

PRACTICAL CONSIDERATIONS

Capacitors C_2 and C_4 increase the noise immunity of the one-shots. C_2 should be the same value as C_1, and C_4 should have the same value as C_3.

If the pulse width of OS-1, PW_1, is too short, trace intensification will be too small to be noticeable. If PW_1 is too long, the trace intensification will appear as a line instead of a dot. Experience in my laboratory has shown that with a Tektronix 565 oscilloscope, the tradeoff is optimal of PW_1 is between 1 and 1.5 msec. Other oscilloscopes may have faster or slower Z-axis modulation characteristics, which would allow shorter or

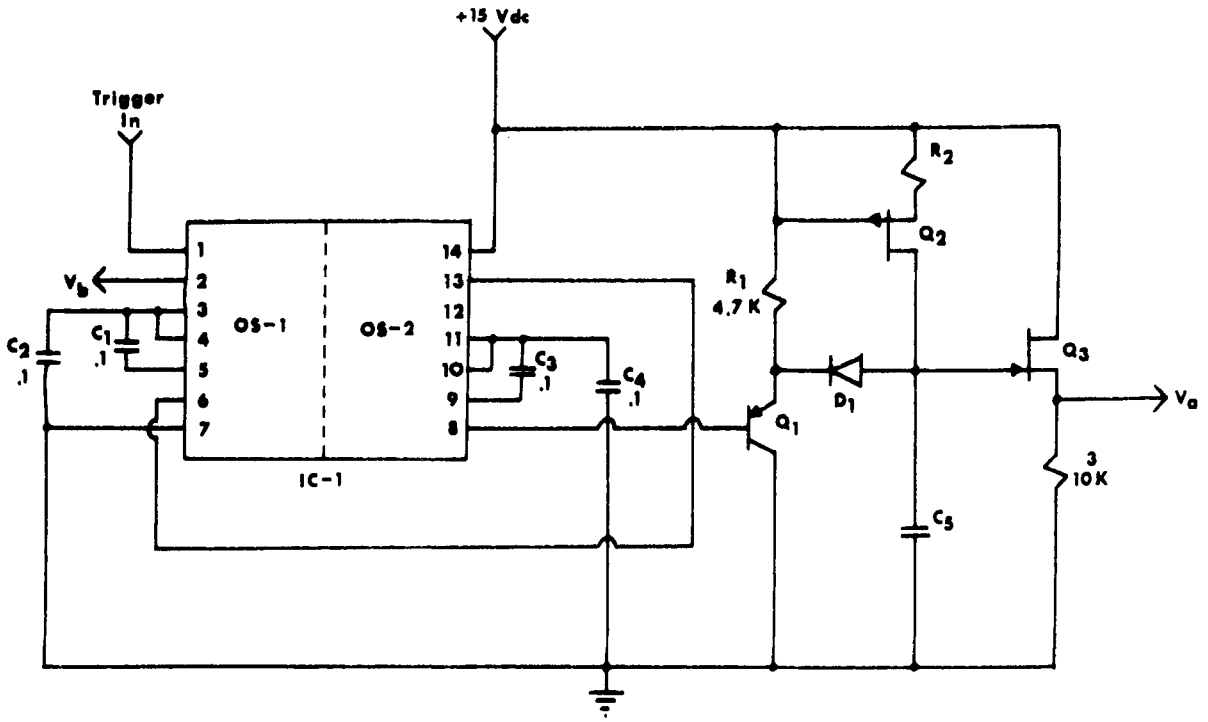

Fig. 1. Schematic diagram of the linear interval to voltage device for oscilloscope display.

require longer PW_1 durations, respectively.

The duration of the reset pulse, PW_2, is "dead time" in that there is no ramp generation during reset. Therefore, PW_2 should be kept as small as possible. The minimum width of PW_2 is determined by the amount of time it takes to discharge C_5. Consequently, the smaller the value of C_5, the shorter PW_2 may be. A PW_2 of 1.4 msec will allow discharge of a C_5 of 0.47 microF. If a smaller C_5 value is used, PW_2 can and should be decreased.

The rate of change of voltage across C_5 during ramp generation is determined by the value of C_5 and the current through R_2. The current through R_2 may be estimated by:

$$I = \frac{3}{R_2}. \tag{3}$$

This estimation will be only approximate because of the differences in characteristics among individual transistors used as Q_3. Therefore, it is advisable to have R_2 adjustable so that transistor variations can be compensated for. A 500-kilohm potentiometer set about midrange works well as R_2. The rate of change of voltage in volts/second across C_5 may be calculated by:

$$\frac{dV}{dt} = \frac{I}{C_5}. \tag{4}$$

Combining Eqs. 3 and 4 will yield

$$\frac{dV}{dt} = \frac{3}{R_2 C_5}. \tag{5}$$

The dV/dt desired depends on the interevent interval, IEI, of interest. If the dV/dt is too slow, resolution is sacrificed. If too fast, C_5 will attain full charge too rapidly and all IEIs longer than a certain value will be displayed at the same, full voltage value. The desired dV/dt can be determined by setting the value of the longest IEI of interest and using the formula:

$$\text{desired } \frac{dV}{dt} = \frac{10\text{ V}}{\text{IEI maximum}}. \tag{6}$$

If the longest IEI of interest were 1 sec, typical values for R_2 and C_5 would be 300 kilohms and 1 microF, respectively; if 100 msec, 300 kilohms and 0.1 microF, respectively, would be typical. It should be noted from Eq. 5 that it is the $R_2 C_5$ product which is important, so that the above typical values for the 100-msec IEI are equivalent to an R_2 of 30 kilohms and a C_5 of 1 microF. Therefore, if a 500-kilohm potentiometer is used for R_2, an adjustment range for maximum IEI of about 2 decades is available for any given C_5 value by setting the R_2 value.

The height of the dot on the screen will be determined by the voltage at V_a during trace intensification, V_{dot}, and may be calculated by:

Table 1
Parts List

IC-1	MC667P or HEP CO911P Motorola high threshold logic dual monostable monovibrator
Q_1	2N4059
Q_2	2N3820
Q_3	2N3819

Note–All resistors are ½ W, 10%.

$$V_{dot} = (IEI - PW_2)\left(\frac{dV}{dt}\right) + V_{offset}, \quad (7)$$

in which V_{offset} is the source follower offset voltage. It is clear that the presence of the source follower offset voltage will prevent the linear relationship between time and voltage from passing through the origin when plotted on cartesian coordinates. If passage through the origin is necessary, the offset voltage can be subtracted by using a simple operational amplifier subtracting circuit (e.g., see Diefenderfer, 1972).

REFERENCE

Diefenderfer, A. J. *Principles of electronic instrumentation.* Philadelphia: Saunders, 1972. P. 314.

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