Hardware techniques for analog processing using the State Systems PDP-8 I/O interface

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Methods are described for construction and use of an analog-to-digital (A/D) converter system which is interfaced with a PDP-8/E through the State Systems interface. Eight bits of one input word are used to bring the results of A/D conversion into the accumulator, and four bits of an output word supply convert and channel-select pulses for the A/D converter and associated eight-channel multiplexer. With a Datel ADC-EH8B1 A/D converter, which digitizes a sample in 4.0 microsec, the system software can perform a conversion in 18.8 microsec. Approximate cost of parts for fabricating the hardware is about \$120. Examples of software incorporating the A/D capability are presented for a laboratory computer system used to measure operant response force.

Users of laboratory computers face two major practical problems: interfacing the computer to conventional instruments and development of software. Both of these problems have been partially solved for experimental psychology laboratories by the State Systems¹ interface for the PDP-8² and the accompanying SKED software (Butler, 1975; Cobe & Snapper, 1976; Snapper & Hamilton, 1974). However, despite its remarkable versatility, the State Systems interface was designed primarily to process digital information. Thus, laboratories which are concerned with measurements based on analog signals are either obliged to build their own interface or forced to turn to the relatively expensive vendors of ready-made equipment. The purpose of this paper is to describe a comparatively low-cost analog-to-digital (A/D) conversion system that can be simply interfaced with the PDP-8 by using the State Systems hardware. Although Butler (1975) has described some software techniques that permit the processing of analog information with the SKED system, we have found that the real-time computing load demanded by experiments on the intensive properties of operant responses does not allow the use of SKED software. Instead, we developed programs in assembly language based on the concepts described by Fowler (1974).

The minimum hardware required for use of the A/D system described here is a PDP-8 computer, a suitable terminal, and a State Systems interface consisting of a BUS-ALL, an input module, an output module, and a real-time clock module. For users who possess a PDP-8/E, the KA8-E positive I/O bus is needed.

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The State Systems interface provides for the output of three 12-bit words (totaling 36 separate bits of information) and the input of three 12-bit words. In practice, the status of an input word is interrogated by issuing an IOT instruction, and the status of the lines is transferred into the accumulator (AC). Similarly, the execution of an appropriate IOT instruction results in the transfer of the contents of the AC to one of the output words. The A/D converter system, schematized in Figure 1, makes use of one output word and one input word. The output word (IOT = 6112) supplies the A/D circuitry with 4 bits of control information, whereas the remaining 8 bits are left unused in this application. An input word (IOT = 6103) carries the results of the 8-bit conversion into the lower 8 bits of the AC; the other 4 input bits are permanently turned off (see diagram for AC Bit 0 in Figure 2).

CIRCUIT OPERATION

Active components of the A/D system may be divided into three functional categories (see Figure 1). These are digital buffering circuits (IC1, IC2, IC5, and IC6), analog multiplexing and buffering (IC3 and IC4), and A/D conversion (Datel³ ADC-EH8B1). A parts list of active circuit elements is given in Table 1.

Digital buffering is required to achieve the proper polarity relationships between the State Systems interface and the A/D system. Each output line of the State Systems interface is driven by a 7406 (hex inverter with open collector output). If the status of an AC bit is "1" when the output instruction is executed, the 7406 output is switched to ground. The 7404 (IC2 in Figure 1) then reinverts the digital signal so that a "1" in the AC is delivered to the A/D system as a positive voltage ("1"). One control pulse from the AC is termed the "convert" pulse. After passing through the 7404, the convert signal triggers the one shot (IC1, Figure 1) to supply a 300-nsec duty-cycle pulse to the A/D con-

Table 1
Parts List of Active Components* for the Circuit Shown in Figure 1

Quantity	Device	Model Number	Manufacturer†	Price
1	A/D Converter (8-Bit)	ADC-EH8B-1	Datel, Inc.	\$85.00
1	Analog Multiplexer	AM3705-CD	National Semiconductor	9.00
1	Op Amp	LH0022	National Semiconductor	12.00
1	One Shot	SN74121	Texas Instruments	.39
1	Hex Inverter	SN7404	Texas Instruments	.45
2	Buffer Driver	SN7407	Texas Instruments	.58

*Resistive and capacitive values are given in Figure 1.

†Manufacturer's address for devices not widely distributed are given in the footnotes.

verter at Pin 3, thereby initiating the conversion. The other three control lines in Figure 1 are labeled 2^0 , 2^1 , 2^2 . These specify the analog channel selected by the analog multiplexer for input to the A/D converter. Of course, the 3 binary bits are used to select one of eight different analog channels. Because the output of the A/D converter is positive logic, 7407s (open collector drivers, IC5 and IC6 in Figure 1) are used to drive the State Systems interface as illustrated in Figure 2 (see AC Bits 4-11). A "1" on the output of the A/D converter causes a "1" to appear in the AC after execution of 6103. The 4 unused bits of IOP3 have both "NO" and "NC" inputs connected to ground so that these 4 higher order bits of the AC are permanently off (see Figure 2, AC Bit 0).

Analog multiplexing is performed by IC3, a 16-pin

integrated circuit (see Figure 1 and Table 1). Detailed specifications for this circuit may be found in *Linear Integrated Circuits* (1974). The switching time is approximately 500 nsec—a value conveniently fast for the PDP-8/E. Through the switch itself the signal current can be as high as 30 mA, but much lower currents are generally encountered in practice. Finally, the AM3705 has the property that voltage on any analog input channel greater than +5 V results in the output's rising immediately to +5 V even if all channels are turned off. For this reason, all analog input voltages must be restricted to values below +5 V. An alternative chip that does not "latch up" below +20 V is available from Siliconix.⁴ The pin configuration of the Siliconix DG508 is slightly different from the AM3705, so they are not interchangeable. With the circuit shown in

Figure 1. Circuit diagram of the analog-to-digital converter system which is interfaced with the PDP-8/E through the State Systems interface. MSB means most significant bit. Resistor and capacitor tolerances are 5%.

Figure 2. Circuit diagram illustrating the connections between the output of the A/D converter system and the input word of the State Systems interface. Representation of the State Systems interface in this figure is taken from the documentation supplied by State Systems, Inc. "NO" and "NC" correspond, respectively, to the normally open and normally closed contacts of an input relay which is the conventional mode of transferring information into the State Systems interface. Accumulator (AC) Bits 1, 2, and 3 are treated just as AC Bit 0 in the figure; similarly, the connections for AC Bits 5-10 are identical to those shown for AC Bits 4 and 11.

Figure 1, the analog signal ground is tied to power ground. This procedure avoids the further wiring complexity of a differential input system. Referencing the analog system to power ground has a negligible effect on signal noise in the present system because the signal preamplification is performed before the signal is applied to the analog switch, and because well-regulated power supplies are employed.

Pin 1 of the analog switch (IC3 in Figure 1) is tied to +5 V in order to maintain the analog switch in the "output enable" condition, thereby simplifying the software manipulation of control pulses.

The output of the analog switch (Pin 3 of IC3 in Figure 1) is fed into an operational amplifier (op amp, IC4 in Figure 1) which serves as a buffer amplifier between the low-impedance analog switch (150 Ω) and the relatively low-impedance A/D converter (4.45 K Ω). The buffer op amp also presents a relatively high input impedance to the signal source. The op amp is wired in a noninverting configuration with a 50-K Ω input resistor (R1 in Figure 1). Thus, some signal scaling can be accomplished with the 500-K Ω potentiometer (R4 in Figure 1). The particular op amp used here is over-designed for this application (given the impedances used). A 741-type op amp is much less expensive and would easily accomplish the required buffering function.

(For applications involving signal frequencies below 100 Hz, slow rate specifications can be ignored.)

The mainstay of the A/D system is the 8-bit A/D converter³ (see Table 1). This device can perform a conversion in 4.0 microsec. It also has the attribute that the results of a conversion are retained on the eight parallel output lines until a new convert pulse arrives. One possible disadvantage of the Datel device is its cost. Recently Burr-Brown⁵ announced an integrated-circuit 8-bit A/D converter with a 2.8 microsec conversion time for only \$55. We have not tested the Burr-Brown circuit (ADC82). However, the Datel A/D converter used here does not seem unduly expensive in view of its reliability; over the course of a year it has performed approximately 500×10^6 conversions.

CONSTRUCTION

The circuit shown in Figure 1 can be constructed on a single printed circuit board following the general techniques described by Brown, Maxfield, and Moraff (1973). We use "DIP" sockets for the integrated circuits and for the modular A/D converter. Because our laboratory employs the State Systems interface for a number of different applications, the input word and the output word are connected to the A/D system by means of 14-pin IC sockets to permit convenient switching among peripherals. A printed circuit board foil pattern and component layout may be obtained by writing the first author.

SYSTEM PERFORMANCE

The capacity of the A/D system to process analog signals satisfactorily depends primarily upon the sampling rate and the aperture time. The aperture time is the

Figure 3. The effect of sampling rate on waveform resolution. The inset at the top center is a strip chart recording of a 10-Hz rectified sine wave. Quantized versions of the signal are shown for sampling rates of 100/sec (on the left) and of 1,000/sec (on the right).

Figure 4. Measurement of response force-time curves using the A/D system. The analog signal depicted in the strip chart recording was sampled at the rate of 100 samples/sec to produce the waveforms represented by the open data points.

time required to take the measurement; during the aperture time the signal may be changing, which results in some error. Because no sample-and-hold circuit was used in the system, the convert time of 4.0 microsec becomes the aperture time. According to nomographs published by Datel (*Engineering Product Handbook*, 1974) a 4.0-microsec aperture time (which equals

conversion time in this case) permits satisfactory conversion of sinusoids of over 100 Hz. The sampling rate, the frequency with which convert pulses are delivered to the A/D converter, must be somewhat higher (five times or more) than the frequency of oscillation of the signal being quantized. In the present application, which measures response force, a sampling rate of 100/sec is adequate.

Examples of analog signals recorded simultaneously with a responsive strip chart recorder (3 dB attenuation at 45 Hz full scale) and the A/D system are shown in Figures 3 and 4. Figure 3 illustrates the performance of the system in quantizing a 10-Hz rectified sinusoid. The function on the left was based on a sampling rate of 100 samples/sec. The lack of correspondence between the strip chart recording and the plotted function based on digital values is a result of insufficiently high sampling rate and is not caused by the comparatively long aperture time. This follows from the fact that the data gathered for the same 10-Hz signal at 1,000 samples/sec (function on the right in Figure 3) provide a much more detailed picture of the waveform. Figure 4 shows data typical of those generated by a rat pressing a force transducer serviced by the A/D system. A sampling rate of 100 samples/sec and the 4.0-microsec aperture time appear adequate for measuring the intensive properties

Table 2
Assembly List of Program Which Obtains 128 Digitized Samples at the Rate of 100 Samples/Sec

0200	0200		*200	
0201	7200		CLA	/ensure accumulator is clear
0202	1217		TAD C128	/add 128 (decimal)
0203	7041		CIA	/to count 128 samples
0204	3220		DCA COUNT	
0205	1221		TAD PNTR	/pointer for data table
0206	3010		DCA 10	/use auto index register 10
0207	6071	ANOTH,	6071	/skip on clock flag; clock set at 100 Hz
0210	5206		JMP.-1	/wait for clock flag
0211	6072		6072	/clear clock flag
0212	1222		TAD CH1	/specify multiplexer channel
0213	4223		JMS SAMPLE	/jump to subroutine sample
0214	3410		DCA I 10	/deposit digitized value
0215	2220		ISZ COUNT	/128 samples yet?
0216	5206		JMP ANOTH	/no
0217	7402		HLT	/yes, halt
0220	0200	C128,	200	/128 (decimal)
0221	0000	COUNT,	0	/counter register
0222	3777	PNTR,	3777	/pointer to data table
0223	0200	CH1,	0	/AC bits 2, 3, and 4 specify analog channel select code: /0 designates channel 1
0224	0000	SAMPLE,	0	/subroutine to perform conversion
0225	6112		6112	/select multiplexer channel
0226	1235		TAD CPULSE	/add convert pulse code
0227	6112		6112	/keep channel on and initiate conversion
0230	7000		NOP	/wait for conversion
0231	7000		NOP	/wait for conversion
0232	7200		CLA	
0233	6112		6112	/set control lines to 0
0234	6103		6103	/bring digitized values into lower 8 bits of AC
0235	5623		JMP I SAMPLE	/return
0236	0000	CPULSE,	2000	

(peak force, duration, and time integral of force) of responses. Moreover, the data presented in Figures 3 and 4 suggest that the A/D system is responsive enough to process many bioelectric phenomena (e.g., EEG, EKG, or EMG).

It should be noted that accurate measurement of the force-time waveform of a pigeon keypeck could probably not be accomplished without the addition of a sample-and-hold circuit, which would reduce the aperture time from 4.0 microsec to perhaps 100 nsec. Such data as have been collected for force of keypeck indicate that many responses are as brief as 5 msec (see Rilling, Kramer, & Askew, 1970); therefore, a 4.0-microsec aperture time could lead to considerable error in describing the waveform, particularly in regions where the force is changing very rapidly.

SOFTWARE

Table 2 gives a short PDP-8 assembly language program which performs A/D conversions for a specified multiplexer channel and stores the resulting data in memory. In this example, it is assumed that the real-time clock of the State Systems interface is manually set to the 100-Hz rate. Note that the subroutine SAMPLE must incorporate delays (in the form of NOPs) to give the A/D converter sufficient time to complete a conversion. Instruction 6112 is issued before returning to the main program so that Logical 1 will be removed from IC1 in Figure 1 to enable retriggering of the one shot on the subsequent convert pulse.

CONCLUSION

Despite the fact that the State Systems interface was originally designed to receive relay closures as inputs and to drive relays on the outputs, the A/D system described here demonstrates the relatively straightforward manner in which standard TTL devices can be interfaced to the PDP-8. By relying on the general concepts embodied in the A/D converter system, our laboratory has used the State Systems hardware as a

communications interface with a PDP-10, as a high-speed paper tape punch interface, and as a driver for an X-Y plotter. In all of the instances, however, software development was accomplished in assembly language. Nevertheless, the user skilled in the use of SKED software may find convenient ways, as Butler (1975) has done, to accommodate the range of hardware options made possible by the State Systems interface.

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NOTES

1. State Systems, Inc., P.O. Box 2215, Kalamazoo, Michigan 49001.
2. PDP is a registered trademark of Digital Equipment Corporation.
3. Datel Systems, Inc., 1020 Turnpike Street, Caton, Massachusetts 02021.
4. Siliconix Inc., 2201 Laurelwood Road, Santa Clara, California 95054.
5. Burr-Brown, International Airport Industrial Park, Tucson, Arizona 85734.