IBM 5028 operation station. The 5028 sells for \$2,240 and the smallest System/7 configuration is priced at \$16,060 (rental is \$352/month), including processor, a 2,048-word memory, and one I/O module. Memory is expandable to 16,384 and the processor has a word length of 16 bits. Memory cycle time is 400 nsec. The logic circuits switch in 8-12 nsec.

The successful Data General minicomputer line (over 700 NOVAs and Supernovas have been installed) has been expanded to include the NOVA 1200, NOVA 800, and the Supernova SC. The NOVA 1200 uses LSI circuits along with a high level of MSI in the central processor. The basic price of \$5,450 includes a 4,096-word by 16-bit word core memory, direct memory access (DMA) channel, and a Teletype interface. Cycle time is 1.2 microsec, effectively 2½ to 3 times faster than NOVA, and the price is almost one-third less than that of the NOVA. The 1200's central processor is built on a single 15-in. square printed circuit board, as is the 4-k core memory. First deliveries are scheduled over the first 6 months of 1971.

The NOVA 800 is a fully parallel minicomputer with an 800-nsec cycle time and is designed for applications with high input/output requirements. Cost of the 800 is \$6,950 including a 4,096-word by 16-bit core memory, DMA channel, and Teletype interface. The Supernova SC has a new 300-nsec all-monolithic memory. Execution time for arithmetic and logical instructions is also 300 nsec: a single instruction cycle. The basic configuration costs \$11,900. All three machines are compatible with each other and with NOVA and Supernova. Software is common to all, and interfaces to peripherals are interchangeable.

Note: There has been a drop in minidisk prices, with the cost per bit down as low as 0.06 cents.

There are now over 75,000 computers in the U.S.

Note

Comparator combines analog-logic function

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Control of events which are

Fig. 1. Comparator circuit.

contingent on response amplitude during a time window may be controlled by this inexpensive circuit. The usual method of accomplishing this control requires an amplifier, Schmidt trigger, AND gate, flip-flop, and a driver.

The comparator circuit shown in Fig. 1 requires two integrated circuits, two transistors, and two diodes. Analog inputs varying more than 20 mV from the set reference voltage will be detected. The analog input impedance is greater than 50 k ohms. The analog circuit was capacitively coupled because of the need for isolation of the input from a dc offset. The unit could be directly coupled if a frequency response lower than 3 Hz was necessary and there was no problem of baseline shift. Logic circuits with "0" logic levels between -4 and -25 V and "1" logic levels between 0 and -1 V may be used for the enable and reset inputs. Examples of logic circuits which could be used are BRS-Foringer and Iconix. The

circuit was laid out on a printed circuit board. It is advisable to mount this circuit in a metal box to provide shielding. The cost of materials is less than \$40.

THEORY OF OPERATION

The circuit is in the inhibit stage if the enable input is at a logic "0." The output of the circuit will not change, regardless of the excursions of the analog input. The circuit is enabled by a logic "1" at the enable input. The output then may switch to the "on" state whenever the analog input exceeds the reference voltage, which may be varied by adjusting the potentiometer on one leg of the comparator. The output is an open collector of a transistor. Once the circuit has been set, the transistor will be biased "on" until reset. Resetting is accomplished by applying a logic "1" to the reset input. The enable input should be returned to a logic "0" when the reset command is given.