An inexpensive digital millisecond timer and event counter

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A simple circuit for a digital millisecond timer and event counter is described. The total cost of the unit including all components, a power supply, and an enclosure is less than \$30. Daily use in simple reaction time experiments has demonstrated the reliability of the design.

Although a number of digital timers and event counters are commercially available, high-precision solid state models often bear formidable price tags. Alternative inexpensive models are usually less accurate, noisy mechanical devices. The circuit described here employs current TTL integrated-circuit (IC) technology (Lancaster, 1974) to produce a device that is sufficiently accurate for most applications at an affordable price (approximately \$30).

CIRCUIT DESCRIPTION

At the heart of the timer circuit (Figure 1) is a 555 timer IC that generates a 1-kHz (1-msec cycle) clock signal. This signal is applied to one input of a two-input NAND gate (IC2A). The other input of this gate is connected to the output of a set/reset flip-flop constructed from two additional two-input NAND gates (IC2B and IC2C). When the start switch is closed, the flip-flop is set, and (inverted) clock pulses appear at the output of IC2A. Closing the stop switch terminates the flow of clock pulses by resetting the flip-flop. The start and stop functions operate independently; that is, the flip-flop may be reset while the start switch is still closed.

Clock pulses from the output of the switching gate

(IC2A) are applied to the input of the "1s" 7490 decade counter (IC3), where they are accumulated. The 4-bit binary output of IC3 is connected to the input of IC6, a 7447 binary-to-decimal decoder. The connection from Pin 11 of IC3 to Pin 14 of IC4 provides a cascading signal to the "10s" decade counter when IC3 resets from a binary 9 to 0. The "10s" decade counter is linked to the "100s" counter in an analogous manner. This arrangement allows the device to accumulate a maximum of 999 pulses (i.e., 999 msec); the 1,000th pulse causes all of the counters to recycle to 0. Accumulated counts (times) can be cleared out of the counters by momentarily opening the reset switch. When the unit is operated as an event counter, externally generated pulses are applied to the input of IC3. The 7447 binary-to-decimal decoders transform the binary outputs of the decade counters into a standard seven-segment format. Seven 222-ohm current-limiting resistors connect each 7447 to a Litronix DL707 (common anode) LED display.

CONSTRUCTION

In the prototype unit, IC1-IC8 and their associated components (see Table 1) were mounted on a perfboard with .100 x .100 in. (.254 x .254 cm) grid hole centers. A regulated 5-V power supply (Radio Shack 277-102) was constructed on a separate board, as was the three-digit LED display. All three boards were housed in a metal cabinet with the LED display visible behind a sheet of red plastic. Banana jacks were used to provide front panel connections for the start, stop, and event counter functions. The reset switch was also mounted on the front panel.

OPERATION

Calibration of the device for use as a millisecond timer is achieved by monitoring the clock pulses at Pin 10 of IC2A with an oscilloscope and adjusting R1 to obtain a pulse-to-pulse interval of 1 msec. Other pulse-to-pulse intervals can be obtained by selecting alternative values for R1 and C1 from readily available

Figure 1. Circuit diagram of the timer/counter. Parts layout and wiring are not critical.

Table 1
Parts List for Timer/Counter

Quantity	Item
1	IC timer (NE555).
1	Quad two-input NAND gate (7400).
3	Decade counter (7490).
3	Binary-to-decimal decoder, common anode output (7447).
3	Seven-segment LED display, common anode input (DL 707).
1	Potentiometer (50K).
26	Resistors ($\frac{1}{4}$ W: 1 1K, 2 2.2K, 2 1M, 21 220 ohm).
4	Capacitors: two .1 microF (1 mylar), two .001 microF.
1	SPST momentary contact, normally closed switch.

Table 2

Interval (sec)	R1	C1 (mF)
.01	500K	.1
.10	500K	1.0
1.00	1M	5.0

nomograms (e.g., Lancaster, 1974). Some possibly useful values are shown in Table 2. By simply adding additional sets of counters, decoders, and LED displays to the circuit, it would be possible to measure time intervals that exceed 1 sec (e.g., those typically observed

in choice reaction time experiments) while retaining millisecond accuracy. Periodic checks made over a period of 10 months (the timer shown in Figure 1 was used daily in simple reaction time experiments) revealed no detectable drift in the initial calibration. Nevertheless, it would be possible to improve the stability of the 555 clock somewhat by using a tantalum capacitor for C1 and a good 10-turn potentiometer for R1. These substitutions would increase the cost of the unit by about \$10. For roughly \$11, the 555 could be replaced with a crystal oscillator and divide-by-10 7490s. This would afford a capability equal to that of any commercially available timer.

To operate the device as an event counter, it is necessary to furnish debounced TTL pulses (+3.5 to +5.5 V) to Pin 14 of IC3 via the front panel connector. This mode of operation requires, of course, that the switching flip-flop (IC2B and IC2C) is in the reset position, so that clock pulses from the clock do not appear at the output of IC2A. Finally, when an external signal is applied to the input of IC3, the count occurs on the falling edge of the pulse.

REFERENCE

LANCASTER, D. *TTL cookbook*. Indianapolis: Howard W. Sams, 1974.

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