Digital Equipment Corporation (DEC) LSI-11

A relay driver and contact closure sensing interface for an LSI-11 DRV11 parallel I/O board

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A simple input and output circuit is described that allows users to sense contact closures and to drive relays from a Digital Equipment Corporation LSI-11 DRV11 parallel interface board or a signal-compatible equivalent.

Typically, computers cannot be connected directly to the everyday equipment in a behavioral laboratory. Parallel I/O boards do not provide the current or voltage necessary to drive light bulbs, solenoids, or even relays, and inputs are frequently noisy and the wrong voltage. The following circuits provide an inexpensive interface for a Digital Equipment Corporation (DEC) DRV11 parallel interface. The interface can sense any switch closure and the relays can be used to operate whatever device the user wishes. None of the circuitry presents more than one TTL load to the DRV11. A full discussion of the DEC DRV11, including the definition of signal names, can be found in the 1977-1978 DEC *Microcomputer Handbook* (pp. 289-299).¹

CIRCUIT DESCRIPTION

Input Logic

Figure 1 shows the input logic. Input signals are shown as logic ground routed through the normally closed contacts of a mechanical switch such as a pigeon key. Optional configurations are shown in Insets A, B, C, and D. The signals from the sensed switches attach to the interface at the "ground inputs," GI00 through GI07. All input circuits are identical to Circuit 1 (GI00 → IN00), which is discussed.

When the signal applied to the preset input of the flip-flop (U3, pin 4) goes from Hi to Lo, the set output of that flip-flop (U3, pin 5) is forced Hi. That preset input can be pulled Lo in either of two ways. As provided in the schematic, a normally closed switch holds the input to the inverter Lo, causing a Hi at the preset input. When ground is removed by opening the switch, the input of the inverter is pulled Hi by R1, causing the preset input of the flip-flop to go Lo, which in turn sets its output. The second method of setting the

flip-flop is with a normally open switch. For this type of switch the inverter in Box 1 is not used. The output of Box 2 is connected directly to its respective flip-flop (U3, pin 4 for GI00). In this configuration the pull-up resistor, R1, holds the preset input Hi and the switch closure forces it Lo, which in turn sets the flip-flop. Inset A presents a circuit which, when used instead of the inverter in Box 1, allows the user to sense either a normally open or normally closed switch. In any case, a set flip-flop presents a Hi to the DRV11 input IN00. This signal will be read when the CPU is directed to read the DRV11 register, DRINBUF.

The CPU can be directed to read the DRV11 register only when a signal is actually present by utilizing the interrupt capability of the DRV11. This is accomplished by generating a signal if any of the flip-flops are set. As can be seen in the schematic, a set flip-flop propagates a signal through the OR gates (U7 and U8) and holds the interrupt line, REQUEST B, Hi. This causes a CPU interrupt.

When the DRV11 input buffer, DRINBUF, is addressed by the CPU, a pulse occurs on the DATA TRANSMITTED line. This Hi is inverted and the output at U2 pin 6 is used to reset all the flip-flops to zero. The flip-flops are also cleared when the LSI-11 is powered up. When powered, the CPU generates the signal "INITIALIZE." This signal is inverted and its output at U2 pin 8 is used to clear all the flip-flops.

Figure 1 shows the circuit for 8 bits. By duplicating the circuit and using the parenthesized labels, another 8 bits can be added. These additional eight lines utilize the other interrupt line available on a DRV11, which is REQUEST A.

Some considerations that should be taken into account are: (1) the choice of the pull-up resistor value (at the inputs to the inverters GI00 → GI07), (2) the

Figure 1. Schematic of input interface.

option of disabling individual input lines, and (3) the possibility of voltage transients occurring on the input lines.

The value of the pull-up resistor was chosen to provide the best noise immunity, that is, preventing false switching of the input line. If the input lines are to be driven by a TTL device rather than a switch closure, R1 through R8 should be at least 1 kohm.

Sometimes it is desirable to disable individual inputs. Insets B and C show a switch that can be used in place of

Box 2 to provide this function. Inset B should be used with a normally closed input and Inset C with a normally open one. In either case, the closed switch forces the preset input of the flip-flop Hi regardless of the state of the input line.

High-voltage transients on the input lines could destroy the integrated circuits. One way of preventing this is to use the circuit shown in Inset D in place of Box 3. The 4N33 is a commonly available optoisolator that completely isolates the input from the rest of the

Figure 2. Schematic of output interface.

U1,U2 Sprague UHP 408

S1 spst

 V_{CC} U1,U2 pin 14

GND U1,U2 pin 7

 V_S 0-40V relative to GNDC1,C2 .01 μ F ceramic disk Input Logic Notes

1. Labels in parentheses denote signal names and connections for additional 8 bits of output
2. A .01 μ F capacitor is wired to +5 and GND
3. All DRV11 connections on J1
4. DRV11 connection

circuit. The value of R depends on the voltage of the external power supply and is found by using the formula shown.

Output Logic

The output logic is shown in Figure 2. It consists simply of a Sprague UHP-408 integrated circuit for each 4 bits of output. The UHP-408 is capable of driving signals of up to 40 V and sinking up to .5 A per signal as long as the total output current does not exceed 1 A per integrated circuit package. This is more than adequate for most relays.

When S1 is open (causing one input of all ANDS to go Hi), a Hi signal on the other input of an AND gate causes the associated transistor to turn on. This turns on the associated relay. All outputs may be disabled by closing S1, causing one of the inputs of each AND gate to be Lo. This disables all the transistors, which drops all the relays. The disabling switch can be used to prevent the relays from turning on during program development and when the DRV11 jumper cable is unplugged. Only 8 bits are shown; extension to 16 bits is accomplished by duplicating the circuit and using the parenthesized signal names.

When using a highly inductive device such as a relay or solenoid, a freewheeling diode is necessary to suppress transient surges that occur when the coil is switched off.

For applications requiring higher output voltages, pin-compatible devices are available. Sprague² UHP-408-1 and UHP-508 are for 70 V and 100 V, respectively. Chips including the freewheeling diode are UHP-407, UHP-407-1, and UHP-507 for 40 V, 70 V, and 100 V, respectively.

Although the circuits shown were designed for use with a DRV11, they are identical for the PDP11 DR11. They can be easily adapted to suit the requirements of almost any parallel interface that uses positive logic TTL signals.

NOTES

1. *Microcomputer Handbook* 1977-1978. Maynard, Mass: Digital Equipment Corporation, 1977.
2. *Series UHP-400, UHP-400-1, and UHP-500 power and relay drivers* (Engineering Bulletin 29, 300B). Worcester, Mass: Sprague Electric Company, 1974.

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