KIM-1 Microcomputer System

A low-cost high-speed digital data acquisition and display system

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A flexible and inexpensive data acquisition and display system based upon the KIM-1 microcomputer module is described. A simple signal-conditioning circuit and program are shown that will allow events to be counted at rates to 1,000/sec and stored in successive time bins. The program counts events from each of two event detectors and stores the count of each detector in an independent set of time bins. Up to 127 16-bit bins are available to each event detector and bin width can be varied from 1 msec to 1 min. A separate input can be used to time-lock data collection to a specific stimulus allowing poststimulus histograms or IRTs to be collected. The collected data can be sequentially displayed as a decimal number on a built-in LED display and stored for later analysis on an inexpensive audio cassette recorder.

Many behavioral science studies require a flexible high-speed data acquisition system. These range from the examination of steady-state or evoked neural activity where a neuron may fire as fast as 1,000 times/sec through the collection of data on interresponse times or activity level where responses may occur from several per second to 1 per several seconds. Commercial solid-state programming systems are available that will meet these requirements, but most are expensive and few offer a convenient method of storing collected data. The development of low-cost microprocessors has brought high-speed data acquisition within the reach of most research budgets. Many of these can be used with only minimal knowledge of electronics. The KIM-1 microcomputer module, which is available from MOS-Technology, 950 Rittenhouse Road, Morristown, Pennsylvania 19401, for approximately \$250, is ideal for high-speed data acquisition and display. The KIM-1 module is fully assembled and needs only to be connected to a +5- and +12-V power supply to be operational. It contains a built-in keyboard and six-digit light-emitting diode (LED) display with a resident monitor and debugging system stored in nonvolatile memory. A tape loading and dumping program is located in ROM and signal-conditioning circuits are hard wired so that data or programs may be stored and retrieved using a low-cost audio cassette recorder. Also available in the module are 15 programmable I/O lines and a programmable crystal-controlled timer.

As an example of the data-handling capability of this small computer, an extremely simple signal-conditioning interface is presented in Figure 1 and a program listing

Figure 1. A two-channel signal-conditioning circuit. The leading edge of a 0- to 5-V transition at the input of either flip flop sets the flip flop. The computer reads the flip flop and then resets it. The interface to the KIM-1 is a 22-pin edge connector.

is shown in Table 1 for a two-channel event counter designed specifically for monitoring neural activity. But the system can be used for any situation where the rate of occurrence of some behavior as a function of time is of interest.

Table 1
Machine-Language Program for Data Collection and Display

MAIN PROGRAM FOR DATA COLLECTION			
0000	A90F	LDA,OF	INITIALIZE DATA DIRECTION
0002	8D0117	STA,IODA	REGISTERS OF IO PORTS A & B
0005	8D0317	STA,IODB	
0008	A900	LDA,00	
000A	AA	TAX	CLEAR INDEX REGISTER
000B	85EE	STA,EE	CLEAR PASS #
000D	8DFA17	STA,I7FA	SET INTERRUPT VECTOR HI
0010	9D0002	STA,0200	
0013	9D0003	STA,0300	
0016	E8	INX	
0017	E000	CPX,00	CLEAR LOCATIONS 0200
0019	D0F5	BNE,ZERO	TO 0300
001B	A9FF	LDA,FF	
001D	8D0017	STA,PIAA	SET PIA OUTPUTS
0020	8D0217	STA,PIAB	TO ALL ONES (+5V)

Table 1 Continued

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0023 A91C      LDA,1C
0025 8DFB17    STA,17FB      SET INTERRUPT VECTOR LOW
0028 207000    START JSR,GO
002B 208600    JSR,TIMER
002E 2C0017    POLLA BIT,PIAA CHECK BIT 6 OF PIAA
0031 701A      BVS,POLLB
0033 A901      INCA LDA,01
0035 18        CLC
0036 7D0102    ADC,0201      IF FLIP FLOP A IS SET, INCREMENT
0039 9D0102    STA,0201      16 BIT COUNTER A(X). IF NOT,
003C A900      LDA,00        SKIP TO POLLB
003E 7D0002    ADC,0200
0041 9D0002    STA,0200
0044 20C400    JSR,WAIT
0047 EE0017    INC,PIAA      TOGGLE BIT 0 OF PIAA
004A CE0017    DEC,PIAA      TO RESET FLIP FLOP A
004D 2C0017    POLLB BIT,PIAA CHECK BIT 7 OF PIAA
0050 301A      BMI,REPT
0052 A901      LDA,01
0054 18        CLC
0055 7D0103    ADC0301      IF FLIP FLOP B IS SET, INCREMENT
0058 9D0103    STA,0301      16 BIT COUNTER B(X). IF NOT
005B A900      LDA,00        SKIP TO REPT
005D 7D0003    ADC,0300
0060 9D0003    STA,0300
0063 20C400    JSR,WAIT
0066 EE0217    INC,PIAB      TOGGLE BIT 0 OF PIAB
0069 CE0217    DEC,PIAB      TO RESET FLIP FLOP B
006C 4C2800    REPT JMP,START REPEAT
006F EA        NOP          DO NOTHING NOT ACCESSED

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THE FOLLOWING SUBROUTINE CHECKS PERIPHERAL INPUT ADAPTOR B TO SEE IF BIT 6 IS SET. SETTING BIT 6 STARTS THE DATA COLLECTION PERIOD. IF BIT 6 OF PIAB IS ZERO THE BIN POINTER IS SET TO BIN ONE, THE BIN WIDTH TIMER IS SET AND THE COUNTERS ARE DISABLED.

```

0070 2C0217    GO BIT,PIAB  POLL PIAB
0073 1001      BPL,01      IS BIT 6 SET?
0075 60        RTS         IF SO RETURN TO MAIN PROGRAM
0076 A900      LDA,00
0078 AA        TAX         IF NOT: CLEAR INDEX,
0079 85ED      STA,TEMPX    CLEAR TEMPX
007B A9F1      LDA,F1
007D 85EC      STA,EC
007F A9F3      LDA,F3      SET BIN WIDTH TIMER TO 1 MIN.
0081 8D4717    LDA,1747
0084 D0EA      BNE,G0      LOOP UNTIL BIT 6 IS SET

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THE FOLLOWING SUBROUTINE EXAMINES THE BIN WIDTH TIMER AND IF ONE MINUTE HAS ELAPSED, THE INDEX REGISTER (X) IS INCREMENTED TWICE TO FORM A NEW TIME BIN FOR THE TWO EVENT DETECTORS TO LOAD. THE INDEX REGISTER IS THEN DISPLAYED FOR 3 MSEC. WHEN ALL 127 TIME BINS HAVE BEEN ENABLED, A WAIT LOOP IS ENTERED AND THE NUMBER OF PASSES THROUGH THE TIME BINS IS DISPLAYED. OPENING OR GROUNDING BIT 6 OF PIAB EXITS THE WAIT LOOP.

```

0086 2C4717    TIMER BIT,1747 IS TIME UP?
0089 1009      BPL,RET      IF NOT RETURN
008B A9F3      LDA,F3      IF TIME IS UP, RESET
008D 8D4717    STA,1747    MSEC TIMER TO F3 MSEC.
0090 C6EC      DEC,EC      DECREMENT SEC TIMER
0092 F001      BEQ,INX
0094 60        RTS         IF SEC TIMER IS ZERO INCREMENT
0095 A6ED      INCX STX,ED   X TWICE CREATING A NEW
0097 E8        INX         TIME BIN
0098 E8        INX
0099 86ED      STX,ED
009B 8A        TXA         HAS LAST BIN BEEN ENABLED?
009C 38        SEC         IF SO, STOP AND DISPLAY #
009D E9FE      SEC,FE      OF PASSES THROUGH THE BINS
009F D014      BNE,RBIN
00A1 E6EE      INC,EE      INCREMENT PASS NUMBER
00A1 A900      DISPP LDA,00
00A5 85FA      STA,FA
00A7 85FB      STA,FB
00A9 A5EE      LDA,EE
00AB 85F9      STA,F9
00AD 201F1F    JSR,1F1F    DISPLAY PASS NUMBER
00B0 2C0217    BIT,PIAB    CHECK BIT 6 OF PIAB, IF SET
00B3 30F8      BMI,DISPP   CONTINUE DISPLAY
00B5 A9F1      RBIN LDA,F1
00B7 85EC      STA,EC      RESET BIN TIMER
00B9 A5ED      LDA,ED
00BB 85F9      STA,F9
00BD 201F1F    JSR,DSPLY   DISPLAY NEW BIN NUMBER
00C0 A5ED      LDA,TEMPX   FOR 3 MSEC
00C2 AA        TAX         RESTORE X REGISTER
00C3 60        RTS         AND RETURN

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THIS SUBROUTINE PRODUCES A 30 MSEC DELAY

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00C4 A0FF      WAIT LDY,FF  SET Y = FF
00C6 208600    PAUS JSR,TIMER WAIT A WHILE
00C9 208600    JSR,TIMER WAIT LONGER
00CC 88        DEY        DECREMENT Y
00CD D0F7      BNE,PAUS   IF Y > 0, REPEAT
00CF 60        RTS         IF NOT RETURN

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MAIN PROGRAM FOR DATA DISPLAY

Table 1 Continued

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0102 8DFA17    STA,17FA
0105 A901      LDA,01      SET INTERRUPT
0107 8DFB17    STA,17FB    MASK
010A A900      LDA,00
010C 85D0      STA,D0
010E 85D1      STA,D1
0110 85D2      STA,D2
0112 85D3      STA,D3      SET DATA STORAGE
0114 85D4      STA,D4      LOCATIONS TO 0
0116 EA        NOP
0117 EA        NOP
0118 AA        TAX         SET X = 0
0119 EA        NOP
011A BD0002    START LDA,0200
011D 85E6      STA,E6
011F BD0112    LDA,0201    GET 16 BIT DATA
0122 85E7      STA,E7      FROM
0124 86ED      STX,ED      LOCATION 0200 + X
0126 204001    JSR,DCML    CONVERT TO BCD
0129 A5E0      LDA,E0
012B 85FB      STA,FB
012D A5E1      LDA,E1
012F 85FA      STA,FA
0131 A5E2      LDA,E2
0133 85F9      STA,F9
0135 201F1F    JSR,DSPLY   DISPLAY 5 DIGIT NUMBER
0138 A5ED      LDA,ED
013A AA        TAX
013B 4C1A01    JMP,START   CONTINUE DISPLAY

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THIS SUBROUTINE CONVERTS THE 16 BIT BINARY NUMBER STORED IN LOCATIONS E6 and E7 INTO A 5 DIGIT DECIMAL NUMBER STORED IN LOCATIONS E0, E1, and E2.

```

0140 F8        SED         SET DECIMAL MODE
0141 98        TYA
0142 48        PHA
0143 8A        TXA         PUSH X AND Y INDEX
0144 48        PHA         ONTO STACK
0145 A900      LDA,00
0147 A206      LDX,06
0149 95DF      ZERO STA,DF  ZERO LOCATIONS E0 to E5
014B CA        DEX
014C D0FB      BNE,ZERO
014E E6E5      INC,E5      LOAD FIRST FACTOR
0150 A5E7      LDA,E7      GET LOW DATA BYTE
0152 48        PHA         PUT IN ON STACK
0153 A008      LDY,08      SET NUMBER OF BITS
0155 68        PULL PLA     PULL DATA
0156 4A        LSR-A      SHIFT RIGHT
0157 48        PHA         STORE IN STACK
0158 900C      BCC,NEXT    IF CARY = 1 CONTINUE
015A A203      LDX,03
015C 18        PHD
015D B5E2      CONV. LDA,E2
015F 75DF      ADC,DF
0161 95DF      STA,DF      IF NOT ADD CONVERSION FACTOR
0163 CA        DEX         TO DECIMAL MEMORY LOCATIONS
0164 D0F7      BNE,CONV.   AND REPEAT
0166 A203      NEXT LDX,03
0168 18        PHP
0169 B5E2      CONV. LDA,E2
016B 75E2      ADC,E2      DOUBLE CONVERSION
016D 95E2      STA,E2      FACTOR AND REPEAT
016F CA        DEX
0170 D0F7      BNE,CONV.
0172 88        DEY
0173 D0E0      BNE,PULL
0175 68        PLA
0176 A5E3      LDA,E3      CHECK HIGHEST CONVERSION
0178 D004      BNE,END     FACTOR. IF = 0 EXIT
017A A5E6      LDA,E6      OTHERWISE REPEAT
017C D0D4      END  BNE,BITT CONVERSION PROCEDURE
017E 68        PLA
017F AA        TAX
0180 68        PLA
0181 A8        TAY         RESTORE REGISTERS
0182 D8        CLD         CLEAR DECIMAL MODE
0183 60        RTS         RETURN TO MAIN PROGRAM

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INTERRUPT ROUTINE TO ADVANCE DISPLAY TO NEXT 16 BIT TIME BIN WHEN THE ST SWITCH IS PRESSED ON THE KIM-1 KEYBOARD

```

0184 48        PHA
0185 8A        TXA
0186 48        PHA         PUSH A, X AND Y
0187 98        TYA         REGISTERS ONTO STACK
0188 48        PHA
0189 A5ED      LDA,ED
018B AA        TAX         FETCH INDEX VALUE
018C E8        INX
018D E8        INX         INCREMENT INDEX BY 2
018E 8A        TXA         STORE X IN TEMPORARY
018F 85ED      STA,ED      LOCATION
0191 68        PLA
0192 A8        TAX
0193 68        PLA
0194 AA        TAY         PULL A, X, AND Y
0195 68        PLA         REGISTERS FROM STACK
0196 40        RTI         RETURN

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0100 A984 LDA,84

The signal conditioner shown in Figure 1 consists of a dual Type D flip flop that is set by the leading edge of a transition from ground to +5 V. The state of each flip flop is examined sequentially by the computer, and if it is found to be set due to the occurrence of an event, a counter is incremented and the flip flop is reset in preparation to receive another count. Switch debouncing is accomplished in software.

The program shown in Table 1 beginning at Location 0000₁₆ and extending to Location 00CF₁₆ begins by defining an area of memory as two sets of 127 16-bit counters. These counters act as "time bins" into which counts may be placed when an event is detected by the signal-conditioning circuit. A bin pointer controls which time bin the count will effect and the length of time that a given bin is opened is controlled by a bin width timer.

When the program begins, the following events occur: The counters in each time bin are set to zero, the bin pointer is set to the first time bin for each of the two separate event detectors, the bin width timer is set to a programmed bin width, and the computer then waits for a +5-V signal to appear at Pin 15 of the application connector. Raising Pin 15 to +5 V enables the counters in Bin 1 and starts the bin width timer. At this point, every time an event occurs, a count is entered into the first of the set of time bins representing the event detector that was activated. When the bin width timer indicates that a preset time interval has passed, the bin pointer is set to enter subsequent counts into the second time bin for each of the two event detectors. This process is repeated each time interval until all 127 time bins for each of the event detectors has been enabled. At that time, the counters are disabled and a 1 is displayed on the LED readout, indicating that one pass through the time bins has been completed. If another pass through the time bins is desired (as in producing a poststimulus histogram), Pin 15 may be opened or grounded. This resets the bin pointer to Bin 1 and disables the counters. When Pin 15 is returned to +5 V, the counters are enabled and the bin width timer is started; the data collection process continues as described above. This has the effect of adding the counts acquired during the second pass through the time bins to those already present from the first pass. When all 127 time bins have been enabled, a 2 appears in the LED display, indicating that two complete passes through the time bins have been completed. This process can be repeated as often as desired, with the restriction that the number of counts in any time bin does not exceed 65,536. Data collection can be timelocked to an external stimulus by raising Pin 15 to +5 V when that stimulus occurs, and maintaining it at that voltage until the data collection period is over. It should then be grounded or opened in preparation for the next stimulus. Alternatively, the event detector may be tied to Pin 15 in such a way that the occurrence of an event

enters a count into the time bin that was enabled during its occurrence and Pin 15 is opened or grounded for at least 60 msec. This causes one count to be deposited, the bin pointer reset to Bin 1, and the bin width timer restarted. This procedure collects interresponse times (IRT) with an accuracy determined by the programmed bin width. While there are two sets of time bins, they are both controlled by the same bin pointer and, therefore, IRTs can only be collected meaningfully from one event detector. Poststimulus histograms may be generated for two separate events provided the stimulus occurs simultaneously in both instances.

Bin width can be set between 1 msec and 1 min, allowing high timing accuracy for short time intervals (at 10 msec, data can be collected for 1.27 sec, while at 1-min bin width, it can be collected for 127 min). At the 1-min bin width, events can be stored at up to 1,000/sec for 127 min.

When events are expected to occur at a rate greater than 10/sec, the software debouncing system, which inserts a 30-msec delay between the detection of an event and resetting the flip flop, must be disabled. This can be accomplished by entering EA₁₆ in memory Locations 44-46₁₆ and 63-65₁₆. This modification causes the program to skip the debounce routine, and it then polls the event detector approximately twice each millisecond.

Bin width is controlled by two timers and may be changed in multiples of 245 msec by altering the contents of memory Location 00B6₁₆. If this location is set to 01, bin width will be 245 msec. For narrower time bins, the basic 245-msec interval described above may be altered in 1.025-msec increments by changing Locations 0080₁₆ and 008C₁₆. If these memory locations are set to 01, the bin width is 1.025 msec times the value loaded into memory Location 0066₁₆. If more accuracy is needed at low bin widths, the 1.025-msec interval can be changed to .064 msec, .008 msec, or .001 msec by changing the contents of memory Locations 0082₁₆ and 008E₁₆, as described in the user's manual. By manipulating the three bin width adjustments, accuracy within a few microseconds can be obtained for times between 1 msec and 1 min.

To use the storage area of the microcomputer to maximum advantage, the data is stored in binary rather than decimal form (in BCD form only 9,999 events could be stored in each bin). For convenience, a program is loaded at Address 0100₁₆ that will convert the data stored in Bin 1 of Counter 1 (Locations 0200 and 0201₁₆) into a five-digit decimal number and display it on the built-in LED display (Gordon, Note 1). Depressing the start button causes the data in Bin 2 (Locations 0202 and 0203₁₆) to be displayed. By repeatedly depressing the start button, the contents of each data bin can be sequentially displayed. To display the data in Counter 2, which occupies memory locations from 0300 to 03FD₁₆, 03₁₆ is entered into

memory Locations 011C₁₆ and 0121₁₆ and the process described above is repeated.

While the system was designed specifically to collect data on rates of neural activity, any device capable of initiating a switch closure or of producing a pulse of greater than 50 nsec may be used to actuate the event counter.

The contents of the two sets of event counters may be stored on almost any inexpensive audio cassette recorder for later analysis. A C-30 cassette stores approximately 10 complete sets of data. The procedures for storage and retrieval of data from tape are described in the handbook and programming manual that accompany the KIM-1.

For those with access to a Teletype, an interface is built into the KIM-1 to allow the data to be printed out with only minor program changes. Clearly, this is a versatile data acquisition and storage system that should find increasing use in behavioral science research.

REFERENCE NOTE

1. Gordon, H. T. Listing of third version of HEDEC. In E. C. Rehnke (Ed.) *KIM-1/6502 User Notes*. Vol. 1, No. 20, 1966. 7656 Broadview Rd., Parma, Ohio 44134.

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