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# COMPUTER TECHNOLOGY

# Control of CRT intensity via Apple II software

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**An inexpensive, easy-to-build device for the Apple II microprocessor is described. The modification permits software control of four levels of relative screen intensity (contrast) settings for any video monitor. The relationship of the technology to choice reaction time and perception research is briefly indicated. Principles governing operation of the modification are also discussed. Finally, a set of step-by-step instructions for building the device is provided.**

The purpose of this brief report is to describe an inexpensive modification of the Apple II designed to control the screen intensity of a video monitor or cathode-ray tube (CRT) device. The modification adapts to the 16-pin game input-output (I/O) port on the Apple II motherboard and, when properly installed, still permits further access to the game I/O and game-paddle connections. A diagram of the modification is shown in Figure 1. Total cost is under $20. Hardware design and layout differences between the Apple II and the Apple IIe suggest that the device described is not directly adaptable to the Apple IIe.

When the device is installed, the command POKE −16293, 0 will dim the intensity (reduce screen contrast) and POKE −16294, 0 will restore the screen to normal, full intensity. The alternative POKEs, −16295 and −16296, will permit an additional dimming level that will sum with the effects of the first. The potentiometers may also be adjusted manually to obtain any degree of dimming change desired.

Choice reaction time research concerned with the effects of intensity and decision time (e.g., Becker & Killion, 1977; Shwartz, Pomerantz, & Egeth, 1977; Adams-Westcott & Hochhaus, Note 1) indicates the plausibility of the contrast manipulation as a way of learning about the stages and subprocesses of human information processing. (See Sanders, 1980, 1983, for recent reviews of related literature.) The precision of the device and its digital and analog flexibility enhance its usefulness in perception research.

## THEORY OF OPERATION

The composite video signal, which the Apple II sends to the video monitor, is originally generated as three separate digital signals: the color burst, the synchronization signal, and the picture-information signal (see Figure 2). The three signals are summed in an analog fashion to produce the composite signal. To accomplish this, each signal source generates an output through its own resistor (R6, R7, and R8, respectively, on the Apple II). The three signals then converge at a common summation point to form the composite video signal (refer to Figure 2).

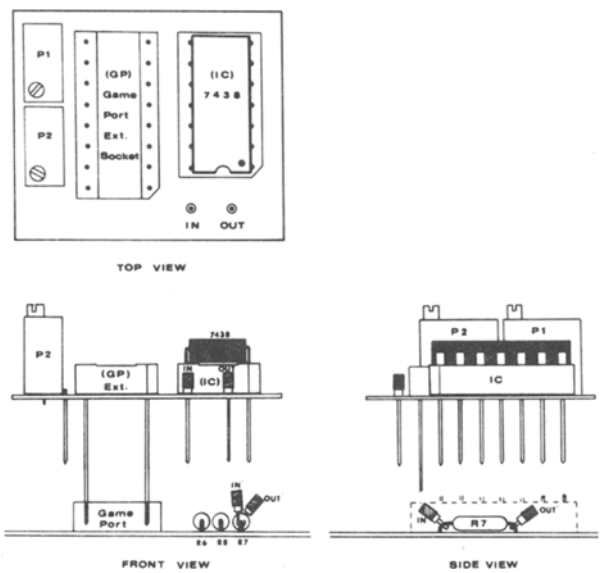


**Figure 1. Diagram of Apple II intensity modification with extension game-port socket, potentiometers, integrated-circuit chip, and gold socket pins.**

As digital signals, the synchronization and picture-information signals may be at only one of two logic states at any given time: either "low" (approximately 0.7 V) or "high" (approximately 2.5 V). However, as can be seen from Figure 2, the composite video signal requires several levels of voltage to operate properly. The lowest level of voltage (0 V) indicates blanking and synchronization characteristics of the video signal. The 0.7-V level, when first encountered, indicates the reference voltage for the darkest level of brightness (i.e., black). The highest voltage (2.5 V) represents the level of the brightest dot (white) that may be encountered.

In order to provide reduced stimulus contrast without

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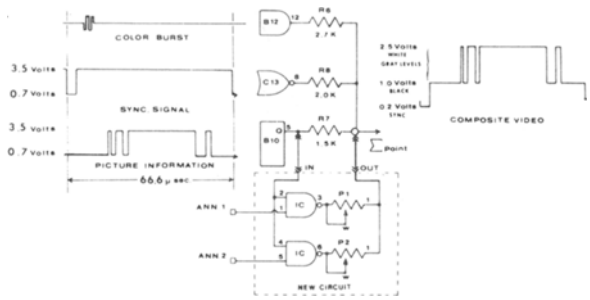


**Figure 2. Schematic diagram of Apple II intensity modification.**

disturbing the synchronization pulses or color-burst information, only the picture information in the composite signal should be altered. As shown in Figure 2, by adding a signal to the summing point that is identical to the picture-information signal but that is opposite in sign, one can subtract any portion of the picture-intensity information desired without disturbing the other two signals. The picture-information signal from the digital output of integrated circuit ICB-10, pin 5, therefore, is inverted using two, two-input NAND gates. The values of the current-limiting resistors (P1 and P2) used to feed two inverted digital signals (the canceling signals) to the summing point determine the amount of picture dimming produced. Two trim potentiometers (P1 and P2 in Figure 2 and Figure 3) determine the amount of dimming produced by each cancelation signal. Adjustment of a small setscrew on each potentiometer determines the amount of cancelation signal provided by each component potentiometer circuit (see Figure 2). In effect, the device provides two independent circuits or mechanisms for regulating the picture contrast.

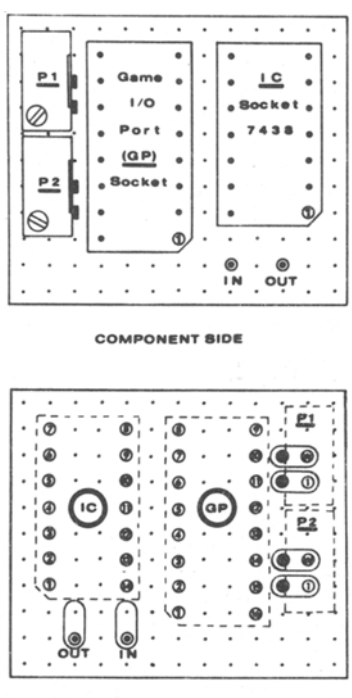


**Figure 3. Guide to wiring diagram. (See Table 2.)**

## LUMINANCE MEASUREMENTS

The device was used to reduce severely the picture-information contrast and was calibrated with a Macbeth illuminometer. Two human observers each carried out four ascending and four descending adjustment trials with the illuminometer. The following values of luminance each represent a mean of 16 measurements. Under standard viewing conditions, the luminance readings were 1.96 cd/m$^2$ (black) and 7.24 cd/m$^2$ (white). When the present device was used to provide maximal reduction of stimulus contrast while maintaining screen legibility of uppercase alphanumeric characters, the respective values were 2.41 and 2.73 cd/m$^2$.

## SOFTWARE COMMANDS

The use of two two-input NAND gates provides a mechanism with which to switch the dimming function on and off through program control. Annunciator output (#1) on the game I/O port is used to control the addition of the first component of the canceling signal to the final composite video signal. Annunciator output #2 controls the addition of the second, independent canceling signal. When the first annunciator is set to 1 (high) by POKE −16293, 0 and the picture-information signal is also high (i.e., currently displaying a dot), then the output of the NAND gate will be forced low, thereby providing a current-sink point for extracting picture-intensity information from the composite video signal at the summing point. To return the screen to its original setting, the command POKE −16294, 0 is used. The second annunciator (activated by POKE −16295, 0 and canceled by POKE −16296, 0) permits subtraction of the second, independent component of the picture-intensity information. When both annunciators are activated, their effects on signal intensity are additive. To keep the output of the NAND gates from going high (and thus distorting the synchronization signal when either input is low) two open-collector outputs IC-7438 (NAND gates) are used. Hence, the open-collector outputs will not send (or source) current when in the high state. When low, they provide two current sinks that allow extraction of the positive picture-intensity information.

## CONSTRUCTION

A parts list is given in Table 1. The 3.2 x 2.8 cm perforated, electrical-mounting board is filed smooth around the edges. The quick-solder pads are affixed to the bottom of the board with their adhesive surfaces, as shown

**Table 1**
**Parts List and Tools for Apple II Intensity Modification**

| Quantity | Part No. | Manufacturer | Cost | Description |
|---|---|---|---|---|
| | | | Parts | |
| 1 | VCT-64P44 | Vector | $1.00 | Perforation board (3.2 x 2.8 cm) |
| 2 | 64W53 | Spectral | $3.00 | 5 K, 20-turn trim potentiometer |
| 1 | 276-1993 | Radio Shack | $1.00 | 3-level, 14-pin DIP wire-wrap socket |
| 1 | 276-1994 | Radio Shack | $1.25 | 3-level, 16-pin DIP wire-wrap socket |
| 1 | DM7438 N | National Semiconductor | $0.50 | Quad, 2-input NAND gate with open-collector outputs |
| 1 ft | 281294 | Radio Shack | $2.19 | 20-AWG hook-up wire |
| 4 ft | 278501 | Radio Shack | $2.39 | 30-AWG wire-wrap wire |
| 4 | VCT-T42 | Vector | $0.03 | Wire-wrap pins |
| 2 | VCT-R32 | Vector | $0.25 | Wire-wrap socket pins |
| | | | Tools | |
| | | | | Hand wire-wrap tool |
| | | | | Wire stripper (20 AWG) |
| | | | | Small screwdriver |
| | | | | Small saw for cutting perforation board |
| | | | | Small diagonal cutters for trimming wire-wrap pins |
| | | | | Fine sandpaper or wire brush |
| | | | | Small soldering iron |

in Figure 3. The pads are cleaned with a wire brush or are burnished with extra-fine sandpaper until they are clean and ready to be soldered. The wire-wrap pins are inserted as shown in Figure 3 and are soldered in place. Next, the gold socket pins are inserted and mounted, and the trim potentiometers are soldered. Care should be used in installing the sockets, with the pin-1 mark on the socket properly oriented (Figure 3).

The pins of the 14-pin DIP socket are cut to 1 cm in length to prevent them from touching components on the Apple II board below. A wire-wrap tool may be purchased for under $6 and should be used to connect the origin and destination of each wire as shown in Table 2. Each wire wrap should consist of two turns of insulation followed by about seven turns of bare wire around each pin.

Next, a gold socket pin is soldered to each end of resistor R7 on the Apple II motherboard. The SN7438 integrated circuit (IC) is inserted into the 14-pin DIP socket, with pin 1 properly oriented. The edge of the Apple II motherboard should be grasped firmly and the 16 pins carefully worked into the game I/O port of the Apple II. To avoid dislodging the wire wraps, pressure should be applied only to the 16-pin socket and not to the perforated, electrical-mounting board. Again, proper orientation of pin 1 must be made. Two 8-cm lengths of 20-AWG (20-ga) wire are cut and 0.5 cm of insulation from each end is stripped. Using one of the cut wires, the input pin (IN) of the new device is connected to the gold socket pin of resistor R7 at the end of the resistor closest to the Apple II keyboard. Similarly, the output pin (OUT) of the new device is connected to the gold socket pin of resistor R7 at the end of the resistor that is closest to the back of the Apple II. Finally, reference

**Table 2**
**Wiring Diagram for Apple II Intensity Modification**

| From | To | Comments |
|---|---|---|
| GP-1 | IC-14 | Vcc +5 V |
| GP-8 | IC-7 | GND 0 V |
| GP-15 | IC-1 | ANN #1 |
| GP-14 | IC-5 | ANN #2 |
| IC-2 | IC-4 | Picture signal from IC B10-5 |
| IC-4 | IN | Picture signal from IC B10-5 |
| IC-3 | P1 W-2 | Inverted picture to wiper of potentiometer, P1 |
| IC-6 | P2 W-2 | Inverted picture to wiper of potentiometer, P2 |
| P1-1 | P2-1 | Sum of two reduced inverted video signals |
| P2-1 | OUT | Sum of two reduced inverted video signals to output socket |
| IC-12 | IC-13 | Tie all unused inputs to ground (0 V) |
| IC-9 | IC-10 | Tie all unused inputs to ground |
| IC-10 | IC-12 | Tie all unused inputs to ground |
| IC-9 | IC-7 | Tie all unused inputs to ground |

*Note–GP = game-port socket; IC = SN7438 socket.*

should be made to the POKE operations described above to test the device.

To disable the modification, the computer is turned off and the 7438 integrated circuit (IC) is removed. This frees the two occupied annunciators (ANNs 1 and 2) for other uses and removes all active loads from the video signals.

This modification results in a useful device for laboratory research programs.

## REFERENCE NOTE

1. Adams-Westcott, J., & Hochhaus, L. *Tests of the cascade model of word recognition.* Unpublished manuscript, Oklahoma State University, Stillwater, Oklahoma, 1983.

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