A large-scale expandable I/O port interface for the TRS-80 microcomputer

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Described is a large-scale expandable input/output port interface for the Tandy Corporation TRS-80 microcomputer.

Microcomputers are potentially very useful to the researcher for on-line control of experiments and data collection. One hurdle that must be overcome before such a system is implemented, however, is the need to purchase or build the interface necessary for communication between the computer and peripheral apparatus. Although a few large port systems are available commercially, they are often more expensive than the microcomputer itself. The present article describes a versatile and large-scale input/output (I/O) port interface that can be constructed in an electronics shop at a fraction of the cost of commercially available systems.

HARDWARE DESCRIPTION

The interface consists of three modules: (1) mother-board, (2) input card, and (3) output card. It can be plugged directly into the Model I expansion interface bus extension by a 40-conductor ribbon cable with a socket connector at one end and a card-edge connector on the other, such as Digi-Key Model 924150-24. This interface can also be used with the TRS-80 Model III with the addition of cable that makes the Model III 50-pin bus compatible with the Model I 40-pin bus. Such a cable is available from Alpha Products or can be constructed by reference to the Model I and Model III technical manuals, available from Radio Shack, which list the pin-out configuration for each microcomputer. The motherboard contains buffers for address lines (74LS08), the data bus (74LS125), and the I/O function-select lines (74LS125). Figure 1 shows a functional block diagram of this board with component identification numbers. Figure 2 shows a schematic of the two chips used as buffers on the motherboard. In addition, the motherboard has 40-pin female edge-card connectors (Texas Instruments Model H4111 31-22) that hold the actual input and/or output port cards. Figure 3 shows the physical layout of the motherboard when printed on circuit board.

Both the input and the output cards use the 8212 chip as their basis (shown as U1 in Figures 4 and 5). The input cards are optically coupled, providing electrical isolation from external apparatus. The output cards are connected to peripheral apparatus by TTL

Figure 1. Functional block diagram of the motherboard containing address and data bus buffers.

Figure 2. Schematic of the data buffers (74LS125) and address buffers (74LS08) used on the motherboard.

Figure 3. Physical layout of the top and bottom of the motherboard as appears on printed circuit board.

Figure 4. Physical layout of top and bottom of the input port card as appears on printed circuit board.

Figure 5. Physical layout of top and bottom of the output port card as appears on printed circuit board.

drivers. These open collector drivers can sink 17 mA at 30 V dc, providing sufficient current to drive most relays; moreover, they are compatible with most solid state device inputs. Figures 6 and 7 show the functional block diagrams for each of these cards, respectively. These cards are address selectable by using a jumper wire from one of the address lines (A0-A7) to Pin 13 of the 8212 chip shown in Figures 6 and 7. Figures 4 and 5 show printed circuitry for these cards, respectively.

This port system can accommodate up to four I/O cards. However, it can be easily modified to accommodate up to eight port cards of each type, by extending the number of card-edge connectors placed on the motherboard. This can be accomplished by printing multiple copies of the motherboard and using jumpers to connect one section of the motherboard to extensions. Thus, this system can accept eight input and eight output cards, for a maximum of 64 bits of I/O. It should be noted that any combinations of I/O cards can be used as needed for the specific application, so that it is possible to configure a system with three

output cards and one input card or, conversely, with one output and three input cards. The configuration of the port is solely determined by the type of cards placed in the motherboard.

SYSTEM OPERATION

Output Mode

The user can control output to peripheral apparatus by BASIC or assembly language programs. The form of the immediate controlling statement in each of these languages is OUT N1, N2, where N1 represents the address of the port selected and N2 is the 8-bit word to be sent to the peripheral device. Upon execution of the command, the N1 value is placed on the lower eight Z80 address lines, the N2 value on the data bus, and the OUT signal line is activated. The simultaneous occurrence of the OUT signal and activation of one of the address lines at the 8212 chip will result in the contents of the data bus being copied into the 8212 data buffers. These in turn activate the TTL drivers, which provide a ground

Figure 6. Functional block diagram of the input port card containing the 8212 port chip and optical isolators.

Figure 7. Functional block diagram of the output port card containing the 8212 port chip and TTL drivers.

Figure 8. Schematic of the optical isolators used on the input port card (U2-U9).

signal that can be used to operate an external device, such as a solid state or electromechanical relay. The TTL (7406) drivers are shown as U2 and U3 in Figure 5.

Input Mode

The CPU can access a byte on the input port via the BASIC statement $X = \text{INP}(N1)$ or by an assembly statement $\text{IN A},(N1)$, where $N1$ is the address of the input port to be accessed. These commands place the $N1$ value on the address lines and activate the IN signal buffer, which in turn activates the IN signal on the 8212 port chip. Upon the simultaneous occurrence of these signals at the port, the status of the output buffers of the 8212 is placed on the data bus, which is transmitted through the data bus buffers into the CPU. Each bit in the I/O input word represents a peripheral signal, where ground is used to activate the LED in the optoisolators that translate the signal to the voltage used by the 8212 chip. A schematic of the optical isolators used as U2-U9 in Figure 4 is shown in Figure 8.

AVAILABILITY

A template suitable for the photographic etching process, a parts list, and instructions necessary for complete assembly of this port system are available from the authors at cost.