A high-gain, low-noise amplifier for EEG

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This paper describes an amplifier for an electroencephalograph with gain of 1×10^4 to 1×10^6 and made entirely of commercially available IC components. The two-stage amplifier has a preamplifier stage with fixed gain of 1000, and a second stage with variable gain from 1 to 100. The final stage, an anti-aliasing filter, adds a gain of 10 to the signal. The circuit has high common mode rejection, low input bias current, very low noise characteristics, low offset voltages, and offset nulling capability built into the circuit.

The electroencephalographic (EEG) signal occurs at the scalp in the range of a few to 100 μV . Since most pen drivers or A/D converters require a signal in the range from -5 to $+5$ V, or occasionally from 0 to $+10$ V, it requires a gain of 10,000 or more to obtain a useful signal. There are several problems associated with achieving this degree of amplification with so small a signal source. The EEG signal occurs in the range of 0-24 Hz, and in this low-frequency range most operational amplifiers suffer from rapidly increasing noise levels. This noise, introduced in the input stage of the amplifier, is carried through and amplified by the later stages, resulting in a serious degradation of the signal output.

Very low input noise levels can be achieved by building an amplifier from separate components, such as the National Semiconductor LM-194 matched transistor pair, or separate low-noise amplifiers, such as the precision Monolithics (PMI) OP-27 or OP-37. However, this approach requires careful matching of resistor ratios, separate offset adjustment for each component, a high parts count, and, in the case of discrete transistors, a high level of input bias current.

Recently, IC "instrumentation amplifiers," such as the PMI AMP-01 and MAT-02, Analog Devices AD-521, or Motorola MC34084 and MC35085, which overcome many of the basic problems, have become available. Most have balanced differential inputs, very low noise characteristics in the low-frequency range, low input bias current requirements, low offset voltages, and offset nulling capability built into the circuits. The circuit described here uses two such instrumentation amplifiers, one as a preamplification stage, and the other as a variable-gain second stage. The 50- μV EEG signal can be amplified to deliver a 0- to 10-V signal at the output.

The heart of the amplifier is the AMP-01 (Figure 1). The AMP-01 has a $1/f$ corner at about 8 Hz, giving it a noise density in the low-frequency range of a few nanovolts per root Hertz. Input bias current is about 4 nA, so there is very little current drain through the input source. The gain of the AMP-01 is given by:

$$\text{Gain} = 20(R_s/R_g).$$

In this case, $R_s = 10\text{K}\Omega$ and $R_g = 200\Omega$, giving a fixed gain of 1000. At this gain, the differential input provides a common mode rejection ratio of 125 dB. Some offset voltage is introduced at both the input and output stages of the amplifier. This offset voltage can be removed by the trim adjustments at $V_{\text{OOS Null}}$ and $V_{\text{IOS Null}}$.

Because of minor differences in electrode placement and other factors, an inherent offset voltage of a few millivolts may exist between the two input leads. In addition, the drift in offset voltage between the two leads may be as much as 10 μV per second (Graham, 1965; Strong, 1970). To remove this offset voltage, the input electrodes are ac coupled to the amplifier through the 10.0- μF nonpolarized capacitors. These have the effect of removing any offset voltage between the two input leads, and also serve to protect the subject from any currents that might arise due to system failure. At very low frequencies, the increasing reactance of the 10- μF capacitors in series with the source resistance causes an unbalanced contribution of noise voltage to the two sides of the differential input, giving rise to slow, random thermal drift of the input offset voltage (Graham, 1965). This drift is removed at the second amplification stage by means of an integrator circuit (see below, Figure 3).

The PMI OP-7 amplifier (Figure 1) is used as a shield driver to bootstrap the input signal common mode voltage to the cable, which reduces capacitive coupling between the shield and the input leads. The input signal applied across pins 18-3 of the AMP-01 is passed through unity-gain transistors internal to the circuit and appears

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Figure 1. First-stage amplifier, showing input configuration and shield driver.

Figure 2. Unity-gain inverter.

on pins 1 and 2. The resistor network across these pins averages the composite signals from the two leads. This removes the differential voltage and presents the common mode voltage to the noninverting input of the OP-07. The OP-07 is configured as a unity-gain voltage follower, with the output attached to the cable shield. Since the shield is driven at nearly the same level as the common mode voltage of the input, capacitive coupling between the shield and the active leads is minimized. This serves to greatly reduce induced voltages between the shield and the input leads, which, if the source resistances are not precisely equal, appear as a confounding differential voltage on the input leads.

The PMI OP-37 (Figure 2) is added to the AMP-01 circuit, configured as a unity-gain inverter. With the output tied to the reference pin of the AMP-01, it becomes an active part of the feedback system of the AMP-01. By floating the output of the AMP-01, a differential input to the next stage can be used. This serves to remove any common mode signal that may be present on the leads connecting the two stages. It is also an appropriate configuration in case it is desirable to separate the preamplifier from the second gain stage (e.g., to isolate a subject from the recording apparatus). In such a case, a second

shield driver can be used for the cable separating the two stages. The OP-37 is useful in this application, not only because of its extremely low noise, but because it contributes negligible phase shift over the operating range of the AMP-01. The OP-37 may introduce a small amount of offset voltage, on the order of 35–50 μV , into the circuit, but it is negligible compared with the level of the signal at this stage.

The second-stage amplification (Figure 3) is the Analog Devices AD-521, which is configured for variable gain. The gain is described as

$$\text{Gain} = \frac{R_{\text{scale}}}{R_g}$$

and is controlled by the 100K Ω trimming resistor on the input stage. With $R_{scale} = 100K\Omega$, R_g can vary from 1K to 101K Ω , giving a gain that can be adjusted from 1 to 100. The output offset voltage introduced by the AD-521 is removed by the trimming resistor at pins 4–6. The common mode rejection ratio of the AD-521 is also quite high, around 100 dB with gain of 100.

In addition to the internal feedback circuit of the AD-521, a negative feedback loop is developed through one

Figure 3. Variable-gain second-stage amplifier.

of the two (National Semiconductor) LF-353 amplifiers (an LF-351 can also be used here). This amplifier functions as a frequency-dependent integrator. At direct current (dc) voltage, the net feedback supplied to the AD-521 is -1 , so any dc offset in the signal at the input stage is passed through the AD-521 without being amplified. As the slow component of the input increases in frequency, lower levels of negative feedback are developed. At about 0.8 Hz, the net negative feedback to the AD-521 is $-.001$, a quite small amount. The effect of this circuit is to remove slowly varying offsets, especially below 0.1 Hz, from the signal. This has the effect of removing the random thermal drift developed at the input stage of the AMP-01 (see above) and/or any temperature-dependent voltage offset drift introduced by the AMP-01. At the same time, frequency components of the signal that are of primary interest are retained.

Since the highest frequencies of interest in the EEG lie in the 25- to 30-Hz range, a sampling rate for A/D conversion as low as 250 Hz can be used. The National Semiconductor AF-100 active filter circuits (Figure 4) serve as an anti-aliasing filter. Although there are several ways in which these circuits may be used, the two AF-100s were configured as a fourth-order low-pass Bessel filter with -3 -dB cutoff frequency of 50 Hz. (The AF-151, equivalent to two AF-100s on a single chip, can also be used here.) The phase shift introduced by this filter stage is approximately linear, preserving composite waveform fi-

delity. The filter circuit introduces a gain of 10 into the circuit. The total gain of the entire circuit can thus be varied from 1×10^4 to 1×10^6 .

The signal at this point varies about ground. The LF-351 circuit (Figure 5) shifts the mean dc level of the signal from 0 to +5 V, bringing it into the center of the voltage window (0–10 V) of the A/D converter. It also serves as a high-pass filter with a cutoff at 0.1 Hz, which removes any offset voltage or slowly varying voltage remaining in the signal. Since this circuit and the integrator circuit described (Figure 3) perform similar functions, in a later version of the amplifier we plan to combine them into a single circuit, thus reducing the total parts count.

The signal at this point can be applied to an A/D conversion system. Description of such a system, under computer control, will be the subject of a later article.

Although the common mode rejection ratio of this circuit is quite high, not all of the interference present appears in a precisely balanced way at the inputs. Differences in resistances of the electrode contacts, their location on the subject, and different paths of the electrode wires through space result in different amounts of interference, especially 60 Hz, being coupled into the two leads. In addition, the input circuit to the amplifier is never perfectly balanced. Because of slight differences in component values, there are small but significant differences in the reactance to ground that each lead sees. The common portion of the induced interference can be largely rejected

RESISTORS 1% METAL FILM $\frac{1}{4}$ W

FIRST SECTION	SECOND SECTION	COMPLETE FILTER
$f_0 = 70.9$ Hz	$f_0 = 79.5$ Hz	$f_0 = 50$ Hz
$Q = 0.522$	$Q = 0.806$	
GAIN = 2.52	GAIN = 3.92	GAIN = 9.88

Figure 4. Low-pass filter.

RESISTORS 5% CARBON COMP, ¼ W
 CAPACITORS POLYSTYRENE METAL FILM 10%
 CUT-ON FREQUENCY 0.1 Hz
 OUTPUT DC LEVEL = +5 V

Figure 5. Level-shift/high-pass circuit.

with proper amplifier and circuit design, but the difference between them cannot be and thus appears confounded with the signal.

There are several things that can be done to reduce this confounding interference. Naturally, thorough shielding of the amplifier in a grounded case is essential. Bootstrapping the common mode signal to the shield, as was done here, is helpful. Bootstrapping the input resistors in the ac input coupling network is another. This greatly multiplies the apparent resistance of the ac coupling resistors, making slight differences in component values small relative to the total. A 60-Hz notch filter could be introduced at the output of the AD-521. A better alternative is to change the AF-100 filter circuit to a lowpass elliptical filter with a transmission zero at 60 Hz just outside the passband of the filter. Either type of filter has the drawback of introducing some phase shift into the signal of interest. Such phase shift would have to be corrected for

if any type of multichannel mapping, interpolation, or vectoring were to be attempted. A third approach would be to implement software filtering, which has the advantage of not introducing phase shift into the signal, but leaves the circuit vulnerable to saturation by large-amplitude interference signals. Since there are trade-offs to be considered in any of these filtering schemes, the choice is open at this point.

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(Manuscript received October 28, 1986;
 revision accepted for publication September 13, 1987.)