A bit-addressable I/O interface for microcomputers

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An input/output (I/O) interface design based on the 6522 VIA is described. This design is enhanced with additional circuitry to provide such features as latched input, bit-addressable I/O line control, and provisions for expansion.

Many designs are available for building input/output (I/O) interfaces necessary for communication between microcomputers and peripheral devices (Jenkins, 1982; Osaka, 1980; Osaka, 1981; Rosellini, Carlson, Dian, Falcone, & Shapiro, 1983). Most use some form of the one-chip programmable interface large-scale integrated circuits (LSI) currently available (either Intel's 8255 or MOS Technology's 6520, 6521, or 6522). Typical designs describe how to interface and program a LSI chip and how to connect switch input buffers and power drivers to interact with peripherals (e.g., switches, lights, relays, etc.). Most fail, however, to consider how to make the most effective use of a large number of I/O lines. For instance, it is a very simple matter to turn on or off a single bit at a time or a number of bits in a synchronized fashion in the typical 8-bit I/O port, but a much more difficult one if the bits are to be turned on or off in an asynchronous fashion. Manipulating a single bit can be accomplished by loading the output (or status) port and using an appropriate mask consisting of either the OR or AND instruction to turn a specific bit either on or off. This takes three instructions [LDA, AND (OR), and STA] and 8 bytes of memory. Although this is quite acceptable, it does require additional lines of programming. Indeed, if the number of I/O lines available in the microcomputer is sufficient to meet the needs of the proposed task, this software solution may be preferable. However, if more I/O lines are required or, as is normally the case, if additional integrated chips (ICs) are needed to buffer the I/O lines, then the bit-addressable I/O interface described here may be more suitable.

This interface design, although based on the 6522 VIA, has several features not found in most other I/O interfaces. Foremost is that of latched inputs plus the ability to turn off or on a single specified bit with only two instructions (LDA and STA). It can also be expanded to accommodate up to 48 (or more) I/O lines.

The interface is composed of two modules, one for input and one for output. Both, however, are controlled

by the same 8-bit port (up to eight modules may be controlled by the port). The input module consists of eight Switch Input Conditioners (SIC) (see Figure 1). The resistance-capacitance (R-C) circuit of the SIC (see Figure 2) allows only the transitional voltage change (i.e., going from 5 V to ground as a result of a switch closure) to set the Flip-Flop (FF). The signal is then fed into a bit of Port A, where it can be detected. After the central processing unit (CPU) reads the port, the FF is reset by a signal from the 74138. Thus, the input is "latched" until the port is read. Furthermore, the switch must be

Figure 1. Functional block diagram of switch input circuitry.

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opened before another pulse can be generated by the R-C circuit. With the values used in Figure 2 for the R-C network, the time constant of the charging of the capacitor is approximately 5 microsec. Since this is a much shorter period of time than it takes a mechanical switch to stop "bouncing," it is necessary to jump to a software timing loop after initially reading the port. Alternatively, the values of the R-C network could be increased to provide a longer time constant. Regardless of how this is handled, the major function of this portion of the circuitry is to provide a "one-shot" mode of operation—only one output pulse per switch closure.

In the output module, a certain value (see Table 1) is sent to the 74154 decoder. Depending on the value, one of 16 lines is enabled, either setting or resetting one of the eight FFs (see Figure 3). The output of the FF is used to control the high-current power drivers (2N3055s). When used with the appropriate heat sink, the 2N3055 transistor can drive devices drawing up to 10 A such as solenoids in feeders, liquid dippers, etc. The 2N2222 transistor itself can supply up to 150 mA current for driving cue lights, relays, etc. If desired, a multiline relay driver device, such as Texas Instruments SN75468 or Spragues ULN2003A, can be used by the FFs for controlling a wide variety of different-voltage dc relays (up to 500 mA).

Whenever there is a write to the 74154 by Port B, CB2 (if enabled) outputs a pulse (low) to G2 during the write, enabling the 74154. (PB4 is normally low; any value between \$10 and \$1F will bring G2 high and deselect the chip.) After the write, CB2 goes high again, restoring the 74154 to its original state (setting all output lines high) and, in effect, disconnects it from all

Figure 2. Circuit diagram of a switch input conditioner (SIC).

Table 1
Values Necessary to Turn an Output Device On or Off
or to Read and Clear a Switch Input

Device	Output		Input		
	Port B		Port A		
	On	Off	Bit	And	Clear
0	\$00	\$08	0	\$01	\$10
1	01	09	1	02	11
2	02	0A	2	04	12
3	03	0B	3	08	13
4	04	0C	4	10	14
5	05	0D	5	20	15
6	06	0E	6	40	16
7	07	0F	7	80	17

Figure 3. Circuit diagram of output driver board.

the FFs. In Figure 3, PB4 is used as a chip select line. By using PB4, PB5, and PB6 to control another 74138, as many as eight additional ICs could be selected, greatly increasing the number of I/O lines controlled. Table 1 contains the values necessary to load into Port B either to turn on or off the power drivers or to reset the switch inputs. To detect an individual switch closure, Port A is loaded and subjected to an AND instruction with the appropriate mask.

The interface circuits described here are constructed out of readily available, low-cost, dual-inline-type ICs. The total parts cost for the interface as shown should be less than \$10.00.

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