A simple IC pulse-pair stimulator

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The present paper describes a simple and relatively inexpensive brain stimulator circuit for generating trains of conditioning (C) and test (T) pulse pairs for refractory period and excitability cycle analyses. C and T outputs are constant-current monophasic cathodal pulses of adjustable frequency, duration, amplitude, and delay. C and T pulses can be controlled manually or through logic programming and can be fed out the same or separate channels. The stimulator can be operated on either ac or dc supplies and, when battery operated, features a high degree of stimulus isolation.

The application of refractory period and excitability cycle analyses to the behavioral effects of electrical brain stimulation has added a powerful new dimension to brain stimulation techniques (e.g., Coons, Schupf, & Ungerleider, 1976; Deutsch, 1964; Gallistel, Rolls, & Greene, 1969; Yeomans, 1975). Such analyses involve the use of trains of stimulation pulse pairs [an initial conditioning (C) pulse and a subsequent test (T) pulse], with varying interpulse delays. From the application of such analyses, it may be possible to neurophysiologically identify the specific activated neurons relevant to a given behavior, to determine the direction of conduction within neurobehavioral systems, and to examine the degree and nature of postsynaptic summation or interaction between neural systems (e.g., Coons et al., 1976).

Unfortunately, commercial stimulators capable of generating pulse-pair trains are quite expensive (e.g., Grass Instruments S88, approximately \$1,200). Deutsch (1966) describes a simple pulse-pair stimulator constructed of digital logic. The Deutsch unit, however, does not provide a constant-current output, and the outputs must be capacitively coupled to prevent dc leakage. In this report, a simple and inexpensive circuit is described that provides trains of constant-current C and T pulse pairs out of the same or different channels. The outputs of the stimulator are monophasic cathodal pulses of adjustable frequency, delay, and pulse width, and can be controlled manually or through logic programming.

CIRCUIT DESCRIPTION

The stimulator (Figure 1) consists of three logic stages: (1) a frequency and delay generator, (2) a pulse former stage, and (3) an output stage. The frequency and delay generator consists of two 555 IC timers in a single 14-pin package (NE 556 or RC 556). One 555 timer (pins 1-6) functions as an astable multivibrator,

generating square wave pulses at a variable frequency (5-1,000 Hz) as a function of the setting of a potentiometer (R2) and switchable range capacitors (C3 and C4). This astable triggers the C pulse output and determines the basic frequency of the stimulation. The astable output also triggers the second 555 timer (pins 8-13) which functions in a monostable mode. Monostable output time is adjustable (potentiometer R1 and switchable range capacitors C1 and C2) and serves to trigger the T pulses after varying delays following the C pulses. The pulse former stage consists of two monostable multivibrators constructed from CMOS NOR gates (CD4001AE, four per IC package); one receives a trigger pulse from the 555 astable and the other is triggered from the 555 monostable. The first CMOS monostable (OG3 and OG4) is triggered from the rising edge of the astable square wave output, and provides an output pulse at the astable frequency. The duration of the output pulse is adjustable (potentiometer R4 and switchable range capacitors C7 and C8) and serves to form the C pulse output. The second CMOS monostable (OG1 and OG2) is triggered on the falling edge of the 555 monostable. The output time of the second CMOS monostable is also adjustable (potentiometer R3 and switchable range capacitors C5 and C6) and serves to form the output T pulses. Both the C and T pulse outputs occur at the basic astable frequency. The delay between the C and T pulses depends on the setting of the 555 delay monostable, which is adjustable from 10 microsec to 10 msec. For longer delays, C2 can be increased or an additional range capacitor added; .1 microfarad provides a maximum of a 100-msec delay. The output stage consists of two CMOS NAND gates ($\frac{1}{2}$ CD4011AE or CD4093BE), used as gated inverters, and two output transistors (GE 2N6004). The CMOS gates invert and square up the positive-going output pulses from the pulse former stage and provide a means of logic gating the output. The C pulses from the pulse former are fed via diode D1 into gate AG3, and T pulses are fed into gate AG4 and, via diode D2 and switch S1, into AG3. The remaining inputs of the two gates are tied together

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Figure 1. Circuit diagram of pulse-pair stimulator.

at G and held at logic high by the 56K pull-up resistor (R5). With switch S1 open, the outputs of gates AG3 and AG4 generate cathodal C and T pulses out separate channels according to the frequency, delay, and pulse widths determined by the first two stages. With switch S1 closed, however, gate AG3 generates similar cathodal C and T pulses with a single-channel output. Outputs can be logic gated by applying a logic low to the G input connection, which serves to hold the outputs of the output gates high. This turns off the stimulation, irrespective of the pulse former inputs.

Stimulation output trains from gates AG3 and AG4 are fed into the output transistors (Q1 and Q2) to allow control over output current levels. Gate outputs are fed, via diodes (D3 and D4) and current-limiting resistors (R6 and R7), into the emitters of the output transistors, Q2 receives the T pulse output from gate AG4; Q1 can receive (via switch S1) either the C pulse output alone or the combined C and T pulses from gate AG3. The current-limiting resistors (R6 and R7) serve to limit both base-emitter and collector-emitter current, and improve temperature stability. The bases of the output transistors are controlled by the voltage divider networks (R8R9R10 and R11R12R13) which determine the

output current level. The outputs of the transistors are then connected (via 1K precision resistors to allow current measurement) to the animal's brain electrodes,

Table 1
Parts List for Pulse-Pair Stimulator

Quantity	Item
1	IC timer (NE 556 or RE 556)
1	CMOS IC quad NAND gate (CD4011AE or CD-4093BE)
1	CMOS IC quad NOR gate (CD4001AE)
1	CMOS IC analog switch (CD4016AE)
1	IC voltage regulator (uA7815 or LM340-15)
2	NPN transistors (GE 2N6004)
4	Switching diodes (1N914)
1	Diode bridge (1A, 50 V)
1	Transformer (24 V at 100 mA)
6	Potentiometers: three 1M, one 150K, two 25K
16	Resistors ($\frac{1}{2}$ W): four 1K (1%), two 5K, two 4.7K, one 10K, two 47K, three 56K, two 68K
14	Capacitors: one 2,200 microfarad, one 10 microfarad, one 1.0 microfarad, two .1 microfarad, three .01 microfarad, two .0025 microfarad, one .001 microfarad, two 250 picofarad, one 100 picofarad
4	Switches: one DPDT, one DPST, two SPST

with V+ serving as the reference (indifferent or anodal pole). By varying the setting of the output potentiometers (R9 and R12), the output transistors provide trains of constant-current C and T pulses ranging from 1 microA to 1.0 mA. The diodes (D3 and D4) between the output gates and the transistors prevent base-emitter reverse biasing and leakage while the gate outputs are high. Since these diodes also drop the first .6 V in the output circuit, they serve to eliminate potential collector-emitter voltage differences during the baseline period, when the gate outputs are high (which can otherwise result from the fact that CMOS logic high outputs never completely reach V+). Since there is no collector-emitter voltage difference while the gate output is high, dc leakage is less than 10 nanoA, which is far superior to most commercial stimulators that we have tested. Output onset and offset are controlled by the output switch (S2) or, if this switch is left on, by logic gating at the gate (G) terminal. Switch S3 allows a selection of current or voltage monitoring by a dual-beam differential input oscilloscope, which measures the voltage drop across the animal or the voltage drop across the precision 1K series resistors; 1 V equals a 1-mA output.

A very simple optional circuit can be added to the stimulator to greatly minimize potential electrode polarization resulting from the high output impedance characteristics of constant-current stimulators. The circuit consists of a single IC analog switch (CD 4016) that serves to short out the animal's electrodes during the baseline period between current pulses. This provides a low-impedance current shunt during the baseline to discharge the polarization potential of the electrodes. This circuit also allows stimulation voltage readings unconfounded by polarization potentials. For this function, two of the four analog switches on the 4016 are used, one for the first channel and the other for the second channel output. The IC package is powered from the stimulator supply, with V_o connected to pin 14 and V- to pin 7. The inputs of these switches (pins 1 and 11) are connected to the indifferent connection (logic high or V_o), and the outputs (pins 2 and 10) are connected to the collectors of Q1 and Q2, respectively. The control inputs of these switches (pins 13 and 12) are connected to the gate sides of R6 and R7. Control pins 5 and 6 of the two unused switches on the 4016 package should be tied to V-. When the gate outputs are high (baseline period between current pulses), the switches are conducting and the electrodes are shorted. When the gate outputs swing low (generating current pulses), the switch is turned off, allowing current to pass to the electrodes. Since the current leakage through the switch in the off condition is only about 10 picoA, an insignificant portion of the output is shunted away from the electrodes during the current pulse.

APPLICATIONS

The unit provides constant-current cathodal pulse-

pair trains, with C and T pulses out the same or separate channels. Constant-current regulation is limited only by the power supply voltage; the maximum load for current regulation at 10 microA of output = 1M, at .1 mA = 100K, and at 1 mA = 10K. Due to the characteristic voltage-dependent breakdown in electrode impedance at higher current levels, these maximum load characteristics allow constant-current operation over the entire range of stimulation levels, even with very small electrode tips. Figure 2 shows representative oscilloscope traces of the stimulator outputs. The pulse-pair frequency of the illustrated stimulator is 5-100 Hz (low range) and 50-1,000 Hz (high range), with C-T delays of 10-1,000 microsec (low range) and .1-10 msec (high range). Longer C-T delays can also be obtained by simply adding another capacitor (see Circuit Description section). Output pulse amplitudes (1 microA to 1 mA) and pulse widths (10 microsec to 1 msec) are separately controllable in the dual-channel output mode; in the single-channel mode, amplitudes of both pulses are controlled from a single potentiometer. Maximum output current can be altered, if higher or lower output currents are desired, by simply decreasing or increasing

Figure 2. Oscilloscope traces of stimulation output. Top: Separate channel conditioning and test pulses (vertical deflection = 5 V/cm; sweep, 1 msec/cm) Bottom: Single-channel conditioning and test pulse output (vertical deflection = 2 V/cm; sweep, 1 msec/cm).

the values of the current-limiting resistors (R6 and R7). Maximum output current is limited by the supply voltage and the load.

The output of the stimulator can be controlled either manually or by logic gating. In the gate control mode, the manual switch is left on, and the stimulator provides an output unless a logic low is applied to the gate input. Since the stimulator delivers cathodal pulses, V_o (logic high) serves as ground and should be connected to the logic high of the programming apparatus for the gating operation. Since the trigger level of the CMOS ICs used in the stimulator is approximately one-half the supply voltage (or about 7.5 V), the gating function is compatible with any programming apparatus having a 9- to 15-V difference between logic low and logic high. With a simple modification, the stimulator outputs can be completely controlled by logic signals. For this logic control mode, the CMOS monostable outputs to the NAND gates in the output stage (AG3 and AG4) are switched out, and outputs of the programming apparatus are switched into the respective NAND gate inputs. When this is done, the stimulator provides adjustable amplitude constant-current cathodal outputs whenever the respective programming input is at logic high, and pulse frequencies, widths, and delays can be independently programmed on an external apparatus. As in the gating mode, the interfacing requirement in the logic control mode is that the voltage difference between logic low and logic high of the programming equipment be between 9 and 15 V.

The power supply of the stimulator is isolated from the line voltage by the power transformer; consequently, the stimulator outputs are floating.

For highly critical applications, such as combined stimulation and recording studies, more effective isolation can be obtained by using a battery supply. This

provides complete stimulus isolation and is highly practical because of the low current draw of the unit (less than 20 mA). The stimulator can be operated from any 18- to 24-V battery connected to the inputs of the voltage regulator, in place of the inputs from the transformer and diode bridge. Since the regulator maintains the supply voltage at 15 V, declining battery voltage does not affect the output, providing battery voltage does not drop below 17 V. Because of this feature, inexpensive carbon-zinc batteries or rechargeable nickel-cadmium batteries can be used. For prolonged operation, mercury batteries are desirable. The unit will run on two 9.8-V mercury batteries (Burgess 302478; 2,400-mAh capacity) for over 120 h of continuous operation.

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