INSTRUMENTATION & TECHNIQUES

The movement-activated recording monitor: A third-generation motor-activity monitoring system

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The movement-activated recording monitor (MARM) is a small noninvasive device that continuously detects, accumulates, and stores the amount of motor activity produced during sequential time intervals of designed duration. If motor activity totals are recorded every 15 min, the MARM is capable of calculating and storing 96 data points/day for 5.33 days. The MARM employs large-scale-integrated complementary-metal-oxide integrated circuits. To date, application has been primarily limited to psychiatric investigations, but the MARM is readily applicable for other time-motion studies of human or animal subjects.

For a number of years, our laboratory has been involved in the development and application of human motor-activity monitoring systems. We have previously reported on both telemetric and large-scale-integrated (LSI) motor-activity monitoring systems (McPartland, Kupfer, Foster, & Weiss, 1976; McPartland, Foster, & Kupfer, 1976), and their clinical applications in psychiatry (Foster & Kupfer, 1975; Kupfer, Weiss, Foster, Detre, Delgado, & McPartland, 1974).

While both the telemetric and LSI monitors have their unique advantages, the recent addition of LSI-CMOS integrated circuits to the realm of microelectronics has made it possible to design a motor-activity monitor having the principal advantages of both. Basically, the addition to the LSI monitor of a time-base generator and multicell Random-Access Memory (RAM) allows the storage of motor-movement sums accumulated over many sequential short time intervals. The addition of a multicell memory and associated time base enables the device to internally record many data points per day. This third-generation motor-activity monitor has received the acronym of MARM, for "Movement-Activated Recording Monitor." The unit is small and can be worn in the same manner as a wristwatch. MARM is not space restrictive and it is nontelemetric.

DESCRIPTION OF THE MARM

Aside from the motion transducer and quartz crystal, the electronic circuitry is comprised of CMOS ICs, operating at very low power levels, which allow small mercury batteries to last for well over 1 month. All integrated circuits in this unit, with the exception of the RAM, are ceramic flat packages

measuring approximately $2.5 \times 7.6 \times 10.1$ mm. The RAM is comprised of two ICs measuring $9.8 \times 28.0 \times 1.5$ mm each. These small ICs and printed circuit techniques allow the entire monitor, weighing approximately 35 g, including batteries (4.2 V dc), to be housed in a Lucite case measuring $4.0 \times 2.0 \times 2.0$ cm.

The block diagram of the MARM is shown in Figure 1. The motion transducer, also used in the LSI monitor, is a miniature mercury switch having known characteristics of movement sensitivity. The detection is linear, with respect to the number of movements present, and gives equal weight to all movements above the small displacement threshold of 5 mm. Its measure, therefore, is a function of the number of movements, and not their magnitude. The scaler, a 12-stage binary counter, is then used to scale down the number of movements detected by the mercury switch. This scaler can be wired to divide the number of movements detected by N , where $N = 2^n$ (n = selected integer between 1 and 12, inclusive, depending upon the count range needed). For each N movements detected, one pulse is originated by the scaler circuit. This pulse increments the accumulator, which sums the number of activity units occurring during the time interval, where one activity unit corresponds to N detected movements. The accumulator has a capacity of four binary bits, allowing it to sum from 0 to 16. A sum of 16 corresponds to $16 \times N$ movements detected.

A quartz crystal oscillator and frequency-divider circuit provide timing pulses to effect the storage of accumulated activity units during successive time intervals. Each successive time interval is terminated by a timing pulse from the frequency divider. The duration of this time interval (T) depends

Figure 1. Functional block diagram of the MARM.

on the crystal frequency and the number of flip-flop stages used in the frequency-divider circuit. Each flip-flop stage divides the frequency by 2. Using an 18.651-kHz crystal, summing intervals of 1.875, 3.75, 7.5, 15, or 30 min can be chosen, depending on whether 21, 22, 23, 24, or 25 flip-flop stages are employed.

At the termination of each summing interval, marked by a timing pulse from the frequency divider, the contents of the accumulator (the number of activity units summed during the preceding time interval) are deposited into memory, and the accumulator is reset to 0. An addressing counter specifies which memory cell receives data. This counter is initially set to 0 and is incremented by 1 after each transfer of data from the accumulator to memory. In this manner, each memory cell from 0 to 511 is sequentially filled at the rate of one cell/T min. The contents of each cell then represent the activity unit total for its respective time interval.

As the RAM becomes full, data must be transferred from the MARM to an external permanent storage medium so that the monitor may be reused and the data analyzed. This is accomplished via a nine-pin connector. These external connections are READ, DATA OUT (four lines), +4.2 V, GROUND, MEMORY ADVANCE, and RESET. In order to effect transfer of data, the following must be performed: (1) +4.2 V, GROUND: Connect +4.2 V and GROUND from the permanent storage instrument to the +4.2 V and GROUND connections of the MARM. (2) RESET: Present a RESET pulse of width 1 msec, or greater, to the RESET connection of the MARM. This resets the addressing counter, enabling the word in Location 0 of the RAM to be presented to the DATA OUT lines. (3) READ: Connect +4.2 V to the READ connection of the MARM. This enables the READ function of the RAMs. (4) MEMORY ADVANCE and DATA OUT: Repetitively pulse the MEMORY-ADVANCE connection of the MARM. Read each

successive word (four parallel bits on the DATA OUT lines) of data during each successive MEMORY ADVANCE pulse applied. In this way, the DATA OUT lines sequentially represent the data words in Cells 0 through 511 of the RAMs. This completes the data transfer, and the monitor is ready for reuse. Presently, this laboratory is using a PDP-11 minicomputer to dump and permanently store the data on disk or Dectape. In place of a computer, an inexpensive Teletype with an appropriate interface for controlling data flow could be used to produce hard copy of the data. Alternatively, a four-channel strip chart recorder, connected to the DATA OUT terminals of the monitor, and a square-wave generator, pulsing the MEMORY ADVANCE terminal, would present binary-encoded data displayed on the recording paper.

CIRCUIT DESCRIPTION

Figure 2 is a detailed circuit schematic of the MARM. The motion transducer, scaler, and accumulator are straightforward. The output of the accumulator is in parallel binary form and is routed to two 5101 RAM integrated circuits. The proper memory IC is chosen by the ninth addressing bit (Q9) of the addressing counter. Memory Cells 0 to 255 are in RAM 1, which is enabled ($\overline{\text{ENABLE}} 1$ low) by Q9 of the addressing counter (Q9 low) during the first 256 time intervals. At this time, RAM 2 is disabled. During the next 256 time intervals, RAM 1 is disabled, and RAM 2 is enabled ($\overline{\text{ENABLE}} 1$ low) by Q9 (Q9 high). The transistor preceding $\overline{\text{ENABLE}} 1$ of RAM 2 functions as a simple inverter, making $\overline{\text{ENABLE}} 1$ of RAM 2 always the complement of $\overline{\text{ENABLE}} 1$ of RAM 1.

The oscillator and the first 21 flip-flop stages of the frequency divider are in a CD4045 IC. Its output feeds the final four flip-flop stages of the frequency divider contained in one-half of a

Figure 2. MARM schematic.

CD4520 IC. A jumper wire is placed between Point A (see schematic) and the output of Flip-Flop Stages 21, 22, 23, and 24 to select the desired time interval. The capacitor-diode-resistor network following Point A narrows the width of the timing pulse to limit the amount of time the RAMs are enabled to accept data (ENABLE 2 high). Except when actively accepting data from the accumulator, the RAMs are in a standby state (ENABLE 2 low) so that a minimum amount of current is drawn by these ICs (less than 15 microA) as compared to the operating current drawn during data transfer (approximately 10 mA).

At the termination of the timing pulse at Point A, the addressing counter IC (CD4040) is incremented by the downward slope of this timing pulse, which is presented at the clock terminal (CL) of the addressing counter. This occurs only after transfer of data to the RAMs has been completed. Figure 3 is a timing diagram showing the temporal relationship of the timing pulse as it appears at Point A, at the ENABLE 2 lines of the RAMs and the addressing counter's CL line.

When dumping stored data, the input lines to the RAMs (D1, D2, D3, and D4) are disabled, and the output lines (DO1, DO2, DO3, and DO4) enabled (READ/WRITE high), by connecting the READ terminal to +4.2 V. The timing pulses at Point A

are overridden by pulsing the MEMORY ADVANCE line by an external source. During the first 3 msec of each pulse, the corresponding data will be present at the output terminals.

CONCLUSIONS

The MARM can record frequent motor-activity totals over relatively short sequential time intervals without confining the subject to a limited spatial range. The MARM is capable of recording motor-

Figure 3. Timing pulse diagram: (a) Point A, (b) ENABLE 2 line of RAM, (c) CL line of addressing counter.

activity data over sequential time intervals of pre-selected durations ranging from 1.875 to 30 min. Since there are 512 memory cells, motor activity can be continuously monitored for at least 16 h (when storing activity totals every 1.875 min), to as long as 10.7 days (when totaling activity every 30 min).

The development of the MARM makes it possible to record detailed motor-activity profiles (e.g., 96 activity totals/day for 15-min intervals/data point) on psychiatric-ward patients or outpatients, permitting an accurate assessment of ultradian and circadian motor-activity rhythms. To date, the MARM has not been employed in other areas; however, possible applications in such fields as cardiology, neurology, physiology, and psychology, would appear to be numerous.

The cost of the MARM is modest, at approximately \$150/unit. A large investment in computing equipment is not necessary to output stored data from this device. We are currently designing an interface to output data on an inexpensive

conventional Teletype. The estimated cost of this system is approximately \$1,200. Any interfacing system would be capable of servicing many MARM units, further reducing the per-unit price of the entire system.

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