INSTRUMENTATION & TECHNIQUES

Digital readouts superimposed electronically on televised pictures

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A display module is described that allows numeric data to be superimposed on televised pictures and recorded as an adjunct to the televised information. The device is inexpensive, versatile, and electrically compatible with most closed circuit television systems. It employs standard, large-scale integrated (LSI) circuits, commonly used in commercial television receivers to display time and channel number. Additional circuits are presented that connect these LSI circuits to those of a conventional television camera and videotape recorder, allow variables other than time and channel number to be displayed, reduce the size of the readouts, and produce more than one set of time and channel number readouts.

Closed circuit television, as a research tool, has come into increasing use since the advent of inexpensive videotape recorders. Besides being used to record time-varying events and behaviors (Masters, 1979; Rutowski, 1977), video systems have been developed to view images illuminated with infrared or ultraviolet light, radiation normally invisible to humans (Conner & Masters, 1978; Eisner, Silberglied, Aneshansley, Carrel, Howland, 1969). As versatile as these video systems are, there are improvements that make them more useful. One refinement is the superposition of digital readouts on the televised pictures. Such readouts enhance the televised information by providing a permanent record of any variable that can be digitized. General experimental data (experiment number, elapsed time, video frame counts), environmental conditions (temperature, wind speed, barometric pressure), and subjects' responses are but a few of the possible data that can be recorded. Described here is a display module and its connection to a conventional video system. For our special purposes, the display module has been used to indicate experiment number and time (Figure 1). The time readout, given in minutes, seconds, and 60ths of 1 sec, changes with each video frame and can thus serve as frame and time marker in playback analysis.

CIRCUIT DESCRIPTION

LSI Readout Circuit

The primary function of the display module is to

This study was supported in part by the National Institutes of Health (Grant AI-02908-21), the National Science Foundation (Grant PCM-77-25807), and Hatch Project NY(C) 191405. I thank Thomas Eisner, Nelson Bryant, and Randall Grant for their helpful comments during the preparation of this manuscript and Bruce Herzog, who assisted in the construction of the first display module.

generate a video-like output of the readouts that is combinable with the video signal produced by a television camera. The composite signal, when transformed by a television monitor, shows the readouts superimposed on the televised scene. A LSI readout circuit (Figure 2A), with appropriate inputs, fabricates a video-like output of time and channel number (National Semiconductor

Figure 1. Photograph of television monitor showing the digital readouts superimposed on a televised image. The image is that of an ant bioassay in which two chemically treated (lower right and upper left) and two untreated (lower left and upper right) food samples were presented to ants. The relative number of ants at treated and untreated sites gives an indication of the potency of the chemical concentration used in the treated samples. The upper readout indicates the experiment number, and the lower readout indicates the elapsed time of the experiment in minutes, seconds, and 60ths of 1 sec. In analyzing a bioassay, counts at each feeding site are made every 5 sec over a period of 1 min. With the readouts, it is very easy, during playback of the videotaped experiments, to stop the tape every 5 sec and make counts at each site.

Figure 2. Block diagram of display module. (A) Readout circuit (National Semiconductor Corporation's MM5841) and associated timing circuits. Three NAND gates (a1-a3) form an oscillator that sets the length of the dots in the display. Potentiometers set time delays relative to the horizontal and vertical synchronization pulses and control the placement of the display in the televised image. (B) Interconnections between the videotape recorder (VTR) system and readout circuit. Inputs from the VTR or camera are buffered. The frequency doubler causes two half-sized displays to be produced, either of which can be blanked, thus reducing the size of the original display. Video mixer combines the video outputs of the camera and readout circuit. (See text for details.) (C) Input devices for the readout circuit. Digital clock circuit (National Semiconductor Corporation's MM5318) provides multiplexed input for the six-digit readout. The vertical synchronization pulse to the readout circuit provides the 60-Hz timing signal needed by the clock circuit. Two thumb-wheel switches are a convenient means of supplying the binary-coded decimal inputs needed for the two-digit readout. All resistors are in ohms. Capacitors are in picofarads unless otherwise indicated. NAND gates (a1-a3) are 75% of an MM4011BCN chip; diodes are 1N4148.

Corporation, 1977b). The output is a sequence of on-off signals that describe the readouts as a pattern of dots on a blank background (dots are actually segments of a video line). The composite output is formed by mixing video signals of the camera and of the readout circuit (Figure 2B) such that the blank background of the display's picture is replaced by the televised image. Registration of the televised and display pictures is made possible by using the same synchronization pulses for the readout circuit and video camera (television transforms space into time; vertical and horizontal synchronization pulses are temporal markings of the top and side of the picture, respectively). With common synchronization pulses, the formation of both pictures begins at the same time and place. Synchronization pulses for the readout circuit can be extracted from the camera's video signal or taken from the videotape recorder, if provided.

The readout circuit also requires inputs that adjust the display's position in the picture and set the size of

the dots. The period of an external oscillator (NAND gates a1-a3, Figure 2A) determines on-time of a dot and, therefore, its length. Two resistor-capacitor circuits set delays relative to the horizontal and vertical synchronization pulses. These delays determine the vertical and horizontal offset of the display relative to the top and side of the picture and are adjustable through potentiometers. The relative position of the time and channel number readouts is preset in the readout circuit.

LSI Digital Clock Circuit

A second function of the display module is to provide data to the readout circuit in the proper formats. Information shown in the time and channel number readouts is entered in multiplexed and direct formats, respectively. Thumb-wheel switches provide a convenient means for entering the channel number input (Figure 2C), although other electronic circuits can be used, particularly if time-varying functions are to be dis-

played. Data for the time readout are entered one digit at a time; the readout circuit produces an output that indicates which one of the six digits is about to be shown, and the input device supplies the appropriate information. Ordinarily, such entries require a substantial amount of circuitry; however a LSI digital clock circuit (Figure 2C) is commercially available that provides an output compatible with the readout circuit's multiplexed input (National Semiconductor Corporation, 1977a). The clock circuit requires a 60-Hz timing signal (vertical synchronization pulses can provide this input) and four inputs controlled by switches. The switches select a clock cycle of 12 or 24 h and one of three modes of timing, fast set, slow set, and normal, in which the "hours" indication changes on the second, minute, and hour, respectively.

Reduction of the Display's Size

The readout circuit, as developed by the manufacturer, produces a display that takes up an unnecessarily large portion of the video image. The display's width is compressed by decreasing the length of the dots. Dots are shortened by reducing the period of the readout circuit's external oscillator (i.e., dot clock; see National Semiconductor Corporation, 1977b). The height of the display is decreased by halving the number of lines used

in a normal display. The pulse rate at the readout circuit's horizontal synchronization input is increased to twice that of the video camera's horizontal synchronization rate. This causes two display lines to be generated for each line of the televised image. A resultant picture would show two displays, both on the same video lines and each with half the number of lines of a normal display. Either of these half-sized displays can be erased by blocking the readout circuit's output during transmission of the display or by selection of appropriate time delays.

Multiple Displays

Without the disabling circuit and with delays that do not eliminate either display, two sets of readouts can be displayed and used. The same technique can be used with vertical synchronization pulses to produce two sets of readouts in the vertical direction.¹ However, providing and multiplexing information for multiple sets of readouts requires a significant addition of circuitry and detracts from the simplicity of the intended design.

Interconnection to Video System

We have adapted the display module to a portable video system (Sony Corporation of America's AV3400 videotape recorder and AVC3400 video camera) as shown in Figure 3.

Figure 3. Connection of video system (Sony Corporation of America's AV3400 and AVC3400) to display module. Horizontal and vertical synchronization pulses from videotape recorder (VTR) are used to generate synchronization pulses to the readout circuit. Voltage comparators (c1 and c2) act as buffers between the VTR and readout circuit, with potentiometers (R1 and R4) used to set the onset and duration of buffered synchronization pulses. Time-delay circuits (b4, c3, R2 and b3, c4, R3) set the interval between buffered and added horizontal synchronization pulses and the duration of the added pulses. Additional pulses are needed to double the horizontal synchronization pulse rate to the readout circuit. This produces two half-sized displays, the first of which is not permitted to reach the output circuitry (NAND gate a4). The video output of the readout circuit during the second display controls transmission gates (TG1 and TG2) that regulate the formation of the composite video output. The brightness of the dots is controlled by a potentiometer (R5). All resistors are in ohms. Capacitors are in picofarads unless otherwise indicated. NAND gate a4 is 25% of an MM4011BCN chip; NOR gates (b1-b4) are a single MM4001BCN chip; comparators (c1-c4) are a single LM339N chip; transmission gates (TG1 and TG2) are half of an MM4066BCN chip; Transistor Q1 is a 2N3904; the diode is a 1N4148.

The formation of the composite video signal is regulated by the readout circuit's output. It controls electronic switches, called transmission gates (TGs), that connect either the televised or display picture to the composite video output. If the readout circuit's output is off, then the video signal from the camera is connected to the composite video output (TG1 is turned on). If the readout circuit's output is on, then the video signal from the camera is disconnected (TG1 is turned off) and the bias level of the output transistor (Q1), and therefore of the composite video output, is increased for the period of the dot clock (TG2 is turned on). Brief changes in bias level form video signals that are manifested as dots on the television screen. The change in the bias level, as controlled by potentiometer (R5), fixes the brightness of the dots.

Registration of the display and televised pictures is achieved by interconnecting the vertical and horizontal synchronization inputs of the camera and display module. Synchronization pulses applied to these common inputs are taken from the videotape recorder, in which they are normally available for the video camera. The pulses are buffered by the display module to prevent the videotape recorder's outputs from being altered and to satisfy the input requirements of the readout circuit. Synchronization signals from the recorder are compared with voltage levels set by potentiometers (R1 and R4), and these comparisons determine the onset and duration of the buffered synchronization pulses.

To double the horizontal synchronization pulse rate, additional pulses are introduced between and combined logically with the buffered horizontal synchronization pulses. Two monostable multivibrators (one-shots) set the interval between the buffered and added pulses and the duration of the extra pulses. These time delays are controlled by potentiometers (R2 and R3). The pulses are joined logically (NOR gate b2) and connected to the readout circuit. Doubling the horizontal synchronization pulse rate causes a pair of half-sized displays to be fashioned by the readout circuit. However, the first of these displays is deleted by inhibiting the passage of the readout circuit's output to the transmission gates until after

the second synchronization pulse occurs (NAND gate a4).

The display module is constructed with devices that consume little power, so that the video camera's power supply is sufficient to handle the increased electrical load. All connections made to the video camera and videotape recorder are available in the cable joining the camera and videotape recorder. Neither camera nor videotape recorder need internal modification.

A detailed list of components and suppliers is available from the author on request. The (1980) price of the electrical components is less than \$50.

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NOTES

1. By applying pairs of vertical and horizontal synchronization pulses to the readout circuit for each vertical and horizontal synchronization pulse applied to the camera, we have been able to produce four sets of readouts on the television screen. With very careful adjustment of time delays, it may be possible to obtain more.
2. The readout and digital clock circuits are available in a single package (National Semiconductor Corporation's MM58106). The use of this device would further simplify the construction of the display module.

(Received for publication July 20, 1980;
accepted August 2, 1980.)