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Quantum-dot cellular automata based reversible low power parity generator and parity checker design for nanocommunication*

Jadav Chandra DAS[1], Debashis DE‡[1,2]

([1]*Department of Computer Science and Engineering, West Bengal University of Technology, Kolkata 700064, India*)

([2]*Department of Physics, University of Western Australia, Crawley WA 6009, Australia*)

E-mail: jadav2u@gmail.com; dr.debashis.de@gmail.com

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Abstract: Quantum-dot cellular automata (QCA) is an emerging area of research in reversible computing. It can be used to design nanoscale circuits. In nanocommunication, the detection and correction of errors in a received message is a major factor. Besides, device density and power dissipation are the key issues in the nanocommunication architecture. For the first time, QCA-based designs of the reversible low-power odd parity generator and odd parity checker using the Feynman gate have been achieved in this study. Using the proposed parity generator and parity checker circuit, a nanocommunication architecture is proposed. The detection of errors in the received message during transmission is also explored. The proposed QCA Feynman gate outshines the existing ones in terms of area, cell count, and delay. The quantum costs of the proposed conventional reversible circuits and their QCA layouts are calculated and compared, which establishes that the proposed QCA circuits have very low quantum cost compared to conventional designs. The energy dissipation by the layouts is estimated, which ensures the possibility of QCA nano-device serving as an alternative platform for the implementation of reversible circuits. The stability of the proposed circuits under thermal randomness is analyzed, showing the operational efficiency of the circuits. The simulation results of the proposed design are tested with theoretical values, showing the accuracy of the circuits. The proposed circuits can be used to design more complex low-power nanoscale lossless nanocommunication architecture such as nano-transmitters and nano-receivers.

Key words: Quantum-dot cellular automata (QCA), Parity generator, Parity checker, Feynman gate, Nanocommunication, Power dissipation

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1 Introduction

In reversible computation, the most promising field of research is quantum-dot cellular automata (QCA), which can suppress the transistor-based complementary metal–oxide–semiconductor (CMOS) technology (Das and De, 2010; 2011; 2012; 2015a; 2015b; Das *et al.*, 2013; 2015). CMOS technology has several fundamental physical limits (Lent and Tougaw, 1997; ITRS, 2005). In recent times, there has been extensive research at the nanoscale to replace the traditional CMOS technology through so-called emerging technologies (Orlov *et al.*, 1997; Zhang *et al.*, 2004). These technologies have achieved extremely high device density with high operational speed. Among these, QCA not only gives a solution at the nanoscale but also opens up a new technique of computation. QCA is a new transistor-less nano-device that is amenable to nanoscale manipulations (Mardiris and Karafyllidis, 2010; Yang *et al.*, 2012; Agrawal and Ghosh, 2015; Das and De, 2015a; 2015b). QCA does not store the logic value as voltage as in CMOS but it is rather based on the individual electron's position within dots. Using the Coulombic interaction between electrons, the information can be propagated through QCA cells. As in QCA circuits, the logic operations are performed based on the

‡ Corresponding author

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ORCID: Debashis DE, http://orcid.org/0000-0002-9688-9806

polarization states of the QCA cell, and the power consumption by the QCA circuit is very low compared to traditional field-effect transistor based circuits (Aghababa *et al.*, 2012; Xiao *et al.*, 2012; Das and De, 2015a; 2015b). In nanocommunication devices, QCA reversible circuits have a major role in detecting an error within a message, as well as in lossless communication. Recently, serial communication architecture based on the parity generator and parity checker has been explored using QCA (Silva *et al.*, 2015). To perform serial communication, Silva *et al.* (2015) have proposed several QCA circuits such as the parallel-to-serial converter, serial-to-parallel converter, comparator, Hamming code generator, parity generator, and parity checker. Using these components, Silva *et al.* (2015) have designed two different QCA communication circuits, i.e., parity check-based communication architecture and Hamming code based communication architecture. These communication architectures have been tested and validated using the QCADesigner tool. The parity generator and parity checker proposed by Silva *et al.* (2015), however, are not reversible circuits. Also, they have not described the complexity of the parity generator and parity checker in terms of area, cell count, and delay in separation. Rather, the design and implementation of the parity circuits were explained along with the design of communication circuits. Besides, the proposed communication architectures are not reversible in nature. QCA design and implementation of the parity generator circuit were proposed by Sheikhfaal *et al.* (2015). The design is a four-bit even-parity generator, which is an irreversible circuit. Thus, in contrast to irreversible parity generator and parity checker circuits (Sheikhfaal *et al.*, 2015; Silva *et al.*, 2015), in this study we have for the first time proposed QCA-based design of reversible odd-parity generator and odd-parity checker circuits using the Feynman gate. Besides, in contrast to irreversible communication architectures proposed by Silva *et al.* (2015), an error detection scheme in the reversible nanocommunication system is explored. All the proposed circuits were designed and tested through QCA Designer-2.0.3 (Walus *et al*., 2004).

Widespread research works that illustrate reversible QCA logic circuits have been reported, but only a few papers have been devoted to the investigation of QCA-based reversible nanocommunication circuits. In nanocommunication architecture, the reversibility of the error detection circuit is a big issue in terms of area and power consumed by the circuit. Thus, the low device density and ultra-low power consumption of QCA have given the power to design, for the first time, the low-power nanoscale reversible odd-parity generator and odd-parity checker based on QCA using the Feynman gate to detect errors in a message.

2 Achievements

In nanocommunication, for lossless data transmission, the detection and correction of errors in the received information is a major issue. At the nanoscale, the architectural complexity of the hardware for error detection is a challenging aspect in terms of device density and power consumption.

The contributions of this work are as follows:

1. The design of the reversible Feynman gate in QCA is achieved.

2. Design of the reversible odd-parity generator circuit and odd-parity checker circuit is achieved using the Feynman gate with equal quantum cost, i.e., two, and garbage outputs, i.e., three.

3. Nanocommunication architecture is achieved using the proposed reversible odd-parity generator and odd-parity checker circuits with equal quantum cost and equal garbage values, i.e., five.

4. For the first time, the proposed reversible parity generator, parity checker, and nanocommunication circuit have been realized in QCA.

5. Quantum cost-based analyses of the proposed reversible circuits and their corresponding QCA layouts are performed.

6. The proposed Feynman gate is compared with existing circuits in terms of area, delay, and cell count.

7. The heat energy dissipated by the proposed designs is estimated.

8. Under thermal randomness, the polarization of output cells is observed and the reliability of the circuits is measured.

3 Reversible parity generator and parity checker circuit using QCA

3.1 Feynman gate (controlled-NOT) gate

The Feynman gate (FG) or CNOT gate is a 2×2 reversible gate. Its two inputs A and B are mapped to

the outputs P and Q as $P=A$ and $Q=A\oplus B$ (Toffoli, 1980), as shown in Fig. 1. Table 1 shows the truth table of the FG.

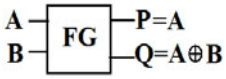


Fig. 1 Block diagram of the Feynman gate

Table 1 Truth table of the Feynman gate

Input		Output	
A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

The majority voter expression for the FG can be derived as

$$P=A, \tag{1}$$

$$Q=M(M(A', B, 0), M(A, B', 0), 1). \tag{2}$$

The QCA schematic representation of the proposed FG is shown in Fig. 2a and its corresponding layout in Fig. 2b.

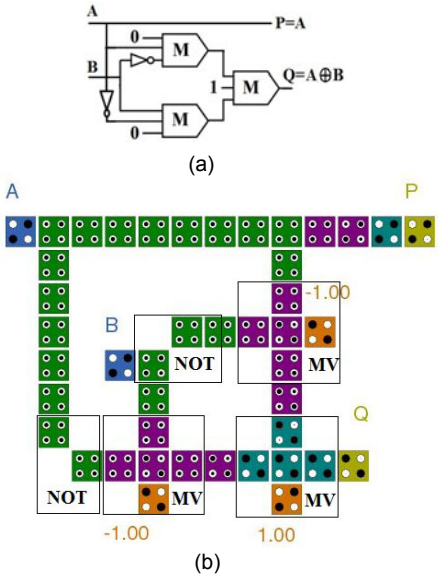


Fig. 2 Proposed Feynman gate: (a) QCA schematic; (b) QCA layout

3.2 Reversible odd-parity generator

Let the three inputs A, B, and C be the three bits of a message that has to be sent through the medium. P_b is the parity bit, i.e., output generated from the circuit (Mano and Ciletti, 2011). The parity bit P_b is so formed that the total number of 1's in the message becomes odd (including P_b). The logic expression of the three-bit odd-parity generator can be written as

$$P_b=A\odot B\oplus C. \tag{3}$$

Eq. (3) reflects that the logic expression of the three-bit odd-parity generator consists of one two-input XOR gate and one two-input XNOR gate. The two gates can be interchanged with each other. So, the expression for the output P_b can also be drawn as

$$P_b=A\oplus B\odot C. \tag{4}$$

The truth table is shown in Table 2. From the truth table, we can see that when the number of 1's in the message is even, i.e., either the inputs A, B, and C are all 0's or any two of the inputs A, B, and C are all 1's, then the value of P_b=1; otherwise, P_b=0.

To generate the parity bit P_b, only one XOR operation followed by one XNOR operation and vice versa are required. Thus, using two reversible FGs and one NOT gate, a three-bit odd-parity generator circuit can easily be achieved (Fig. 3).

Table 2 Truth table of the reversible odd-parity generator

Three-bit message			Generated parity bit P_b
A	B	C	
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

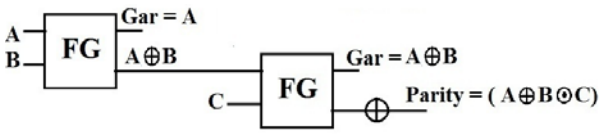


Fig. 3 Block diagram of the proposed reversible odd-parity generator circuit using the Feynman gate

As shown in Fig. 3, first the FG produces the XOR of the inputs A and B with one garbage value

equal to input A. The produced XOR-ed value of the inputs A and B of the first FG is then applied as an input to the second FG. The second FG generates the outputs as $A \oplus B$, which is treated as a garbage value, and $(A \oplus B) \oplus C$. The generated output value $(A \oplus B) \oplus C$ is propagated through a reversible NOT gate, which finally produces the required parity bit. Using Table 2, the majority gate expression of the proposed FG-based reversible odd-parity generator circuit in QCA can be drawn as

$$P_b = M(M(M(M(A', B, 0), M(A, B', 0), 1)', C, 0), M(M(M(A', B, 0), M(A, B', 0), 1), C', 0), 1)'. \quad (5)$$

The corresponding QCA schematic diagram and the QCA outline of the proposed FG-based reversible parity generator circuit are illustrated in Figs. 4a and 4b, respectively.

3.3 Reversible odd-parity checker

The odd-parity checker checks the parity bit that was padded within the message for error detection. An error occurs during transmission if the parity bit out of the four bits (three-bit message plus parity bit) is even, since the transmitted binary information was originally odd (Mano and Ciletti, 2011). When an error occurs, the value of output P_c=1, i.e., the number of 1's in the four bits is even. Table 3 shows the truth table for the four-bit odd-parity checker circuit.

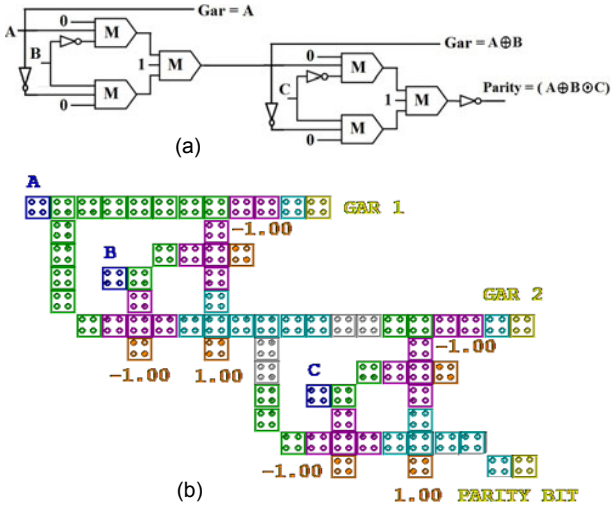


Fig. 4 The proposed reversible odd-parity generator circuit using the Feynman gate: (a) QCA schematic; (b) QCA layout

Table 3 Truth table of the reversible odd-parity checker circuit

4-bit message (including parity bit P_b)				Parity-bit error check
A	B	C	P_b	P_c
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

From the truth table (Table 3), it can be seen that the output P_c consists of eight minterms having an even number of 1's. Each value of P_c is the logical XNOR operation of the inputs A, B, C, and P_b. So, the logic expression for P_c can be written as

$$P_c = (A \odot B) \odot (C \odot P_b). \quad (6)$$

To generate the parity check bit P_c, only three XNOR operations are required, as shown in Eq. (6). Thus, using three reversible FGs and three reversible NOT gates, the four-bit odd-parity checker circuit can easily be achieved (Fig. 5).

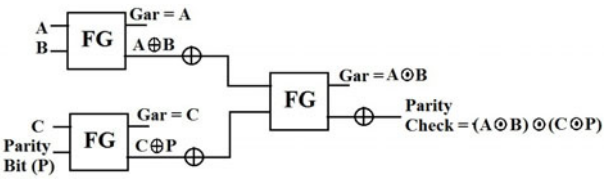


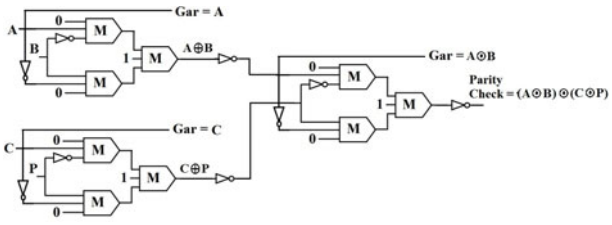
Fig. 5 Block diagram of the proposed reversible odd-parity checker circuit using the Feynman gate

As shown in Fig. 5, the first FG produces the XOR of the inputs A and B, i.e., $A \oplus B$, with one garbage value equal to input A. The produced XOR-ed value of the inputs A and B is then propagated through

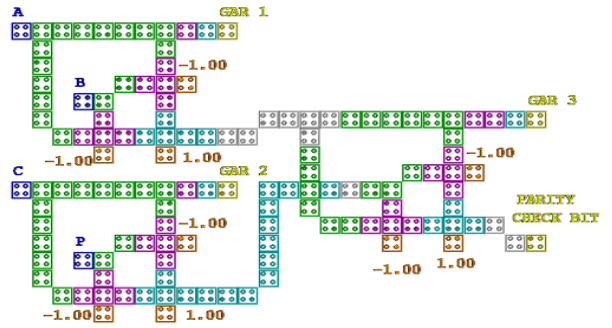
the first reversible NOT gate, which generates the XNOR of the inputs A and B, i.e., $A\Theta B$. Similarly, the second FG generates the output as $C\oplus P$, with the garbage value equal to input C. The resultant $C\oplus P$ is then passed through the second reversible NOT gate, which generates $C\Theta P$. The outputs of the first and second reversible NOT gates are then used as inputs for the third FG. The third FG generates the output as $(A\Theta B)\oplus(C\Theta P)$, with garbage $A\Theta B$. The generated output value $(A\Theta B)\oplus(C\Theta P)$ is then propagated through the third reversible NOT gate, which finally produces the required parity check bit. Using Table 3, the majority gate expression of the proposed FG-based reversible parity checker circuit in QCA can be drawn as

$$\begin{aligned}P_c=&M(M((M(M(A', B, 0), M(A, B', 0), 1)', \\ &M(M(C', P, 0), M(C, P', 0), 1)', 0), \\ &M(M(A', B, 0), M(A, B', 0), 1)', \\ &(M(M(C', P, 0), M(C, P', 0), 1)')', 1)'. \end{aligned} \quad (7)$$

The corresponding QCA schematic diagram and the QCA layout of the proposed FG-based reversible odd-parity checker circuit are expressed in Figs. 6a and 6b, respectively.



(a)



(b)

Fig. 6 Proposed reversible odd-parity checker circuit using the Feynman gate: (a) QCA schematic; (b) QCA layout

3.4 Proposed reversible odd-parity generator and odd-parity checker circuit based nanocommunication system

Fig. 7a shows the block diagram of a simple nanocommunication architecture using the proposed reversible odd-parity generator and odd-parity checker circuit. The nanocommunication circuit works as follows:

1. At the transmitter end, the parity generator takes the three-bit message as an input and generates the parity bit with only two garbage values.

2. The three-bit message and the generated parity bit are then sent via the communication medium to their destination, where they are moved through the parity checker circuit.

3. At the receiver end, the parity checker checks the parity bit that was padded within the message for error detection.

An error occurs during transmission if the parity bit out of the four bits (three-bit message plus parity bit) is even, since the transmitted binary information was originally odd. The truth table is described in Table 4. The truth table of the proposed nanocommunication system is achieved by considering the values of the parity bit as shown in Table 2. Thus, the inputs to the transmitter of the proposed nanocommunication system are the same as in Table 2, which causes all the outputs of the parity checker bit at the receiver end to be 0. Parity checker bits are all 0's because in the received four-bit message, i.e., each row of Table 4 at the receiver end, the number of 1's is always odd.

The QCA schematic diagram of the proposed nanocommunication circuit is shown in Fig. 7b and corresponding QCA layout in Fig. 7c.

Table 4 Truth table of the nanocommunication system

Parity generator				Parity checker				
3-bit message			Generated parity bit P_b	4-bit message				Parity checker bit P_c
A	B	C		A	B	C	P_b	
0	0	0	1	0	0	0	1	0
0	0	1	0	0	0	1	0	0
0	1	0	0	0	1	0	0	0
0	1	1	1	0	1	1	1	0
1	0	0	0	1	0	0	0	0
1	0	1	1	1	0	1	1	0
1	1	0	1	1	1	0	1	0
1	1	1	0	1	1	1	0	0

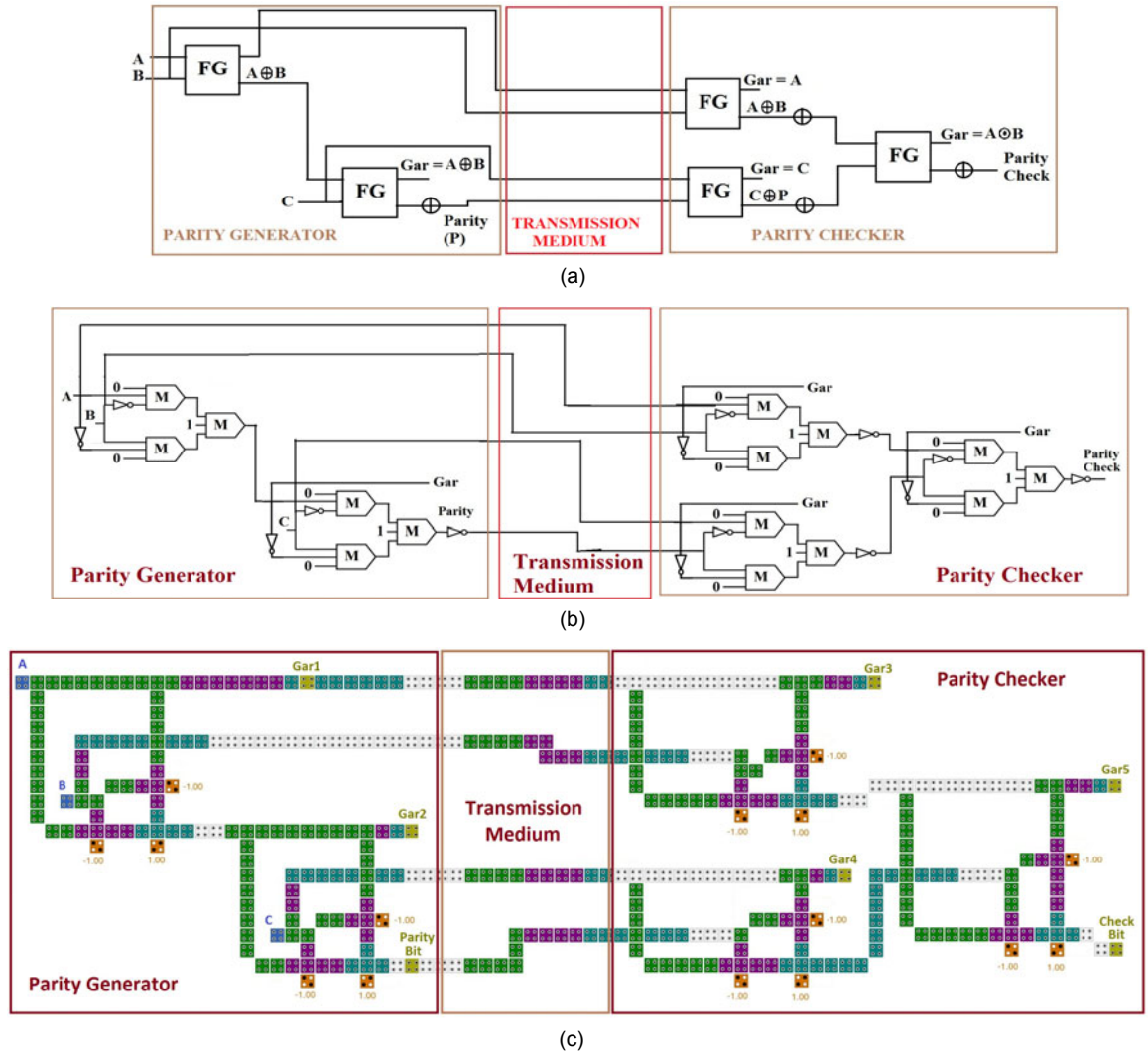


Fig. 7 Proposed reversible nanocommunication system: (a) block diagram; (b) QCA schematic; (c) QCA layout

4 Simulation results and discussion

The proposed circuits are implemented and simulated using the simulator QCA Designer-2.0.3, a bi-stable simulator (Walus *et al.*, 2004). The bi-stable approximation is performed using the parameters as follows:

1. QCA cell width is 18 nm and cell height is 18 nm;
2. The quantum dot diameter is 5 nm;
3. The amplitude factor is 2.0000;
4. The highest value of clock is 9.80000e–22 J and the lowest is 3.80000e–23 J;
5. The number of samples is 12 800;
6. The maximum number of iterations per sample is 10 000;
7. The radius of effect is 65.00 nm;
8. Relative permittivity is 12.900;
9. Layer separation is 11.50000 nm;
10. Convergence tolerance is 0.001000.

4.1 Simulation results of the proposed QCA circuits

4.1.1 Simulation results of the proposed QCA-based FG

Fig. 8a describes the simulation results of the proposed QCA-based FG. The results are confirmed with the theoretical values shown in Table 1. This evaluation demonstrates the efficiency of the circuit. Fig. 8a reflects that if the inputs are A=0 and B=0, then the outputs will be P=0 and Q=0, respectively. If

the inputs are A=0 and B=1, then the outputs will be P=0 and Q=1, respectively, and so on. Outputs for P and Q are started after the first clock pulse, as shown in Fig. 8a using arrows.

4.1.2 Simulation results of the proposed QCA reversible odd-parity generator circuit

Fig. 8b deals with the simulation results of the proposed reversible odd-parity generator circuit. The simulation results are tested with the theoretical values shown in Table 2. Fig. 8b describes that if the inputs are A=0, B=0, and C=0, then the outputs will be GAR1=0, GAR2=0, and parity bit P_b=1, respectively. When the inputs A=0, B=0, and C=1 are supplied to the circuit, then the outputs will be GAR1=0, GAR2=0, and parity bit P_b=0, respectively, and so on. Therefore, the circuit functions expertly. The output of parity bit P_b appears after the second clock pulse, as shown in Fig. 8b by an arrow. GAR1 and GAR2 in Fig. 8b stand for garbage outputs.

4.1.3 Simulation results of the proposed QCA reversible odd-parity checker circuit

The simulation results of the proposed reversible odd-parity checker circuit are explored in Fig. 8c. For inputs A=0, B=0, C=0, and P=0, the outputs will be GAR1=0, GAR2=0, GAR3=1, and parity check bit P_c=1, respectively. When the input values are A=0, B=0, C=0, and P=1, the output values will be GAR1=0, GAR2=0, GAR3=1, and parity check bit P_c=0, respectively, and so on. These simulation results are verified using theoretical values shown in Table 3. The evaluation shows that the circuit functions skillfully. The output parity check bit appears after the second clock pulse, as shown in Fig. 8c by an arrow. GAR1, GAR2, and GAR3 in Fig. 8c stand for garbage outputs.

4.1.4 Simulation results of the proposed QCA reversible nanocommunication circuit

Fig. 8d shows the simulation results of the proposed nanocommunication circuit. The results are verified with the truth table of the proposed nanocommunication circuit shown in Table 4. The verification shows that the communication circuit functions efficiently and produces correct outputs. The simulation results of the proposed nanocommunication circuit are described as follows.

1. Transmitter section

Fig. 8d illustrates that at the transmitter section, when the inputs to the parity generator are A=0, B=0, and C=0, then the outputs will be GAR1=0, GAR2=0, and parity bit P_b=1, respectively. When the inputs are A=0, B=0, and C=1, the outputs will be GAR1=0, GAR2=0, and parity bit P_b=0, respectively. Similarly, the other input combinations and their corresponding outputs are shown by the rectangular box in Fig. 8d. All these output values satisfy the truth table shown in Table 4. Thus, the transmitter circuit of the proposed nanocommunication system functions expertly. GAR1 and GAR2 in Fig. 8d are used to describe the garbage outputs. The outputs of GAR2 and parity bit P_b appear after the second clock pulse as shown by the arrows.

2. Receiver section

Fig. 8d demonstrates that at the receiver section, when the inputs to the parity checker are A=0, B=0, and C=0, the outputs at the decoder will be GAR3=0, GAR4=0, GAR5=1, and parity check bit P_c=0. When the inputs are A=0, B=0, C=1, and P_b=1, the outputs will be GAR3=0, GAR4=1, GAR5=1, and parity check bit P_c=0. Similarly, the outputs corresponding to other input combinations are shown by the rectangular box in Fig. 8d. All these output values are tested with the truth table shown in Table 4. Thus, the transmitter circuit of the proposed nanocommunication system is working efficiently. GAR3, GAR4, and GAR5 in Fig. 8d are used to describe the garbage outputs. The outputs of all output lines appear after the third clock pulse as shown by arrows in Fig. 8d.

4.2 Design complexity of the proposed QCA circuits

Table 5 shows the design complexities in terms of the number of majority voters, the number of QCA cells, the number of inverters, circuit density, and the number of clocking zones used to design the circuit.

4.3 Proposed QCA FG versus existing layouts

This section explores the comparison between the proposed QCA FG and existing ones (Ma, 2008; Rahman *et al.*, 2013; Biswas *et al.*, 2014; Kunalan *et al.*, 2014; Mohammadi and Mohammadi, 2014; Akter *et al.*, 2015; Das and De, 2015a; Shabeena and Pathak, 2015). The proposed FG is compared with existing layouts in terms of cell count, area, and delay. The results are shown in Table 6.

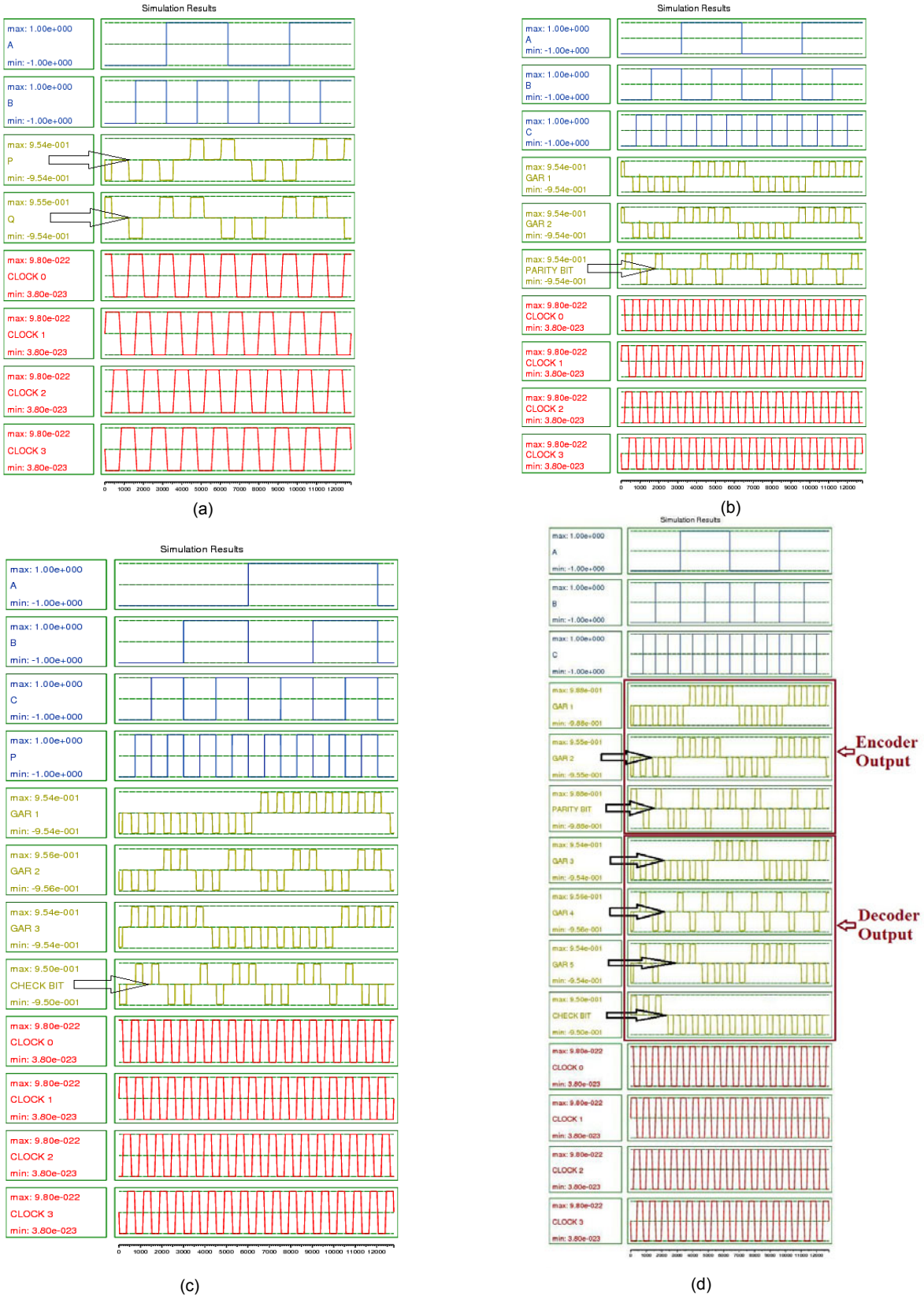


Fig. 8 Simulation results of QCA layout of the Feynman gate (a), odd-parity generator (b), odd-parity checker (c), and nanocommunication circuit (d)

Table 5 Complexity of the proposed circuit

Proposed QCA circuit	Number of majority voters	Number of inverters	Number of QCA cells	Total area (μm^2)	Cell area (μm^2)	Percentage of area usage (%)	Number of clocking zones
Feynman gate	3	2	43	0.038	0.014	36.84	3
Reversible odd-parity generator	6	5	72	0.078	0.023	30.00	4
Reversible odd-parity checker	9	9	130	0.143	0.042	29.41	4
Nanocommunication circuit	15	15	293	0.479	0.095	19.79	4

Table 6 demonstrates that the proposed FG has improvements of 44.87%, 47.94%, and 25% in terms of cell count, area, and delay, respectively, relative to the layout proposed by Ma (2008). The improvements over the design proposed by Rahman *et al.* (2013) are 28.33%, 51.28%, and 25% in terms of cell count, area, and delay, respectively. Similarly, the improvements over existing layouts (Biswas *et al.*, 2014; Kunalan *et al.*, 2014; Mohammadi and Mohammadi, 2014; Akter *et al.*, 2015; Das and De, 2015a; Shabeena and Pathak, 2015) are estimated (Table 6). The comparison shows that the proposed FG has less cell count and higher device density, and is faster than existing layouts.

Table 6 Proposed QCA Feynman gate and existing layouts

QCA Feynman gate	Cell count	Area (μm^2)	Delay (clock cycle)
Proposed	43	0.038	0.75
Ma (2008)	78 (44.87%)	0.073 (47.94%)	1.0 (25%)
Rahman *et al.* (2013)	60 (28.33%)	0.078 (51.28%)	1.0 (25%)
Mohammadi and Mohammadi (2014)	78 (44.87%)	0.09 (57.78%)	1.0 (25%)
Biswas *et al.* (2014)	75 (42.67%)	0.08 (52.50%)	1.0 (25%)
Kunalan *et al.* (2014)	62 (30.64%)	0.11 (65.45%)	1.0 (25%)
Akter *et al.* (2015)	51 (15.6%)	0.07 (45.71%)	0.75 (0%)
Shabeena and Pathak (2015)	84 (48.81%)	0.09 (57.78%)	1.0 (25%)
Das and De (2015a)	54 (20.37%)	0.039 (2.56%)	0.75 (0%)

The percentages in the brackets indicate the improvement of the respective performance of the proposed QCA Feynman gate over existing layouts

4.4 Quantum cost of the proposed reversible circuit and its QCA layout

The quantum cost of any 2×2 reversible gate is considered unity, whereas all reversible 1×1 gates (NOT gate) have a quantum cost of zero (Smolin and DiVincenzo, 1996; Hung *et al.*, 2006). Thus, the quantum cost of FG (CNOT gate) is one. The proposed reversible odd-parity generator circuit is composed of two FGs and one reversible NOT gate, whereas the reversible odd-parity checker circuit is composed of three FGs and three reversible NOT gates. The nanocommunication circuit requires five FGs and four reversible NOT gates. Therefore, the proposed odd-parity generator circuit has a quantum cost of (2×1+1×0), i.e., 2.0. Similarly, the odd-parity checker circuit and nanocommunication circuit have the quantum costs as 3.0 and 5.0, respectively (Table 7). The corresponding quantum costs of the proposed QCA circuits are estimated (Table 8).

Table 7 Quantum cost of the proposed reversible circuit

Proposed reversible circuit	Quantum cost	Garbage value	Number of FGs used
Feynman gate	1	0	–
Reversible odd-parity generator	2	2	2
Reversible odd-parity checker	3	3	3
Nanocommunication circuit	5	5	5

Table 8 Quantum cost of the proposed QCA layout

Proposed QCA circuit	Area (μm^2)	Latency (clock cycle)	Quantum cost*
Feynman gate	0.038	0.75	0.021
Reversible odd-parity generator	0.078	1.75	0.239
Reversible odd-parity checker	0.143	2.0	0.572
Nanocommunication circuit	0.479	2.0	1.916

* Quantum cost=area·latency^2

The proposed QCA FG has area 0.038 μm^2 and latency 0.75. Thus, the quantum cost of the proposed

QCA FG is area×latency^2=0.038×0.75^2, i.e., 0.021. The proposed QCA reversible odd-parity generator circuit has an area of 0.078 μm^2 and a latency of 1.75, which cause the quantum cost of the proposed QCA reversible odd-parity generator circuit to be area×latency^2=0.078×1.75^2, i.e., 0.239. Similarly, the quantum costs of other proposed circuits are calculated, and the results are shown in Table 8.

4.5 Quantum cost-based analysis of the proposed reversible circuit and its QCA layout

The comparative study of the proposed reversible circuits and their QCA layouts in terms of quantum cost is performed in this section. The quantum cost of FG in conventional design is 1.0, but in QCA-based design, it is only 0.021. For reversible odd-parity generator circuit, conventional design requires a quantum cost of 2.0, whereas QCA-based design requires a quantum cost of only 0.239. Similarly, the other proposed circuits are compared (Table 9). Table 9 shows that the quantum cost of QCA-based designs is lower than that of conventional designs. Thus, QCA-based designs are most cost-effective with respective to quantum cost. The relevant comparison is also illustrated in Fig. 9.

Table 9 Comparison of quantum cost of the proposed reversible circuit and its corresponding QCA layout

Proposed circuit	Quantum cost	
	Traditional design	QCA layout
Feynman gate	1	0.021
Reversible odd-parity generator	2	0.239
Reversible odd-parity checker	3	0.572
Nanocommunication circuit	5	1.916

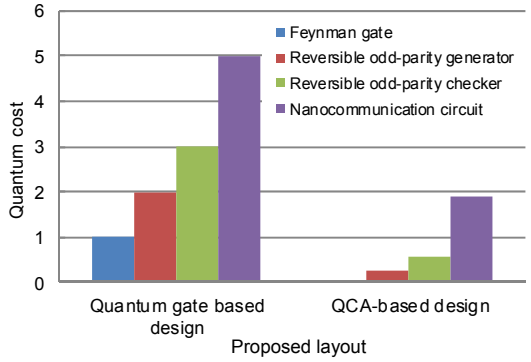


Fig. 9 Quantum cost of the proposed reversible circuit and its QCA layout

4.6 Power dissipation of the proposed reversible QCA circuits

The power dissipation by every cell in a QCA circuit is equivalent (Liu *et al.*, 2012). Thus, in an array of similar QCA cells, the total dissipated power can be estimated by totaling the dissipated power of all QCA cells within the array. The power consumption by the QCA circuit is dependent on the logic gates used in designing the circuit (Liu *et al.*, 2012). Use of a greater number of logic gates, i.e., the majority gate and inverter, implies higher power dissipation by the QCA circuits. The dissipated energy of the QCA circuit is the summation of the power dissipated by all the inverters, majority gates, and the array of QCA cells. Recently, estimate of energy dissipation by QCA layouts has been achieved at temperature T=2.0 K and at different tunneling energies such as $0.25E_k$ and $0.5E_k$ (Sheikhfaal *et al.*, 2015). The estimation has been carried out on a new five-input majority gate, an XOR gate, and parity generator circuits. Sheikhfaal *et al.* (2015) described the estimation of average leakage, as well as switching and total power dissipations, by these structures. The calculation is performed by using the QCA power dissipation tool QCAPro (Srivastava *et al.*, 2011).

In this paper, however, in spite of using the QCAPro power dissipation tool, mathematical analysis of Hamming distance based estimation of power dissipation (Liu *et al.*, 2012) is used to perform the energy dissipation calculation of the proposed designs. The estimation is performed using the same temperature (i.e., T=2.0 K) and the same tunneling energies (i.e., $0.25E_k$, $0.5E_k$, etc.), as in Sheikhfaal *et al.* (2015). It has been reported by Liu *et al.* (2012) that for an alteration in the Hamming distance between inputs to the QCA circuit, the power dissipation will also be varied. For example, Liu *et al.* (2012) showed that in the case of the inverter, 0→0 or 1→1 input switching means Hamming distance '0', and the inverter has 0.8 meV dissipated power at $\gamma=0.25E_k$ and 8.0 meV at $\gamma=1.0E_k$. For 0→1 or 1→0 input switching, Hamming distance '1' is considered for the inverter and then dissipation will be 28.4 meV at $\gamma=0.25E_k$ and 30.2 meV at $\gamma=1.0E_k$. A maximum Hamming distance of '3' is considered for the majority gate for 000→111 input switching, which causes the maximum dissipated energy of 41.0 meV by the majority gate at

γ=0.25E_k and 42.9 meV at γ=1.0E_k. Similarly, the power dissipation by the majority gate for different Hamming distances was reported in Liu *et al.* (2012).

Now, consider the QCA layout of the proposed FG shown in Fig. 2b. The QCA layout of the proposed FG consists of two inverters and three majority gates. Fig. 2b shows that each of these majority gates has one fixed input polarization cell. Thus, the Hamming distance for each of these majority gates is considered to be '2'. For maximum power dissipation, Hamming distance '1' is considered for each of the inverters in Fig. 2b. Using the Hamming distances corresponding to the input to logic gates and considering the QCA arrays present in FG as shown in Fig. 2b, the power dissipated by the proposed FG is calculated in this study. The results are presented in Table 10. A similar approach is used for estimating the power dissipation by the remaining proposed reversible circuits and the results are expressed in Table 10.

Table 10 Energy dissipated by the proposed QCA layouts for different γ's

Proposed QCA layout	Power dissipated at T=2.0 K (meV)			
	0.25E_k	0.5E_k	0.75E_k	1.0E_k
Feynman gate	105.1	110.5	118.2	127.6
Reversible odd-parity generator	293.8	301.4	313.9	329.8
Reversible odd-parity checker	426.5	437.8	456.2	479.6
Nanocommunication circuit	666.7	692.8	732.3	781.0

Table 10 describes that the power dissipated by the FG at γ=0.25E_k is 105.1 meV and at γ=1.0E_k, it is 127.6 meV. The power dissipated by the parity generator at γ=0.25E_k is 293.8 meV and at γ=1.0E_k, it is 329.8 meV, whereas for the parity checker circuit, it is 426.5 meV and 479.6 meV, respectively. The power dissipated by the nanocommunication circuit at γ=0.25E_k is 666.7 meV and at γ=1.0E_k, it is 781.0 meV. Here, T stands for temperature, γ stands for tunneling energy, and E_k represents the kink energy. These results show that all the circuits dissipate very low heat energy. The results are also outlined in Fig. 10.

4.7 Reliability of the proposed reversible QCA circuits

The average output polarization (AOP) of any output cell of the QCA circuit is reduced by raising the temperature (Pudi and Sridharan, 2011). The effect of temperature on the AOP of the proposed QCA circuits is shown in Fig. 11. The AOP of the output

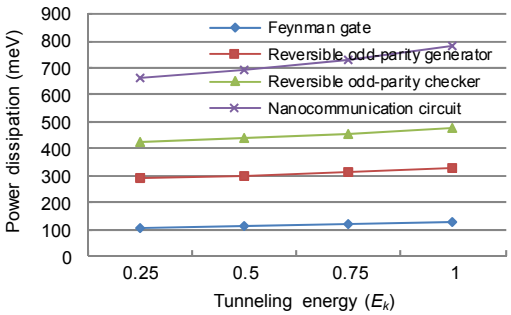


Fig. 10 Power dissipation by the proposed QCA reversible circuit (T=2.0 K)

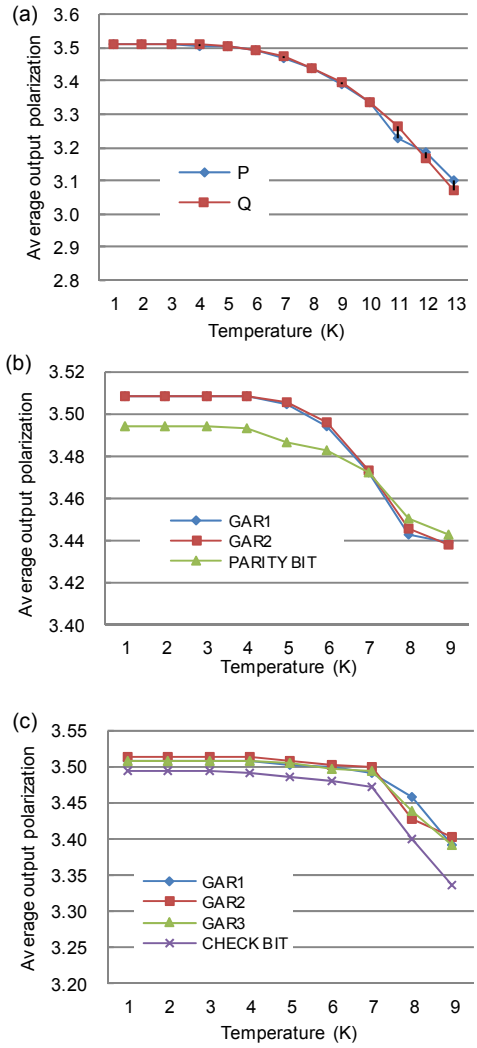


Fig. 11 Effect of temperature on average output polarization of the proposed QCA circuits: (a) FG; (b) parity generator; (c) parity checker

cells P and Q of the FG is gradually reduced, up to a temperature of T=11 K (Fig. 11a). Thus, in between 1 K and 11 K, the FG circuit works efficiently. Above T=11 K, the AOP is very low, and the circuit malfunctions. Similarly, the parity generator and parity checker circuit work competently between 1 K and 7 K (Figs. 11b and 11c). However, both circuits begin malfunctioning above T=7 K. To generate the AOP at different temperatures, all the proposed circuits are simulated by the QCADesigner tool and the maximum and minimum polarizations for each output cell are observed. For example, at T=1 K, the maximum and minimum polarizations of output cell Q of FG are 9.55e–1 and –9.54e–1, respectively. Therefore, the AOP for output cell Q is [(9.55e–1)–(–9.54e–1)]/2= 3.511 (Fig. 11a). In the same manner, the AOPs for different output cells of each proposed layout at different temperatures are calculated (Fig. 11).

5 Conclusions

In nanocommunication systems, the detection of errors in a received message is a key factor for lossless transmission of information. At the nanoscale, the most challenging aspect is the complexity of the nanocommunication hardware architecture used to detect errors in the received information in terms of power dissipation and device density. For the first time, the designs of the reversible odd-parity generator and odd-parity checker using QCA-based FG have been proposed in this paper. The proposed QCA–FG outshines the existing ones in terms of area, cell count, and delay. The quantum cost based analysis establishes that the proposed QCA circuits have very low quantum cost compared to conventional designs. The designs have very low heat energy dissipations, showing that QCA nano-devices are suitable for implementing reversible circuits. The analysis of stability of the proposed circuits under thermal randomness shows the stability of the circuits. The proposed circuits can be used to design more complex low-power nanoscale lossless nanocommunication architectures such as nano-transmitters and nano-receivers. The comparison of simulation results of the proposed design with theoretical values proves the functionality of the circuits.

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